

DESCRIPTION

TITLE OF THE INVENTION: SEMICONDUCTOR PACKAGE ASSEMBLY AND METHOD FOR FORMING THE SAME

TECHNICAL FIELD

[0001] The present application generally relates to manufacture of semiconductor devices, and more particularly, to semiconductor package assembly and method for forming the same.

BACKGROUND OF THE INVENTION

[0002] The semiconductor industry is constantly faced with complex integration challenges as consumers want their electronics to be smaller, faster and higher performance with more and more functionality packed into a single device. In some devices, a semiconductor package is integrated together with an inductor in the form of an assembly, and magnets in the inductor may have a limited heat dissipation ability. Therefore, for such semiconductor package assembly the overall heat dissipation ability may be limited, which may harm its performance due to heat accumulated during operation.

[0003] Thus, there exists a need for a semiconductor package assembly with an improved heat dissipation ability.

SUMMARY OF THE INVENTION

[0004] An objective of the present application is to provide a semiconductor package assembly with an improved heat dissipation ability.

[0005] According to an aspect of the present application, a semiconductor package assembly is provided. The semiconductor package assembly comprises: a semiconductor package comprising: a substrate; a semiconductor die mounted on the substrate; a pair of interconnection blocks mounted on the substrate and at opposite sides of the semiconductor die; and an encapsulant layer formed on the substrate to encapsulate the semiconductor die and the pair of interconnection blocks, wherein the pair of interconnection blocks have respective top surfaces exposed from the encapsulant layer and a top surface of the semiconductor die is exposed from the encapsulant layer;

and an inductor block mounted on the semiconductor package, wherein the inductor block comprises: an insulation body; an inductor extending through the insulation body in a horizontal direction of the insulation body, and having a pair of inductor contact pads exposed at a bottom surface of the insulation body, wherein the pair of inductor contact pads are aligned to and electrically coupled to the pair of interconnection blocks; and a thermally conductive coating formed at an outer surface of the insulation body and extending in a vertical direction of the insulation body from the bottom surface to a top surface of the insulation body, wherein the thermally conductive coating is thermally coupled to the semiconductor die to allow dissipation of heat generated by the semiconductor die through the thermally conductive coating..

[0006] According to another aspect of the present application, a method for forming a semiconductor package assembly is provided. The method comprises: providing a substrate; mounting a semiconductor die and a pair of interconnection blocks on the substrate, wherein the pair of interconnection blocks are mounted at opposite sides of the semiconductor die; forming an encapsulant layer on the substrate to encapsulate the semiconductor die and the pair of interconnection blocks but expose respective top surfaces of the pair of interconnection blocks and a top surface of the semiconductor die; providing an inductor block, wherein the inductor block comprises: an insulation body; an inductor extending through the insulation body in a horizontal direction of the insulation body, and having a pair of inductor contact pads exposed at a bottom surface of the insulation body; and a thermally conductive coating formed at an outer surface of the insulation body and extending in a vertical direction of the insulation body from the bottom surface to a top surface of the insulation body; and mounting the inductor block on the encapsulant layer such that the pair of inductor contact pads are aligned to and electrically coupled to the pair of interconnection blocks, and the thermally conductive coating is thermally coupled to the semiconductor die to allow dissipation of heat generated by the semiconductor die through the thermally conductive coating.

[0007] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only, and are not restrictive of the invention. Further, the accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description, serve to explain principles of the invention.

BRIEF DESCRIPTION OF DRAWINGS

[0008] The drawings referenced herein form a part of the specification. Features shown in the drawing illustrate only some embodiments of the application, and not of all embodiments of the application, unless the detailed description explicitly indicates otherwise, and readers of the specification should not make implications to the contrary.

[0009] Fig. 1A illustrates a cross-sectional view of a semiconductor package assembly according to an embodiment of the present application.

[0010] Fig. 1B illustrates a perspective view of an inductor block according to an embodiment of the present application.

[0011] Fig. 1C illustrates a top view of the inductor block shown in Fig. 1B.

[0012] Fig. 1D illustrates a front view of the inductor block shown in Fig. 1B.

[0013] Fig. 1E illustrates a bottom view of the inductor block shown in Fig. 1B.

[0014] Fig. 2 illustrates a perspective view of an inductor block according to another embodiment of the present application.

[0015] Figs. 3A to 3F illustrate steps for forming a semiconductor package assembly according to an embodiment of the present application.

[0016] Figs. 4A to 4C illustrate steps for forming solder paste and thermal interface material layer according to an embodiment of the present application.

[0017] The same reference numbers will be used throughout the drawings to refer to the same or like parts.

DETAILED DESCRIPTION OF THE INVENTION

[0018] The following detailed description of exemplary embodiments of the application refers to the accompanying drawings that form a part of the description. The drawings illustrate specific exemplary embodiments in which the application may be practiced. The detailed description, including the drawings, describes these embodiments in sufficient detail to enable those skilled in the art to practice the application. Those skilled in the art may further utilize other embodiments of the application, and make logical, mechanical, and other changes without departing from the spirit or scope of the application. Readers of the following detailed description should, therefore,

not interpret the description in a limiting sense, and only the appended claims define the scope of the embodiment of the application.

[0019] In this application, the use of the singular includes the plural unless specifically stated otherwise. In this application, the use of “or” means “and/or” unless stated otherwise. Furthermore, the use of the term “including” as well as other forms such as “includes” and “included” is not limiting. In addition, terms such as “element” or “component” encompass both elements and components including one unit, and elements and components that include more than one subunit, unless specifically stated otherwise. Additionally, the section headings used herein are for organizational purposes only, and are not to be construed as limiting the subject matter described.

[0020] As used herein, spatially relative terms, such as “beneath”, “below”, “above”, “over”, “on”, “upper”, “lower”, “left”, “right”, “vertical”, “horizontal”, “side” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly. It should be understood that when an element is referred to as being “connected to” or “coupled to” another element, it may be directly connected to or coupled to the other element, or intervening elements may be present.

[0021] Figs. 1A illustrates a cross-sectional view of a semiconductor package assembly 100 according to an embodiment of the present application. Fig. 1B illustrates a perspective view of an inductor block 120 of the semiconductor package assembly 100 according to an embodiment of the present application. Figs. 1C to 1E show views from different perspectives of the inductor block 120.

[0022] Referring to Fig. 1A, the semiconductor package assembly 100 generally includes a semiconductor package 110, and an inductor block 120 mounted on the semiconductor package 110. In particular, the semiconductor package 110 includes a substrate 111, a semiconductor die 112 mounted on the substrate 111, and a pair of interconnection blocks 113 mounted at opposite sides of the semiconductor die 112. In some embodiments, other electronic components 117 can also be mounted on the substrate 111 as desired.

[0023] The substrate 111 may be a multi-layer structure, and the multi-layer structure may include multiple insulating or passivation layers and multiple conductive layers formed over or between the insulating layers. The substrate 111 may include one or more laminated layers of polytetrafluoroethylene pre-impregnated, FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. The insulating layers may contain one or more layers of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), silicon oxynitride (SiON), tantalum pentoxide (Ta_2O_5), aluminum oxide (Al_2O_3), or other material having similar insulating and structural properties. The substrate 111 can also be a multi-layer flexible laminate, ceramic, copper clad laminate, glass, or semiconductor wafer including an active surface containing one or more transistors, diodes, and other circuit elements to implement analog circuits or digital circuits. The substrate 111 may include one or more electrically conductive layers or redistribution layers (RDL) formed using sputtering, electrolytic plating, electroless plating, or other suitable deposition process.

[0024] The semiconductor die 112 may take different forms and may have different functionality as desired. In some embodiments, the semiconductor die 112 may be a power module including one or more insulated gate bipolar transistor(s) (IGBT), one or more metal oxide semiconductor field effect transistor(s) (MOSFET), or one or more gate turn-off thyristor(s) (GTO). In some embodiments, the semiconductor die 112 may be a power supply integrated circuit that integrates at least a driver circuit and one or more MOSFET transistor(s). In such cases, the semiconductor die 112 may generate a relatively large amount of heat and requires efficient heat dissipation.

[0025] The pair of interconnection blocks 113 may take different forms and be made of different materials as desired. Preferably, each of the pair of interconnection blocks 113 may be made of one or more metal materials which have good thermal conductivity, such that the pair of interconnection blocks 113 may provide optimal heat conduction as well as structural support. More preferably, each of the pair of interconnection blocks 113 may be a Cu block.

[0026] An encapsulant layer 114 is formed on the substrate 111 to encapsulate the semiconductor die 112 and the pair of interconnection blocks 113. In some embodiments, the encapsulant layer 114 can be a polymer composite material, such as epoxy resin, epoxy acrylate, or any suitable polymer with or without filler. The encapsulant layer 114 may be non-conductive, provide structural support, and environmentally protect the electronic devices therein from external environment and contaminants. The encapsulant layer 114 may be formed with any shape as

desired. The encapsulant layer 114 may be formed by depositing an encapsulant or molding compound on the substrate 111 using injection molding, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or another suitable processes.

[0027] Specifically, top surfaces of the pair of interconnection blocks 113 and a top surface of the semiconductor die 112 are exposed from the encapsulant layer 114, such that electrical connection or heat dissipation directly from the respective top surfaces can be achieved.

[0028] The configuration of the encapsulant layer 114 and the semiconductor package 112 can vary as desired. In some embodiments, the semiconductor package 112 may have other components mounted thereon, and the top surface of the semiconductor package 112 may be indirectly exposed from the encapsulant layer 114. For example, as shown in Fig. 1A, a heat sink 115 is attached on the top surface of the semiconductor die 112, optionally via a thermal interface material layer 116 formed between the heat sink 115 and the semiconductor die 112, and the heat sink 115 may be at least partially exposed from the encapsulant layer 114, such that heat generated from the semiconductor die 112 may be dissipated via the thermal interface material layer 116 and the heat sink 115 to the external environment or further components.

[0029] The heat sink 115 and the thermal interface material layer 116 may take an area generally the same as the top surface of the semiconductor die 112. In some embodiments, the heat sink 115 may be made of the same material as the pair of interconnection blocks 113. Preferably, the heat sink 115 is made of Cu. In some embodiments, the thermal interface material layer 116 can be made of one or more thermally conductive, dispensable materials, preferably thermal greases, thermal adhesives, thermal gap fillers, liquid metal, and solder paste. In another embodiment, the thermal interface material layer 116 includes solder paste which has improved thermal conductivity over typical thermal interface materials. In some other alternative embodiments, the semiconductor package 112 may have a height generally the same as the pair of interconnection blocks 113, and a top surface of the semiconductor package 112 may be directly exposed from the encapsulant layer 114. In other words, there may be no heat sink and thus the thermal interface material layer formed on the top surface of the semiconductor package 112.

[0030] The inductor block 120 is mounted on the semiconductor package 110. Specifically, the inductor block 120 may include an insulation body 121 and an inductor 122 extending through the insulation body 121. In some embodiments, the insulation body 121 is formed of a magnetic molding compound and the inductor 122 is molded within the insulation body 121. The insulation

body 121 may provide high voltage resistance of inductor parts with a large concentration of highly permeable metal powder. In some embodiments, the insulation body 121 is made of a ferrite material.

[0031] The inductor 122 may take any form and material as desired. In some embodiments, the inductor 122 may be an inductor clip. Specifically, the inductor 122 may have a pair of inductor contact pads 123 exposed at a bottom surface of the insulation body 121. As shown in Fig. 1A, the pair of the inductor contact pads 123 are such positioned that they are aligned to the pair of interconnection blocks 113. Additionally, each inductor contact pad 123 may be electrically coupled together with one of the interconnection blocks 113 such as via direct contact or solder paste 130, and therefore, the inductor 122 may achieve electrical connection to the substrate 111 and other electronic components, such as the semiconductor die 112, via the pair of interconnection blocks 113.

[0032] As shown in Figs. 1A to 1E, a thermally conductive coating 124 is formed on an outer surface of the insulation body 121 to assist heat dissipation. Specifically, the thermally conductive coating 124 is formed to be in thermal contact with the semiconductor die 112 underneath. Also, the thermally conductive coating 124 may at least partially extend in a vertical direction of the insulation body 121 from the bottom surface to the top surface of the insulation body 121.

[0033] In an embodiment, as shown in Fig. 1A to 1E, the inductor block 120 may include two inductors 122, and each inductor may have a corresponding thermally conductive coating portion formed to surround the inductor. In some embodiments, as shown in Fig. 1B, the thermally conductive coating portions corresponding to different inductors may be separated from each other to avoid undesired thermal crosstalk. In some other embodiments, the thermally conductive coating portions may be a continuous coating instead of segmented coatings.

[0034] The thermally conductive coating 124 with respect to the inductors 122 may be positioned to efficiently use the bottom surface of the insulation body 121, as well as to achieve optimal heat dissipation. Preferably, the inductors 122 may be symmetrically arranged to extend horizontally, such as along a longer side of the insulation body 121, and the two thermally conductive coating portions may be symmetrically formed relative to a central line of the insulation body 121 extending in the inductors' extension direction. Each thermally conductive coating portion may be formed with multiple sub-portions. For example, as shown in Fig. 1B, the front thermally conductive coating portion may include a sub-portion 124-1 on the top surface of the insulation

body 121, a sub-portion 124-2 on the front surface of the insulation body 121, and a sub-portion 124-3 on the bottom surface of the insulation body 121. The sub-portion 124-1 may assist heat dissipation to an external environment vertically over the inductor block 120. In some embodiments, another heat spreader may be arranged on top of the sub-portion 124-1 to further assist heat dissipation. The sub-portion 124-2 may assist heat dissipation to an external environment at a side of the inductor block 120. And the sub-portion 124-3 may be arranged to be in thermal contact with the semiconductor die 112 underneath. Such arrangement may allow heat generated by the semiconductor die 112 to be dissipated in various directions to the external environment via a relatively large area. Also, as shown in the bottom view of Fig. 1E, in such arrangement, the pair of inductor contact pads 123 are located at both ends of the longer side of the insulation body 121, while the sub-portion 124-3 takes a relatively central position and most of the area of the bottom surface of the insulation body 121. Preferably, a width of the thermally conductive coating 124 in the horizontal direction of the insulation body 121 may be between 50% and 100% of a length of the inductor 122 in the horizontal direction of the insulation body 121. Therefore, the area of the bottom surface of the insulation body 121 is efficiently used, and an area for thermal contact between the thermally conductive coating 124 and the semiconductor die 112 is relatively large. It can also be understood that, the thermally conductive coating 124 may also help dissipate heat accumulated inside the insulation body 121.

[0035] The heat conduction from the semiconductor die 112 to the thermally conductive coating 124 may vary according to the specific structure of the semiconductor package assembly 100. In some embodiments, as shown in Fig. 1A, the semiconductor package 110 may include the thermal interface material layer 116 and the heat sink 115 on the top surface of the semiconductor die 112. On the heat sink 115, a thermal interface material layer 140 may be disposed. Therefore, heat generated by the semiconductor die 112 can be conducted via the thermal interface material layer 116, the heat sink 115, and the thermal interface material layer 140 to the thermally conductive coating 124 and be dissipated therethrough.

[0036] In some other embodiments (not shown), a top surface of the semiconductor die 112 may be directly exposed from the encapsulant layer 114, the inductor block 120 may be in direct contact with the semiconductor package 110, and the thermally conductive coating 124 may be in direct contact with the top surface of the semiconductor die 112. In this case, heat generated by the

semiconductor die 112 may be conducted directly to the thermally conductive coating 124, and heat may be dissipated therethrough.

[0037] The thermally conductive coating 124 may be made of any suitable material for heat dissipation. Preferably, the thermally conductive coating 124 may be made of metal, such as Cu, Al, Ag or metal alloy. Preferably, the thermally conductive coating 124 is made of Cu.

[0038] In some embodiments, in order to improve the reliability of connection between the inductor block 120 and the semiconductor package 110, an under-fill material layer 150 may be formed between the bottom surface of the insulation body 121 and the top surface of the encapsulant layer 114. In some embodiments, the under-fill material layer 150 may be formed of an encapsulant material. Such under-fill material layer 150 may fill in a gap between the inductor block 120 and the semiconductor package 110 which is not occupied by the solder paste 130 and the optional thermal interface material layer 140. The under-fill material layer 150 may advantageously minimize the coefficient of thermal expansion between the two components connected by the under-fill material layer 150, increase the solder joint reliability, and structurally protect the semiconductor die 112.

[0039] The configuration of the inductor and the thermally conductive coating of the inductor block may vary as desired. For example, as shown in Fig. 2, the inductor block 220 may include one inductor 222 molded within the insulation body 221. The thermally conductive coating 224 may be formed to continuously surround the inductor 222. It can be understood that, the number, position and form of the inductor and the thermally conductive coating may vary as desired.

[0040] The present semiconductor package assembly may improve the power density, efficiency and thermal performance, which results in improved overall performance, especially when it is used in applications where power consumption is high and/or signal processing is continuous, such as in a server.

[0041] Figs. 3A to 3F illustrate steps of a method for forming a semiconductor package assembly according to an embodiment of the present application. For example, the method may be used to form the semiconductor package assembly shown in Figs. 1A to 1E.

[0042] Referring to Fig. 3A, a substrate 311 is provided, and a semiconductor die 312 and a pair of interconnection blocks 313, and optionally, an electronic component 317 are mounted on the substrate 311, wherein the pair of interconnection blocks 313 are mounted at opposite sides of the semiconductor die 312.

[0043] In some embodiments, a height difference between the semiconductor die 312 and the pair of interconnection blocks 313 may be relatively large, and additional components may be disposed on the semiconductor die 312 to make up the height difference. For example, as shown in Fig. 3B, a thermal interface material layer 316 may be formed on the semiconductor die 312. The thermal interface material layer 316 can be made of thermally conductive, dispensable materials, preferably thermal greases, thermal adhesives, thermal gap fillers, liquid metal, and solder paste. The thermal interface material layer 316 may be formed with any suitable process, for example dispensing a thermal interface material, CVD, PVD, etc. Then, referring to Fig. 3C, a heat sink 315 may be attached on the thermal interface material layer 316 on the top surface of the semiconductor die 312. The heat sink 315 may be made of metal, such as Cu, such that heat generated by the semiconductor die 312 may be conducted upwards through the heat sink 315. After the heat sink 315 is attached, a top surface of the heat sink 315 may or may not level with a top surface of the pair of interconnection blocks 313.

[0044] Referring to Fig. 3D, an encapsulant layer 314 is formed on the substrate 311 to encapsulate the semiconductor die 312 and the pair of interconnection blocks 313, the thermal interface material layer 316 and the heat sink 315. The components may be fully encapsulated.

[0045] Referring to Fig. 3E, a grinding process may be performed to at least partially expose a top surface of the pair of interconnection blocks 313 and a top surface of the heat sink 315 to the external environment. It can be understood that, in this case, a top surface of the semiconductor die 312 is free from and indirectly exposed from the encapsulant layer 314. After the grinding process, a semiconductor package 310 is formed, and electrical connection from an inductor block to be attached above the semiconductor package 310 to the pair of interconnection blocks 313 may be achieved, and thermal conduction from the semiconductor die 312 via the heat sink 315 to the inductor block to be attached above the semiconductor package 310 may be achieved.

[0046] It can be understood that, in some other embodiments, the encapsulant layer 314 may be firstly formed, then a laser ablation process may be adopted to form a cavity on the semiconductor die, and then the thermal interface material layer 316 and the heat sink 315 may be formed.

[0047] It can also be understood that, in some other embodiments, a height of the pair of interconnection blocks 313 and a height of the heat sink 315 can be determined in advance such that after the heat sink 315 is attached on the semiconductor die 312, a top surface of the pair of interconnection blocks 313 and the top surface of the heat sink 315 may level with each other. In

such cases, a film-assisted molding process may be adopted, and no grinding process would be needed.

[0048] It can also be understood that, in some embodiments, the formation of the semiconductor package 310 may be carried out in a wafer-level, and the semiconductor package 310 and other similar packages may be singulated from a substrate strip before an inductor block is mounted on each of the semiconductor packages. In the case where a height of the inductor block is relatively large and the inductor block may be tilted after being mounted on the semiconductor package 310, the risk of the inductor block being damaged during singulation is reduced.

[0049] Referring to Fig. 3F, after the formation of the semiconductor package 310, an inductor block 320 is provided and mounted on the encapsulant layer 314 of the semiconductor package 310. The configuration of the inductor block 320 may refer to the inductor block 120 illustrated above with reference to Fig. 1A and would not be repeated herein. The inductor block 320 may be positioned, for example via a pick-and-place machine, such that the pair of inductor contact pads 323 are aligned to and electrically coupled to the pair of interconnection blocks 313, and the thermally conductive coating 324 is thermally coupled to the semiconductor die 312 to allow dissipation of heat generated by the semiconductor die 312 through the thermally conductive coating 324.

[0050] The configurations at the interface between the semiconductor package 310 and the inductor block 320 may vary as desired. As shown in Fig. 3F, in some embodiments, solder paste 330, a thermal interface material layer 340, and an under-fill material layer 350 may be formed between the inductor block 320 and the semiconductor package 310. The solder paste 330 and the thermal interface material layer 340 may be formed to assist electrical connection and thermal conductivity, respectively. The under-fill material layer 350 may help improve the reliability of the overall structure. The solder paste 330, the thermal interface material layer 340, and the under-fill material layer 350 may be formed via any suitable process. In some embodiments, the thermal interface material layer 340 and the under-fill material layer 350 can also be formed before or after the attachment of the inductor block 320, such as by depositing thermal interface material and encapsulant material in-between the semiconductor package 310 and the inductor block 320, respectively.

[0051] In some embodiments, the solder paste and thermal interface material layer may be formed via a stencil printing process. Figs. 4A to 4C illustrate steps for forming solder paste and thermal

interface material layer according to an embodiment of the present application, which may be alternative to the method shown in Figs. 3A to 3F.

[0052] Referring to Fig. 4A, a stencil 500 may be disposed on the semiconductor package 410. The stencil 500 may have a pair of through holes 501 at a position over the pair of interconnection blocks 413, such that solder paste 430 (shown in Fig. 4B) may be formed in the through holes 501 in a solder paste printing process.

[0053] Referring to Figs. 4B and 4C, a thermal interface material layer may be formed via a stencil printing process with a half-etched stencil 600. Specifically, the half-etched stencil 600 may include a through hole 601 at a position over the semiconductor die 412, and a pair of etched portion 602 at a position of the solder paste 430. Each etched portion 602 may take the form of a blind hole, such that the solder paste 430 may be accommodated within the pair of etched portion 602 and would not be exposed by the half-etched stencil 600. A thermal interface material layer 440 (shown in Fig. 4C) may be formed in the through hole 601 in a thermal interface material printing process.

[0054] It can be understood that, with the process described above, the solder paste 430 and the thermal interface material layer 440 may be formed separately without being affected by each other. As illustrated in the aforementioned embodiments, the solder paste 430 may be used for the electrical connection between the pair of interconnection blocks 413 underneath and a pair of inductor contact pads of an inductor block to be mounted above, and the thermally conductive coating 440 may be used for thermal conduction from the semiconductor die 412 underneath to a thermally conductive coating of an inductor block to be mounted above.

[0055] The discussion herein included numerous illustrative figures that showed various portions of a semiconductor package assembly and method for forming the same. For illustrative clarity, such figures did not show all aspects of each example assembly. Any of the example assemblies and/or methods provided herein may share any or all characteristics with any or all other assemblies and/or methods provided herein.

[0056] Various embodiments have been described herein with reference to the accompanying drawings. It will, however, be evident that various modifications and changes may be made thereto, and additional embodiments may be implemented, without departing from the broader scope of the invention as set forth in the claims that follow. Further, other embodiments will be apparent to those skilled in the art from consideration of the specification and practice of one or

more embodiments of the invention disclosed herein. It is intended, therefore, that this application and the examples herein be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following listing of exemplary claims.

Claims

Claim 1: A semiconductor package assembly, comprising:

a semiconductor package comprising:

a substrate;

a semiconductor die mounted on the substrate;

a pair of interconnection blocks mounted on the substrate and at opposite sides of the semiconductor die; and

an encapsulant layer formed on the substrate to encapsulate the semiconductor die and the pair of interconnection blocks, wherein the pair of interconnection blocks have respective top surfaces exposed from the encapsulant layer and a top surface of the semiconductor die is exposed from the encapsulant layer; and

an inductor block mounted on the semiconductor package, wherein the inductor block comprises:

an insulation body;

an inductor extending through the insulation body in a horizontal direction of the insulation body, and having a pair of inductor contact pads exposed at a bottom surface of the insulation body, wherein the pair of inductor contact pads are aligned to and electrically coupled to the pair of interconnection blocks; and

a thermally conductive coating formed at an outer surface of the insulation body and extending in a vertical direction of the insulation body from the bottom surface to a top surface of the insulation body, wherein the thermally conductive coating is thermally coupled to the semiconductor die to allow dissipation of heat generated by the semiconductor die through the thermally conductive coating.

Claim 2: The semiconductor package assembly of claim 1, the semiconductor package further comprising:

a heat sink attached on the top surface of the semiconductor die and exposed from the encapsulant layer, and

a thermal interface material layer formed between the heat sink and the insulation body of the inductor block, such that the semiconductor die is thermally coupled to the thermally conductive coating via the heat sink and the thermal interface material layer.

Claim 3: The semiconductor package assembly of claim 1, wherein the insulation body is formed of a magnetic molding compound, and the inductor is molded within the insulation body.

Claim 4: The semiconductor package assembly of claim 1, wherein a width of the thermally conductive coating along the horizontal direction of the insulation body is between 50% to 100% of a length of the inductor along the horizontal direction of the insulation body.

Claim 5: The semiconductor package assembly of claim 1, wherein the thermally conductive coating comprises a first portion and a second portion which are symmetrically formed relative to a central line of the insulation body extending in the horizontal direction.

Claim 6: The semiconductor package assembly of claim 1, further comprising: an under-fill material layer formed between the bottom surface of the insulation body and a top surface of the encapsulant layer.

Claim 7: A method for forming a semiconductor package assembly, comprising:

providing a substrate;

mounting a semiconductor die and a pair of interconnection blocks on the substrate, wherein the pair of interconnection blocks are mounted at opposite sides of the semiconductor die;

forming an encapsulant layer on the substrate to encapsulate the semiconductor die and the pair of interconnection blocks but expose respective top surfaces of the pair of interconnection blocks and a top surface of the semiconductor die;

providing an inductor block, wherein the inductor block comprises: an insulation body; an inductor extending through the insulation body in a horizontal direction of the insulation body, and having a pair of inductor contact pads exposed at a bottom surface of the insulation body; and a thermally conductive coating formed at an outer surface of the insulation body and extending in a vertical direction of the insulation body from the bottom surface to a top surface of the insulation body; and

mounting the inductor block on the encapsulant layer such that the pair of inductor contact pads are aligned to and electrically coupled to the pair of interconnection blocks, and the thermally conductive coating is thermally coupled to the semiconductor die to allow dissipation of heat generated by the semiconductor die through the thermally conductive coating.

Claim 8: The method of claim 7, wherein before mounting the inductor block, the method further comprises: attaching a heat sink on the top surface of the semiconductor die, wherein a top surface of the heat sink is exposed from the encapsulant layer; and

the method further comprises: forming a thermal interface material layer on the heat sink and under the insulation body of the inductor block, such that the semiconductor die is thermally coupled to the thermally conductive coating via the heat sink and the thermal interface material layer.

Claim 9: The method of claim 8,

wherein before forming a thermal interface material layer, the method comprises: forming solder paste on the encapsulant layer, such that the pair of inductor contact pads are electrically coupled to the pair of interconnection blocks via the solder paste; and

wherein when forming a thermal interface material layer, a half etched stencil is used such that the solder paste is accommodated within an etched portion of the half etched stencil.

Claim 10: The method of claim 7, wherein the insulation body is formed of a magnetic molding compound, and the inductor is molded within the insulation body.

Claim 11: The method of claim 7, wherein a width of the thermally conductive coating along the horizontal direction of the insulation body is between 50% to 100% of a length of the inductor along the horizontal direction of the insulation body.

Claim 12: The method of claim 7, wherein the thermally conductive coating comprises a first portion and a second portion which are symmetrically formed relative to a central line of the insulation body extending in the horizontal direction.

Claim 13: The method of claim 7, further comprising: forming an under-fill material layer between the bottom surface of the insulation body and a top surface of the encapsulant layer.