CLAIMS

I/We claim:

1. A method of manufacturing stacked semiconductor assemblies, comprising:

mounting a semiconductor wafer to a temporary carrier wherein the wafer has a plurality of first dies arranged in a die pattern on the wafer;

thinning the wafer;

attaching a plurality of singulated second dies to corresponding first dies, wherein the second dies are arranged in the die pattern and spaced apart from each other by gaps;

disposing an encapsulating material in the gaps between the second dies; and

thinning the second dies after attaching the second dies to the first dies.

2. The method of claim 1 wherein thinning the second dies includes grinding a back side of the second dies.

3. The method of claim 1, further comprising cutting through the encapsulating material in the gaps and cutting the wafer to singulate stacked microelectronic devices having a first die and a corresponding second die.

4. The method of claim 1 wherein:

individual first and second dies include an integrated circuit and a terminal electrically coupled to the integrated circuit; and

before mounting the wafer to the temporary carrier, the method further comprises forming an interconnect in at least a portion of the individual first dies in electrical contact with the terminal;

thinning the wafer comprises simultaneously exposing a plurality of first die interconnects at a back side of the wafer that define external contacts; and

attaching the second dies to the first dies further comprises electrically coupling front side terminals of the second dies to corresponding external contacts at the back side of the wafer.

5. The method of claim 1 wherein:

before attaching the plurality of second dies to corresponding first dies, the method further comprises testing individual first dies and individual second dies to determine known good first and second dies and known bad first and second dies; and

attaching the second dies to corresponding first dies comprises attaching known good second dies to known good first dies and attaching known bad second dies to known bad first dies to form a plurality of known good stacked devices and a plurality of known bad stacked devices.

6. The method of claim 1, further comprising:

attaching singulated third dies to corresponding second dies such that the third dies are spaced apart from each other by gaps;

disposing additional encapsulant material in the gaps between the third dies; and

removing material from a back side of the third dies after disposing the encapsulant material in the gaps between the third dies.

7. The method of claim 1 wherein the individual second dies have a handling thickness when the second dies are attached to the first dies, and thinning the second dies comprises reducing the thickness of the second dies to about 20-150 microns.

8. The method of claim 1 wherein the individual second dies have a handling thickness when the second dies are attached to the first dies, and thinning the second dies comprises reducing the thickness of the second dies to less than 100 microns.

9. The method of claim 1 wherein the wafer has an initial thickness before thinning of approximately 700-1000 microns, and thinning the wafer comprises reducing the thickness to approximately less than 50 microns, wherein the individual second dies have a handling thickness greater than 150 microns when the second dies are attached to the first dies, and thinning the second dies comprises reducing the thickness of the second dies to about 20-150 microns.

10. A method of manufacturing semiconductor workpieces, comprising:

reducing an initial thickness of a semiconductor wafer between a front side of the wafer and a back side of the wafer, wherein the wafer has a plurality of first dies and first interconnects;

mounting a plurality of separated second dies to corresponding first dies in a stacked configuration to form a plurality of stacked microelectronic devices, wherein individual second dies have second interconnects connected to terminals on a first side of the second die and extending to an intermediate level such that the second interconnects are not exposed on a second side of the second die opposite the first side;

at least partially encapsulating the stacked devices; and

thinning the second dies and exposing the second interconnects on the second side after at least partially encapsulating the stacked devices.

11. The method of claim 10 wherein reducing the initial thickness of the semiconductor wafer comprises reducing the initial thickness between the front side and the back side to approximately less than 100 microns, and wherein thinning the second dies comprises reducing a second die thickness between the first and second sides to less than 300 microns.

12. The method of claim 11 wherein:

before mounting the plurality of second dies to corresponding first dies, the method further comprises testing individual first dies and individual second dies to determine known good first and second dies and known bad first and second dies; and

mounting the second dies to corresponding first dies comprises mounting known good second dies to known good first dies arranged in a stacked configuration and mounting known bad second dies to known bad first dies arranged in a stacked configuration to form a plurality of known good stacked devices and known bad stacked devices.

13. The method of claim 10 wherein thinning the second dies comprises simultaneously thinning the second dies to a thickness between the first and second sides of approximately less than 300 microns.

14. The method of claim 10 wherein:

before encapsulating the stacked devices, the method further comprises dispensing an underfill material between the second dies and the wafer; and

thinning the second dies includes grinding the second sides of the second dies while in a stacked configuration.

15. The method of claim 11 wherein the initial thickness of the semiconductor wafer is approximately 500-1000 microns and the second die have thickness of approximately 500-1000 microns after the mounting stage but before the thinning stage.

16. A method of manufacturing semiconductor assemblies, the method comprising:

forming first and second semiconductor wafers having front sides and back sides opposite the front sides and an array of dies at the front sides arranged in a die pattern, the individual dies including an integrated circuit and a terminal electrically coupled to the integrated circuit;

forming a plurality of interconnects in electrical contact with the die terminals on the first and second wafers;

attaching a carrier substrate to the front side of the first wafer;

processing the back side of the first wafer to form a thinned base wafer with exposed interconnect studs;

dividing the second wafer to form singulated second dies;

populating the first dies with singulated second dies to form an array of stacked semiconductor devices in the die pattern, wherein the terminals on the front side of the second dies are electrically coupled with the corresponding interconnect studs of the first dies;

at least partially encapsulating the stacked devices; and

grinding the back side of the second dies after encapsulating the stacked devices.

17. The method of claim 16 wherein:

before populating the first dies with the second dies, the method further comprises testing individual first dies and second dies to determine known good first and second dies and known bad first and second dies; and

populating the first dies with second dies comprises attaching known good second dies to known good first dies arranged in a stacked configuration and attaching known bad second dies to known bad first dies arranged in a stacked configuration to form a plurality of known good stacked devices and known bad stacked devices.

18. A semiconductor assembly, comprising:

a thinned semiconductor wafer having an active side, a back side opposite the active side, and a plurality of first dies arranged in a die pattern at the active side, wherein individual first dies have an integrated circuit and first through die interconnects electrically connected to the integrated circuit, and wherein the first through die interconnects have interconnect contacts exposed at the back side of the wafer; and

a plurality of separate second dies spaced apart from each other and arranged in the die pattern relative to the thinned semiconductor wafer, individual second dies having a second active side, a second back side, a second integrated circuit, and a second terminal electrically coupled to the second integrated circuit on the second active side, wherein the individual second dies have a thickness of approximately less than 150 microns.

19. The assembly of claim 18, further comprising an underfill deposited between the first and second dies.

20. The assembly of claim 18 wherein the thickness of the plurality of second dies is substantially uniform across the thinned semiconductor wafer.

21. The assembly of claim 18 wherein the thinned semiconductor wafer has a thickness of approximately less than 100 microns.

22. The assembly of claim 18 wherein the thinned semiconductor wafer has a wafer thickness of approximately less than 50 microns and the thickness of the second die is approximately less than 50 microns.

23. The assembly of claim 18, further comprising:

a plurality of separate third dies spaced apart from each other and arranged in the die pattern relative to the thinned semiconductor wafer, individual third dies having a third active side, a third back side, a third integrated circuit, a third terminal electrically coupled to the third integrated circuit on the third active side, wherein the third die has a thickness of approximately less than 100 microns.

24. An intermediate stacked semiconductor assembly, comprising:

a thinned semiconductor wafer having an active side, a plurality of first dies arranged in a die pattern, and first through die interconnects extending from the active side to a back side of the wafer;

a plurality of singulated second dies mounted to corresponding first dies, wherein the individual second dies are spaced apart from each other by gaps, and wherein the second dies have a first side, a second side spaced apart from the first side by a handling thickness, and a second interconnect extending from the first side to an intermediate depth in the second die such that the second interconnects are not exposed on the second side of the second dies; and

an encapsulant in the gaps.

25. The assembly of claim 24 wherein the individual second dies have a handling thickness approximately greater than 300 microns.

26. The assembly of claim 24 wherein the thinned semiconductor wafer has a final thickness approximately less than 50 microns.

27. A semiconductor assembly, comprising:

a wafer including a plurality of known good first dies and a plurality of known bad first dies;

a plurality of separated known good second dies attached to corresponding known good first dies, and a plurality of separated known bad second dies attached to corresponding known bad first dies, wherein the second dies are spaced apart from each other by gaps; and

an encapsulant material in the gaps.

28. The assembly of claim 27 wherein the wafer has a thickness approximately less than 100 microns.

29. The assembly of claim 27 wherein the separated second dies have a thickness approximately less than 100 microns.

CLAIMS

I/We claim:

1. A method of manufacturing stacked semiconductor assemblies, comprising:

mounting a semiconductor wafer to a temporary carrier wherein the semiconductor wafer has a plurality of first dies arranged in a die pattern on the semiconductor wafer, the individual first dies having a first terminal at a first side and a through-die interconnect in contact with the first terminal and extending from the first side towards a second side of the semiconductor wafer, wherein the through-die interconnects are spaced apart from the second side of the semiconductor wafer;

thinning the semiconductor wafer to expose the through-die interconnects at the second side;

attaching a plurality of singulated second dies to corresponding first dies, wherein the second dies are arranged in the die pattern and spaced apart from each other by gaps, the individual second dies having a second terminal in contact with one of the exposed through-die interconnects;

disposing an encapsulating material in the gaps between the second dies; and

thinning the second dies after attaching the second dies to the first dies.

2. The method of claim 1 wherein thinning the second dies includes grinding a back side of the second dies.

3. The method of claim 1, further comprising cutting through the encapsulating material in the gaps and cutting the semiconductor wafer to singulate stacked microelectronic devices having a first die and a corresponding second die.

4. The method of claim 1 wherein:

before mounting the semiconductor wafer to the temporary carrier, the method further comprises forming the through-die interconnects in at least a portion of the individual first dies in electrical contact with the first terminal;

attaching the second dies to the first dies further comprises electrically coupling the second terminals of the second dies to corresponding exposed through-die interconnects.

5. The method of claim 1 wherein:

before attaching the plurality of second dies to corresponding first dies, the method further comprises testing individual first dies and individual second dies to determine known good first and second dies and known bad first and second dies; and

attaching the second dies to corresponding first dies comprises attaching known good second dies to known good first dies and attaching known bad second dies to known bad first dies to form a plurality of known good stacked devices and a plurality of known bad stacked devices.

6. The method of claim 1, further comprising:

attaching singulated third dies to corresponding second dies such that the third dies are spaced apart from each other by gaps;

disposing additional encapsulant material in the gaps between the third dies; and

removing material from a back side of the third dies after disposing the encapsulant material in the gaps between the third dies.

7. The method of claim 1 wherein the individual second dies have a handling thickness when the second dies are attached to the first dies, and thinning the second dies comprises reducing the thickness of the second dies to about 20-150 microns.

8. The method of claim 1 wherein the individual second dies have a handling thickness when the second dies are attached to the first dies, and thinning the second dies comprises reducing the thickness of the second dies to less than 100 microns.

9. The method of claim 1 wherein the semiconductor wafer has an initial thickness before thinning of approximately 700-1000 microns, and thinning the semiconductor wafer comprises reducing the thickness to approximately less than 50 microns,

wherein the individual second dies have a handling thickness greater than 150 microns when the second dies are attached to the first dies, and thinning the second dies comprises reducing the thickness of the second dies to about 20-150 microns.

10. The method of claim 1 wherein the through-die interconnects of adjacent first dies are spaced apart from one another.

11. The method of claim 1, further comprising keeping the semiconductor wafer mounted to the temporary carrier while thinning the semiconductor wafer, attaching the plurality of singulated second dies to corresponding first dies, disposing the encapsulating material in the gaps between the second dies, and thinning the second dies.

12. A method of manufacturing semiconductor workpieces, comprising:

reducing an initial thickness of a semiconductor wafer between a front side of the wafer and a back side of the wafer, wherein the semiconductor wafer has a plurality of first dies individually having a first terminal and first interconnects in contact with the first terminal and extending between the front side and the back side of the semiconductor wafer, wherein the first interconnects are spaced apart from the back side of the semiconductor wafer;

exposing the first interconnects at the back side via reducing the initial thickness of the semiconductor wafer;

mounting a plurality of separated second dies to corresponding first dies in a stacked configuration to form a plurality of stacked microelectronic devices, wherein individual second dies have second interconnects connected to second terminals on a first side of the second die and extending to an intermediate level such that the second interconnects are not exposed on a second side of the second die opposite the first side, the second terminals being in contact with one of the exposed first interconnects;

at least partially encapsulating the stacked devices; and

thinning the second dies and exposing the second interconnects on the second side after at least partially encapsulating the stacked devices.

13. The method of claim 12 wherein reducing the initial thickness of the semiconductor wafer comprises reducing the initial thickness between the front side and the back side to approximately less than 100 microns, and wherein thinning the second dies comprises reducing a second die thickness between the first and second sides to less than 300 microns.

14. The method of claim 12 wherein:

before mounting the plurality of second dies to corresponding first dies, the method further comprises testing individual first dies and individual second dies to determine known good first and second dies and known bad first and second dies; and

mounting the second dies to corresponding first dies comprises mounting known good second dies to known good first dies arranged in a stacked configuration and mounting known bad second dies to known bad first dies arranged in a stacked configuration to form a plurality of known good stacked devices and known bad stacked devices.

15. The method of claim 12 wherein thinning the second dies comprises simultaneously thinning the second dies to a thickness between the first and second sides of approximately less than 300 microns.

16. The method of claim 12 wherein:

before encapsulating the stacked devices, the method further comprises dispensing an underfill material between the second dies and the semiconductor wafer; and

thinning the second dies includes grinding the second sides of the second dies while in a stacked configuration.

17. The method of claim 13 wherein the initial thickness of the semiconductor wafer is approximately 500-1000 microns and the second die has a thickness of approximately 500-1000 microns after the mounting stage but before the thinning stage.

18. A method of manufacturing semiconductor assemblies, the method comprising:

forming first and second semiconductor wafers having front sides and back sides opposite the front sides and an array of dies at the front sides arranged in a die pattern, the individual dies including an integrated circuit and a terminal electrically coupled to the integrated circuit;

forming a plurality of interconnects in electrical contact with the die terminals on the first and second wafers;

attaching a carrier substrate to the front side of the first wafer;

processing the back side of the first wafer to form a thinned base wafer with exposed interconnect studs at the back side of the first wafer;

dividing the second wafer to form singulated second dies;

populating the first dies with singulated second dies to form an array of stacked semiconductor devices in the die pattern, the terminals on the front side of the second dies being in contact with one of the exposed interconnect studs on the first wafer, wherein the terminals on the front side of the second dies are electrically coupled with the corresponding interconnect studs of the first dies;

at least partially encapsulating the stacked devices; and

grinding the back side of the second dies after encapsulating the stacked devices.

19. The method of claim 18 wherein:

before populating the first dies with the second dies, the method further comprises testing individual first dies and second dies to determine known good first and second dies and known bad first and second dies; and

populating the first dies with second dies comprises attaching known good second dies to known good first dies arranged in a stacked configuration and attaching known bad second dies to known bad first dies arranged in a stacked configuration to form a plurality of known good stacked devices and known bad stacked devices.

20. A semiconductor assembly, comprising:

a thinned semiconductor wafer having an active side, a back side opposite the active side, and a plurality of first dies arranged in a die pattern at the active side, wherein individual first dies have an integrated circuit and first through die interconnects electrically connected to the integrated circuit, and wherein the first through die interconnects have interconnect contacts exposed at the back side of the wafer; and

a plurality of separate second dies spaced apart from each other and arranged in the die pattern relative to the thinned semiconductor wafer, individual second dies having a second active side, a second back side, a second integrated circuit, and a second terminal electrically coupled to the second integrated circuit on the second active side, wherein the individual second dies have a thickness of approximately less than 150 microns.

21. The assembly of claim 20, further comprising an underfill deposited between the first and second dies.

22. The assembly of claim 20 wherein the thickness of the plurality of second dies is substantially uniform across the thinned semiconductor wafer.

23. The assembly of claim 20 wherein the thinned semiconductor wafer has a thickness of approximately less than 100 microns.

24. The assembly of claim 20 wherein the thinned semiconductor wafer has a wafer thickness of approximately less than 50 microns and the thickness of the second die is approximately less than 50 microns.

25. The assembly of claim 20, further comprising:

a plurality of separate third dies spaced apart from each other and arranged in the die pattern relative to the thinned semiconductor wafer, individual third dies having a third active side, a third back side, a third integrated circuit, a third terminal electrically coupled to the third integrated circuit on the third active

side, wherein the third die has a thickness of approximately less than 100 microns.

26. An intermediate stacked semiconductor assembly, comprising:

a thinned semiconductor wafer having an active side, a plurality of first dies arranged in a die pattern, and first through die interconnects extending from the active side to a back side of the wafer;

a plurality of singulated second dies mounted to corresponding first dies, wherein the individual second dies are spaced apart from each other by gaps, and wherein the second dies have a first side, a second side spaced apart from the first side by a handling thickness, and a second interconnect extending from the first side to an intermediate depth in the second die such that the second interconnects are not exposed on the second side of the second dies; and

an encapsulant in the gaps.

27. The assembly of claim 26 wherein the individual second dies have a handling thickness approximately greater than 300 microns.

28. The assembly of claim 26 wherein the thinned semiconductor wafer has a final thickness approximately less than 50 microns.

29. A semiconductor assembly, comprising:

a wafer including a plurality of known good first dies and a plurality of known bad first dies;

a plurality of separated known good second dies attached to corresponding known good first dies, and a plurality of separated known bad second dies attached to corresponding known bad first dies, wherein the second dies are spaced apart from each other by gaps; and

an encapsulant material in the gaps.

30. The assembly of claim 29 wherein the wafer has a thickness approximately less than 100 microns.

31. The assembly of claim 29 wherein the separated second dies have a thickness approximately less than 100 microns.

32. The assembly of claim 29 wherein the known good first dies individually comprise a first integrated circuit electrically coupled to a first terminal and a through die interconnect, and wherein the known good second dies individually comprise a second terminal electrically coupled to a second integrated circuit and an interconnect contact point of the corresponding through die interconnect.

33. A method of manufacturing semiconductor assemblies, the method comprising:

attaching a first front side of a first semiconductor wafer to a carrier substrate, the first semiconductor wafer having an array of first dies at the first front side and arranged in a die pattern, the individual first dies having a first terminal at the first front side and a first interconnect in contact with the first terminal and extending between the first front side and a first back side of the semiconductor wafer, wherein the first interconnects are spaced apart from the first back side of the semiconductor wafer;

removing material from the first back side of the first semiconductor wafer until the first interconnects at the first back side is exposed, the first back side being opposite the first front side;

singulating a second wafer into a plurality of singulated second dies individually having a second terminal at a second front side and a second back side opposite the second front side;

stacking the singulated second dies onto the individual first dies with the second front side facing the first back side of the first semiconductor wafer with the second terminal in contact with one of the exposed first interconnects;

at least partially encapsulating the stacked first and second dies; and

removing material from the second back side of the second dies after encapsulating the stacked first and second dies to achieve a target thickness of the second dies.

34. The method of claim 33 wherein removing material from the second back side includes grinding the second back side of the second dies.

35. The method of claim 33, further comprising cutting through the encapsulating material and the first semiconductor wafer to singulate stacked microelectronic devices individually having one of the first dies and one of the corresponding second dies.

36. The method of claim 33 wherein:

stacking the singulated second dies comprises electrically coupling the second terminals at the second front side of the second dies to the corresponding first interconnect of the first dies exposed at the first back side of the first semiconductor wafer.

37. The method of claim 33, further comprising:

attaching a third front side of individual singulated third dies to the corresponding second back side of the second dies;

at least partially encapsulating the first, second, and third dies with an additional encapsulant; and

removing material from a third back side of the third dies after at least partially encapsulating the first, second, and third dies, the third back side being opposite the third front side.

38. The method of claim 33 wherein removing material from the second back side of the second dies includes removing material from the second back side of the second dies after encapsulating the stacked devices to achieve a target thickness of about 20-150 microns.

39. The method of claim 33 wherein removing material from the second back side of the second dies includes removing material from the second back side of the second dies after encapsulating the stacked devices to achieve a target thickness of about less than 100 microns.

40. The method of claim 33 wherein:

the first semiconductor wafer has a first thickness of approximately 700-1000 microns prior to removing material from the first back side of the first semiconductor wafer;

removing material from the first back side of the first semiconductor wafer includes reducing the thickness of the first semiconductor wafer to approximately less than 50 microns;

the individual second dies have a second thickness greater than 150 microns when the singulated second dies are stacked onto the individual first dies; and

removing material from the second back side of the second dies comprises reducing the second thickness

of the second dies to about 20-150 microns.