

Description

Background of the Invention

Field of the Invention

The present invention relates to a constant-voltage generation circuit which is manufactured in a standard CMOS process technology; a standard output voltage of which is determined by a bandgap voltage of transistors, and more particularly to a constant-voltage generation circuit employing operational amplifiers operated by a single power source.

Description of the Related Art

A constant-voltage generation circuit preserves its standard output voltage at a constant level, though the inputted voltage varies due to temperature variation.

A conventional constant-voltage generation circuit is well known, for example, disclosed in Japanese Patent Laid-Open Publication No. 61-217815.

The conventional circuit includes a reference voltage generation circuit and amplifiers, in which the reference voltage generation circuit is connected to power source voltage VDD and outputs reference voltages V1 and V2 by inputting standard output voltage VR of the output of the circuit.

The operational amplifiers output standard output voltage VR by differentially amplifying reference voltages V1 and V2.

The reference voltage generation circuit, which incorporates two transistors operationally controlled by standard output voltage VR and a plurality of resistors, outputs reference voltages V1 and V2 based upon the bandgap voltage of these transistors.

Two transistors and the plurality of resistors of the reference voltage generation circuit are connected to each other in such a manner that a reference voltage satisfying $V1 < V2$ or $V1 > V2$ is outputted, respectively, depending on standard voltage VR being either higher or lower.

The operational amplifiers are so constructed that the non-inverted input terminal is connected to reference voltage V1 and the inverted input terminal is connected to reference voltage V2, respectively.

The operational amplifier outputs at its output terminal standard voltage VR which is amplified in proportion to the difference voltage between the two input terminals.

It is well known as such the operational amplifiers that include either a combination of a PNP-MOS transistor and a NPN-MOS transistor or a NPN-MOS transistor and a PNP-MOS transistor.

In both cases, the operational amplifiers are connected between power source voltage VDD and negative power source voltage Vss, in which the prescri-

bed transistors differentially amplify reference voltages V1 and V2.

In the above described constant-voltage generation circuit, when standard output voltage VR increases as a result of a change in temperature, reference voltage V1 becomes lower than reference voltage V2, whereby the supply voltage to the non-inverted input terminal of the operational amplifier becomes lower than the voltage supplied to the inverted input terminal so that standard output voltage VR drops.

In this manner, the constant-voltage generation circuit compensates standard output voltage VR so as to output stabilized constant standard output voltage VR.

The constant-voltage generation circuit according to the conventional technology has the following problems set forth below to be improved.

The requirement for low power consumption restricts two transistors in the reference voltage generation circuit to be supplied with high current.

Also, the requirement for minimizing package area restricts the resistor employed in the reference voltage generation circuit to a large resistance value.

As the result, the reference voltage is set to nearly ground voltage GND.

Accordingly, since reference voltages V1 and V2 become less than a threshold voltage of the differential amplification transistor of the operational amplifier, the transistor turns off occasionally.

In order to preserve the threshold voltage of the transistor, negative power supply voltage Vss of the operational amplifier must be set lower than ground voltage GND.

For the reasons set forth above, the conventional constant-voltage generation circuit requires another negative power supply voltage Vss in addition to normal power supply voltage VDD and ground voltage GND.

US-A-4,287,439 discloses a bandgap voltage reference source with an output feedback and a voltage generation circuit. The source is temperature stable or temperature controlled and can be made by standard CMOS process.

IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE, vol. 28, February 1985, Coral Gables, Florida, USA, pages 144-145 discloses a voltage reference circuit being built around a CMOS amplifier, being constructed from a P-channel differential pair working into an N-channel current mirror at ground to allow the reference voltage to be based at ground potential.

Summary of the Invention

An object of the present invention is to provide an improved constant-voltage generation circuit which can be operated with a single power supply.

To accomplish the object, the present invention

provides a constant-voltage generating circuit as claimed in claims 1.

Further scope of applicability of the present invention will become apparent from the detailed description and specific examples, while indicated as preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

Brief Description of Drawings

These and other features and advantages of the invention may be more completely understood from the following detailed description of the preferred embodiments of the invention with reference to the accompanying drawings in which:

Fig. 1 is a circuit diagram of a constant-voltage generation circuit illustrating one embodiment of the present invention;

Fig. 2 is a circuit diagram of illustrating one embodiment of the operational amplifier shown in Fig. 1;

Fig. 3 is a circuit diagram illustrating another embodiment of the operational amplifier shown in Fig. 1.

Detailed Description of the Preferred Embodiments

Referring to the attached drawings, the preferred embodiments according to the present invention will be further explained in detail.

Fig. 1 shows a circuit diagram of a constant-voltage generation circuit illustrating one embodiment of the present invention, which comprises reference voltage generation circuit 150, standard output voltage generation circuit (operational amplifier) 160, first level shift circuit 170 and second level shift circuit 180.

Reference voltage generation circuit 150 outputs first and second reference voltages V11 and V12 based on the bandgap voltages of the first and the second transistors which control, in response to standard output voltage VR outputted from standard output voltage generation circuit 160, the current from power source voltage V_{DD} .

First level shift circuit 170 elevates first reference voltage V11 to a prescribed level (the third reference voltage) depending on the value of first reference voltage V11.

Second level shift circuit 180 elevates second reference voltage V12 to a prescribed level (the fourth reference voltage) depending on the value of second reference voltage V12.

Standard output voltage generation circuit 160 amplifies the difference voltage between the third and the fourth reference voltages to output standard

output voltage VR as the output of the constant-voltage generation circuit.

Standard output voltage VR is also outputted to reference voltage generation circuit 150 to supply negative feed-back to reference voltage generation circuit 150.

Reference voltage generation circuit 150 incorporates NPN type first transistor 151, the collector and the emitter of which are respectively connected to power source voltage VDD and resistor 153, and the base of which is connected to the base of NPN type second transistor 152.

The collector and the emitter of transistor 152 are respectively connected to power source V_{DD} and node N12 where second reference voltage appears.

Node N12 is connected via resistor 154 to ground voltage GND.

Resistor 153 is also connected to ground voltage GND via node N11 and resistor 155 where first reference voltage appears at node N11.

Transistors 151 and 152 differ from each other in emitter size.

First level shift circuit 170 comprises PMOS transistor 171 operating as a constant-current circuit for the first level shift and PMOS transistor 172 operating as a driving transistor for the first level shift.

The source, drain and gate of PMOS transistor 171 are respectively connected to power source voltage VDD, the source of PMOS transistor 172 and input terminal 170a which is used for inputting external bias voltage VB.

The drain and the gate of PMOS transistor 172 are respectively connected to ground voltage GND and node N11.

Second level shift circuit 180 comprises PMOS transistor 181 operating as a constant-current circuit for the second level shift and PMOS transistor 182 operating as a driving transistor for the second level shift.

The source, the drain and the gate of transistor 181 are respectively connected to power source VDD, the source of PMOS transistor 182 and input terminal 170a which is used for inputting external bias voltage VB.

The drain and the gate of PMOS transistor 182 are respectively connected to ground voltage GND and node N12.

Further, the source of PMOS transistor 172 is connected to non-inverted input terminal (first input terminal) 161 of the operational amplifier constituting the standard output voltage generation circuit 160.

The source of PMOS transistor 182 is connected to inverted input terminal (second input terminal) 162 of the operational amplifier.

Input terminals 161 and 162 of the operational amplifier are respectively inputted third reference voltage V13 and fourth reference voltage V14.

The output of the operational amplifier is con-

nected to the bases of transistor 151 and 152 and to output terminal 160a where standard output voltage VR is outputted.

Both PMOS transistors 171 and 181 have the same size. Also, both PMOS transistors 172 and 182 have the same size.

Fig. 2 is a circuit diagram of the operational amplifier constituting the standard output voltage generation circuit 160 shown in Fig. 1 which illustrates one embodiment of the present invention.

The operational amplifier incorporates PMOS transistors 263 and 264, the sources of each are respectively connected to power source voltage V_{DD} .

The gate of PMOS transistor 263 is connected to the gate of PMOS transistor 264 at connecting node N13 where the drains of transistor 264 and NMOS transistor 265 are respectively connected.

The drain of transistor 263 is connected to the drain of NMOS transistor 266, and the source of the transistor 266 is connected to the source of NMOS transistor 265 at connecting node N14.

The gate of transistor 266 is connected to non-inverted input terminal 161.

The gate of transistor 265 is connected to inverted input terminal 162.

The drain and the gate of NMOS transistor 267 are respectively connected to connecting node N14 and each of gates of NMOS transistors 268 and 269.

Further, each of sources of transistors 267, 268 and 269 is respectively connected to ground voltage GND.

The gate and the drain of PMOS transistor 270 are commonly connected each other and further connected to the gate and drain of transistor 269.

The gate and the drain of PMOS transistor 271 are also commonly connected each other and further connected to the source of transistor 270.

The source and the gate of PMOS transistor 272 are respectively connected to power source voltage VDD and the drains of transistor 263 and 266.

Both of the drains of transistors 263 and 266 are connected, via phase compensation resistor 273 and capacitor 274, to the drains of transistors 268 and 272.

The drains of transistors 272 and 268, which are commonly connected and constitute an output terminal of the standard output voltage generation circuit 160, are connected to output terminal 160a where the output of the constant-voltage generation circuit according to the invention is achieved.

Now, hereinafter, the operations of the constant-voltage generation circuit described above will be further explained.

The standard output voltage of the constant-voltage generation circuit is determined by the bandgap voltage of transistors.

Accordingly, first and second reference voltages V11 and V12 become low, nearly equal to ground vol-

tage GND, so that PMOS transistors 172 and 182 turn to "on".

When bias voltage VB is, on this instance, provided at input terminal 170a, the prescribed current passes, via PMOS transistor 172, from power source voltage V_{DD} to ground voltage GND, respectively, because PMOS transistors 171 and 181 stay "on".

On this instance, due to the "on" state of PMOS transistor 172, third reference voltage V13 appears at the source of transistor 172 and is also provided to non-inverted input terminal 161.

In the same way, due to the "on" state of PMOS transistor 182, fourth reference voltage V14 appears at the source of PMOS transistor 182 and is also provided to inverted input terminal 162.

Third and fourth reference voltages V13 and V14 are respectively elevated approximately to half level of power source voltage V_{DD} .

Accordingly, there is no need to prepare other power source (V_{ss}) to be connected to the operational amplifier.

In this invention, when ground voltage GND is connected to transistor 267 for supplying constant-current, transistors 265 and 266 can operate stably, whereby standard output voltage VR can be achieved from output terminal 160a.

When standard output voltage VR elevates due to, for example, variation of temperature, the current passing between collectors and emitters of transistor 151 and 152 varies in accordance with the elevated value of standard output voltage VR.

As the result, first reference voltage V11 which is lower than second reference voltage V12 and is also determined by a differential ratio of resistors 153 and 155 will appear at node 11.

Accordingly, the conductivity of PMOS transistor 172 is going greater than that of PMOS transistor 182, whereby third reference voltage V13 appears at the source of PMOS transistor 172 depending on the value of first reference voltage V11.

In the same manner, the fourth reference voltage V14 appears at the source of transistor 182 depending on the value of second reference voltage V12.

On this instance, third reference voltage V13 becomes lower than fourth reference voltage 14.

As the result, the gate voltage of transistor 265 becomes higher than the gate voltage of transistor 266 so that the gate voltage of transistor 172 elevates, which causes drop of standard output voltage VR at output terminal 160a.

In this manner, stabilized standard output voltage VR with constant voltage level can be outputted.

Fig. 3 is a circuit diagram of the operational amplifier employed in the constant-voltage generation circuit illustrating another embodiment of the present invention.

This constant-voltage generation circuit substitutes bipolar transistors for operational amplifier 160

shown in Fig. 1 and the circuit design which is nearly the same as in Fig. 2 comprises a differential amplifier stage including PNP transistors 363a and 364a, and NPN transistors 365a, 366a and 367a, an output stage constituted by PNP transistor 368a and NPN transistor 369a, phase compensation capacitor 360b for the output stage, and an internal bias circuit stage constituted by NPN transistor 370 and resistor 372.

The present invention is not limited to the foregoing embodiments illustrated since various changes and modifications can be achieved within the spirit and scope of the invention.

For example, instead of PMOS transistors 171 and 181 utilized as the constant-current circuit for the first level shift circuit resistors can be alternatively utilized.

As explained above in detail, the present invention is designed such that the first driving transistor for level shift and the first constant-current power source for level shift the first reference voltage, and the second driving transistor for level shift and the second constant-current power source for level shift the second reference voltage, whereby other power source can be eliminated except for the power source which operates the standard output voltage generation circuit.

In other words, a constant-voltage generation circuit can be realized with a single power source.

Claims

1. A constant-voltage generation circuit for outputting an output voltage signal (VR) comprising a bandgap reference voltage circuit (150) coupled to a power source (VDD) for outputting first and second reference voltage signals (V11, V12) in response to the output voltage signal (VR) and a voltage generation circuit (160) for outputting the output voltage signal (VR);
characterized by:
 - a) a first level shift circuit (170) for outputting a third reference voltage signal (V13) in response to the first reference voltage signal (V11);
 - b) a second level shift circuit (180) for outputting a fourth reference voltage signal (V14) in response to the second reference voltage signal (V12);
 - c) whereby the voltage generation circuit (160) outputs the output voltage signal (VR) by amplifying a differential voltage between a voltage level of the third reference voltage signal (V13) and a voltage level of the fourth reference voltage signal (V14).
2. The constant-voltage generation circuit in accordance with claim 1 wherein the bandgap refer-

ence voltage circuit (150) comprises: first and second bipolar transistors (151, 152) each transistor having a respective base, collector and emitter;

wherein the collectors of said first and second bipolar transistors (151, 152) are connected to the power source (VDD);

wherein the bases of said first and second bipolar transistors (151, 152) are commonly connected to each other and the output voltage signal (VR) being provided thereto;

first, second and third resistors (153, 155, 154) wherein the emitter of the first bipolar transistor (151) is connected to one end of the first resistor (153); wherein the other end of the first resistor (153) is connected to one end of said second resistor (155);

wherein the other end of the second resistor (155) is connected to one end of the third resistor (154); wherein the other end of the third resistor (154) is connected to the emitter of the second bipolar transistor (152); and

whereby the first reference voltage signal (V11) appears at one end of the second resistor (155), and the second reference voltage signal (V12) appears at the other end of the third resistor (154).

3. The constant-voltage generation circuit in accordance with claim 1 wherein the first level shift circuit (170) comprises a first constant-current source (171) and a first level shift driving circuit (172) connected to each other in series, whereby the third reference voltage signal (V13) is generated between the first level shift driving circuit (172) and the first constant-current source (171) when the first reference voltage signal (V11) is inputted to the first level shift driving circuit (172).
4. The constant-voltage generation circuit in accordance with claim 3, wherein the first constant-current source (171) and the first level shift driving circuit (172) include PMOS transistors.
5. The constant-voltage generation circuit in accordance with claim 4 wherein the PMOS transistor of the first constant-current source (171) is controlled at its base by an external bias voltage signal (VB).
6. The constant-voltage generation circuit in accordance with claim 1 wherein the second level shift circuit comprises a second constant-current source (181) and a second level shift driving circuit (182) connected to each other in series, whereby the fourth reference voltage signal (V14) is generated between the second level shift driv-

shown in Fig. 1 and the circuit design which is nearly the same as in Fig. 2 comprises a differential amplifier stage including PNP transistors 363a and 364a, and NPN transistors 365a, 366a and 367a, an output stage constituted by PNP transistor 368a and NPN transistor 369a, phase compensation capacitor 360b for the output stage, and an internal bias circuit stage constituted by NPN transistor 370 and resistor 372.

The present invention is not limited to the foregoing embodiments illustrated since various changes and modifications can be achieved within the spirit and scope of the invention.

For example, instead of PMOS transistors 171 and 181 utilized as the constant-current circuit for the first level shift circuit resistors can be alternatively utilized.

As explained above in detail, the present invention is designed such that the first driving transistor for level shift and the first constant-current power source for level shift the first reference voltage, and the second driving transistor for level shift and the second constant-current power source for level shift the second reference voltage, whereby other power source can be eliminated except for the power source which operates the standard output voltage generation circuit.

In other words, a constant-voltage generation circuit can be realized with a single power source.

Claims

1. A constant-voltage generation circuit for outputting an output voltage signal (VR) comprising a bandgap reference voltage circuit (150) coupled to a power source (VDD) for outputting first and second reference voltage signals (V11, V12) in response to the output voltage signal (VR) and a voltage generation circuit (160) for outputting the output voltage signal (VR); characterized by:
 - a) a first level shift circuit (170) for outputting a third reference voltage signal (V13) in response to the first reference voltage signal (V11);
 - b) a second level shift circuit (180) for outputting a fourth reference voltage signal (V14) in response to the second reference voltage signal (V12);
 - c) whereby the voltage generation circuit (160) outputs the output voltage signal (VR) by amplifying a differential voltage between a voltage level of the third reference voltage signal (V13) and a voltage level of the fourth reference voltage signal (V14).
2. The constant-voltage generation circuit in accordance with claim 1 wherein the bandgap refer-

ence voltage circuit (150) comprises: first and second bipolar transistors (151, 152) each transistor having a respective base, collector and emitter;

wherein the collectors of said first and second bipolar transistors (151, 152) are connected to the power source (VDD);

wherein the bases of said first and second bipolar transistors (151, 152) are commonly connected to each other and the output voltage signal (VR) being provided thereto;

first, second and third resistors (153, 155, 154) wherein the emitter of the first bipolar transistor (151) is connected to one end of the first resistor (153); wherein the other end of the first resistor (153) is connected to one end of said second resistor (155);

wherein the other end of the second resistor (155) is connected to one end of the third resistor (154); wherein the other end of the third resistor (154) is connected to the emitter of the second bipolar transistor (152); and

whereby the first reference voltage signal (V11) appears at one end of the second resistor (155), and the second reference voltage signal (V12) appears at the other end of the third resistor (154).

3. The constant-voltage generation circuit in accordance with claim 1 wherein the first level shift circuit (170) comprises a first constant-current source (171) and a first level shift driving circuit (172) connected to each other in series, whereby the third reference voltage signal (V13) is generated between the first level shift driving circuit (172) and the first constant-current source (171) when the first reference voltage signal (V11) is inputted to the first level shift driving circuit (172).
4. The constant-voltage generation circuit in accordance with claim 3, wherein the first constant-current source (171) and the first level shift driving circuit (172) include PMOS transistors.
5. The constant-voltage generation circuit in accordance with claim 4 wherein the PMOS transistor of the first constant-current source (171) is controlled at its base by an external bias voltage signal (VB).
6. The constant-voltage generation circuit in accordance with claim 1 wherein the second level shift circuit comprises a second constant-current source (181) and a second level shift driving circuit (182) connected to each other in series, whereby the fourth reference voltage signal (V14) is generated between the second level shift driv-



ing circuit (182) and the second constant-current source (181) when the second reference voltage signal (V12) is inputted to the second level shift driving circuit (182).

7. The constant-voltage generation circuit in accordance with claim 6 wherein the second constant-current source (181) and the second level shift driving circuit (182) include PMOS transistors.
8. The constant-voltage generation circuit in accordance with claim 7 wherein the PMOS transistor of the second constant-current source (181) is controlled at its base by an external bias voltage source (VB).
9. The constant-voltage generation circuit in accordance with claim 1 wherein the standard voltage generation circuit (160) includes an operational amplifier.

Patentansprüche

1. Konstantspannungs-Generatorschaltung zur Ausgabe eines Ausgangsspannungssignals (VR) mit einer Bandabstand-Bezugsspannungsschaltung (150), die mit einer Stromquelle (VDD) verbunden ist, zur Ausgabe eines ersten und zweiten Bezugsspannungssignals (V11, V12) in Reaktion auf das Ausgangsspannungssignal (VR) und mit einer Spannungs-Generatorschaltung (160) zur Ausgabe des Ausgangsspannungssignals (VR); gekennzeichnet durch:
 - a) eine erste Pegelverschiebe-Schaltung (170) zur Ausgabe eines dritten Bezugsspannungssignals (V13) in Reaktion auf das erste Bezugsspannungssignal (V11);
 - b) eine zweite Pegelverschiebe-Schaltung (180) zur Ausgabe eines vierten Bezugsspannungssignals (V14) in Reaktion auf das zweite Bezugsspannungssignal (V12);
 - c) wobei die Spannungs-Generatorschaltung (160) das Ausgangsspannungssignal (VR) durch Verstärken einer Differenzspannung zwischen einem Spannungsniveau des dritten Bezugsspannungssignals (V13) und einem Spannungsniveau des vierten Bezugsspannungssignals (V14) ausgibt.
2. Konstantspannungs-Generatorschaltung nach Anspruch 1, wobei die Bandabstand-Bezugsspannungsschaltung (150) folgendes umfaßt:
 - einen ersten und zweiten Bipolartransistor (151, 152), wobei jeder Transistor eine entsprechende Basis, einen entsprechenden Kollektor und einen entsprechenden Emmitter aufweist; wobei der Kollektor des ersten und des zweiten Bipolartransistors (151, 152) mit der Stromquelle (VDD) verbunden sind; wobei die Basis des ersten und des zweiten Bipolartransistors (151, 152) miteinander verbunden sind und das Ausgangsspannungssignal (VR) an sie geliefert wird; einen ersten, zweiten und dritten Widerstand (153, 155, 154), wobei der Emmitter des ersten Bipolartransistors (151) mit einem Ende des ersten Widerstands (153) verbunden ist; wobei das andere Ende des ersten Widerstands (153) mit einem Ende des zweiten Widerstands (155) verbunden ist; wobei das andere Ende des zweiten Widerstands (155) mit einem Ende des dritten Widerstands (154) verbunden ist; wobei das andere Ende des dritten Widerstands (154) mit dem Emmitter des zweiten Bipolartransistors (152) verbunden ist; und wobei das erste Bezugsspannungssignal (V11) an einem Ende des zweiten Widerstands (155) auftritt und das zweite Bezugsspannungssignal (V12) am anderen Ende des dritten Widerstands (154) auftritt.
3. Konstantspannungs-Generatorschaltung nach Anspruch 1, wobei die erste Pegelverschiebe-Schaltung (170) eine erste Konstantstromquelle (171) und eine erste Pegelverschiebe-Treiberschaltung (172) umfaßt, die miteinander in Reihe geschaltet sind, wobei das dritte Bezugsspannungssignal (V13) zwischen der ersten Pegelverschiebe-Treiberschaltung (172) und der ersten Konstantstromquelle (171) generiert wird, wenn das erste Bezugsspannungssignal (V11) in die erste Pegelverschiebe-Treiberschaltung (172) eingegeben wird.
4. Konstantspannungs-Generatorschaltung nach Anspruch 3, wobei die erste Konstantstromquelle (171) und die erste Pegelverschiebe-Treiberschaltung (172) PMOS-Transistoren beinhalten.
5. Konstantspannungs-Generatorschaltung nach Anspruch 4, wobei der PMOS-Transistor der ersten Konstantstromquelle (171) an seiner Basis von einem externen Vorspannungssignal (VB) gesteuert wird.
6. Konstantspannungs-Generatorschaltung nach Anspruch 1, wobei die zweite Pegelverschiebe-Schaltung eine zweite Konstantstromquelle (181) und eine zweite Pegelverschiebe-Treiberschaltung (182) umfaßt, die miteinander in Reihe geschaltet sind, wobei das vierte Bezugsspannungssignal (V14) zwischen der zweiten Pegelverschiebe-



Treiberschaltung (182) und der zweiten Konstantstromquelle (181) generiert wird, wenn das zweite Bezugsspannungssignal (V12) in die zweite Pegelverschiebe-Treiberschaltung (182) eingegeben wird.

7. Konstantspannungs-Generatorschaltung nach Anspruch 6, wobei die zweite Konstantstromquelle (181) und die zweite Pegelverschiebe-Treiberschaltung (182) PMOS-Transistoren beinhalten.
8. Konstantspannungs-Generatorschaltung nach Anspruch 7, wobei der PMOS-Transistor der zweiten Konstantstromquelle (181) an seiner Basis von einem externen Vorspannungssignal (VB) gesteuert wird.
9. Konstantspannungs-Generatorschaltung nach Anspruch 1, wobei die Standardspannungs-Generatorschaltung (160) einen Operationsverstärker beinhaltet.

Revendications

1. Circuit générateur de tension constante pour fournir un signal (VR) de tension de sortie comprenant un circuit (150) de tension de référence à barrière de potentiel couplé à une source (VDD) d'alimentation pour fournir en sortie des premier et second signaux (V11, V12) de tension de référence en réponse au signal (VR) de tension de sortie et un circuit (160) générateur de tension pour fournir en sortie le signal (VR) de tension de sortie; caractérisé par
 - a) un premier circuit (170) de décalage de niveau pour fournir en sortie un troisième signal (V13) de tension de référence en réponse au premier signal (V11) de tension de référence;
 - b) un second circuit (180) de décalage de niveau pour fournir en sortie un quatrième signal (V14) de tension de référence en réponse au second signal (V12) de tension de référence;
 - c) le circuit (160) générateur de tension fournissant en sortie le signal (VR) de tension de sortie en amplifiant une tension différentielle entre un niveau de tension du troisième signal (V13) de tension de référence et un niveau de tension du quatrième signal (V14) de tension de référence.
2. Circuit générateur de tension constante selon la revendication 1, dans lequel le circuit (150) de tension de référence à barrière de potentiel comprend: des premier et second transistors (151, 152) bipolaires, chaque transistor ayant une base, un collecteur et un émetteur respectifs; dans lequel les collecteurs desdits premier et second transistors (151, 152) bipolaires sont connectés à la source (VDD) d'alimentation; dans lequel les bases desdits premier et second transistors (151, 152) bipolaires sont connectées en commun l'une à l'autre et au signal (VR) de tension de sortie qui leur est fourni; des première, seconde et troisième résistances (153, 155, 154) dans lequel l'émetteur du premier transistor (151) bipolaire est connecté à une extrémité de la première résistance (153); dans lequel l'autre extrémité de la première résistance (153) est connectée à une extrémité de la dite seconde résistance (155); dans lequel l'autre extrémité de la seconde résistance (155) est connectée à une extrémité de la troisième résistance (154); dans lequel l'autre extrémité de la troisième résistance (154) est connectée à l'émetteur du second transistor (152) bipolaire; et le premier signal (V11) de tension de référence apparaissant à une extrémité de la seconde résistance (155), et le second signal (V12) de tension de référence apparaissant à l'autre extrémité de la troisième résistance (154).
3. Circuit générateur de tension de constante selon la revendication 1, dans lequel le premier circuit (170) de décalage de niveau comprend une première source (171) de courant constant et un premier circuit (172) d'attaque de décalage de niveau connectés l'un à l'autre en série, le troisième signal (V13) de tension de référence étant généré entre le premier circuit (172) d'attaque de décalage de niveau et la première source (171) de courant constant lorsque le premier signal (V11) de tension de référence est fourni en entrée au premier circuit (172) d'attaque de décalage de niveau.
4. Circuit générateur de tension constante selon la revendication 3, dans lequel la première source (171) de courant constant et le premier circuit (172) d'attaque de décalage de niveau comprennent des transistors PMOS.
5. Circuit générateur de tension constante selon la revendication 4, dans lequel le transistor PMOS de la première source (171) de courant constant est commandé sur sa base par un signal (VB) de tension de polarisation externe.
6. Circuit générateur de tension constante selon la revendication 1, dans lequel le second circuit de décalage de niveau comprend une seconde source (181) de courant constant et un second circuit (182) d'attaque de décalage de niveau connectés



l'un à l'autre en série, le quatrième signal (V14) de tension de référence étant généré entre le second circuit (182) d'attaque de décalage de niveau et la seconde source (181) de courant constant lorsque le second signal (V12) de tension de référence est fourni en entrée au second circuit (182) d'attaque de décalage de niveau.

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7. Circuit générateur de tension constante selon la revendication 6, dans lequel la seconde source (181) de courant constant et le second circuit (182) d'attaque de décalage de niveau comportent des transistors PMOS.

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8. Circuit générateur de tension constante selon la revendication 7, dans lequel le transistor PMOS de la seconde source (181) de courant constant est commandé sur sa base par une source (VB) de tension de polarisation externe.

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9. Circuit générateur de tension constante selon la revendication 1, dans lequel le circuit (160) générateur de tension normalisée comporte un amplificateur opérationnel.

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