CLAIMS

What is claimed is:

1. A method of forming a three dimensional memory array, comprising:

forming a stack comprising a set of conductive layers, wherein each conductive layer of the set is separated from an adjacent conductive layer of the set by a thermally insulating region, the thermally insulating region having a thermal resistance greater than that of the adjacent conductive layer;

forming a set of insulating layers within each thermally insulating region, wherein the set of insulating layers comprises at least two layers that comprise electrically insulating material;

forming a via through the stack, wherein at least a portion of the via passes through each conductive layer of the set of conductive layers;

forming a recess in at least one conductive layer of the set of conductive layers, wherein the recess is adjacent the via; and

forming a memory cell within the recess.

2. The method of claim **1**, wherein forming the set of insulating layers within each thermally insulating region comprises:

forming a first electrically insulating layer that comprises a first material; and

forming a second electrically insulating layer positioned on top of the first electrically insulating layer, wherein the second electrically insulating layer comprises a second material that is different from the first material.

3. The method of claim **1**, wherein forming the set of insulating layers within each thermally insulating region comprises:

forming a first electrically insulating layer according to a first set of formation parameters; and

forming a second electrically insulating layer according to a second set of formation parameters that is different from the first set of formation parameters, wherein the first electrically insulating layer and the second electrically insulating layer comprise a different material.

4. The method of claim **1**, wherein forming the set of insulating layers within each thermally insulating region comprises:

forming a first electrically insulating layer that comprises a first material;

forming a second layer positioned on top of the first electrically insulating layer, wherein the second layer comprises a second material different from the first material; and

forming a third layer positioned on top of the second layer, wherein the first and third layer comprise a same material.

5. The method of claim **4**, wherein the second material comprises at least one of a metal, a metal alloy, carbon, or a compound comprising silicon and nitrogen.

6. The method of claim **1**, wherein forming the stack, the set of insulating layers, and the memory cell comprises:

depositing material using one of chemical vapor deposition, metal-organic chemical vapor deposition, physical vapor deposition, or atomic layer deposition.

7. The method of claim **1**, further comprising:

forming a first conductive element on a surface of the via, wherein the first conductive element is coupled to the memory cell;

forming an intervening component on a surface of the first conductive element in the via, wherein the intervening component is coupled to the first conductive element; and

forming a second conductive element, wherein the second conductive element fills a remainder of the via and is coupled to the intervening component.

8. The method of claim **1**, further comprising:

forming an intervening material on the memory cell, wherein both the intervening material and the memory cell are formed within the recess;

forming an intervening component on a surface of the via, wherein the intervening component is coupled to the intervening material and the intervening material separates the intervening component and the memory cell; and

forming a conductive element, wherein the conductive element fills a remainder of the via and is coupled to the intervening component.

9. The method of claim **1**, further comprising:

forming a conductive element in the via, wherein the conductive element fills an entirety of the via and is coupled to the memory cell; and

forming an end component at an end of the conductive element and coupled to the conductive element, wherein the end component comprises one of a diode, a bipolar junction device, an ovonic threshold selector, a field effect transistor, or a chalcogenide material.