Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

forming a first semiconductor package by,

providing an interposer;

disposing a first semiconductor die over the interposer;

depositing a first encapsulant over the first semiconductor die and interposer,

depositing a second encapsulant over the first semiconductor die and contacting a surface of the interposer and a surface of the first encapsulant, wherein the second encapsulant covers an entirety of the surface of the first encapsulant and an entirety of the surface of the interposer, and

forming a first interconnect structure over the interposer opposite the first semiconductor die;

forming a second semiconductor package by,

providing a second semiconductor die,

disposing a modular interconnect unit completely outside a footprint of the second semiconductor die,

depositing a third encapsulant over the second semiconductor die and modular interconnect unit, and

forming a build-up interconnect structure over the second semiconductor die, modular interconnect unit, and third encapsulant; and

disposing the first semiconductor package over the second semiconductor package opposite the build-up interconnect structure, wherein the first interconnect structure of the first

semiconductor package extends to the modular interconnect unit of the second semiconductor package.

2. The method of claim 1, further including removing the second encapsulant from a top surface of the first encapsulant opposite the interposer.

3. The method of claim 1, further including removing the second encapsulant from a side surface of the first encapsulant.

4. The method of claim 1, further including disposing a vertical interconnect structure adjacent to the second semiconductor die.

5. The method of claim 1, wherein forming the first semiconductor package further includes disposing a third semiconductor die over the interposer.

6. A semiconductor device, comprising:

a first semiconductor package including,

an interposer including a top surface, a bottom surface opposite the top surface, and a side surface of the interposer that extends from the top surface to the bottom surface,

a first semiconductor die disposed on the top surface of the interposer;

a first encapsulant deposited over the first semiconductor die and interposer, wherein a side surface of the first encapsulant is coplanar with the side surface of the interposer,

a second encapsulant deposited over the first semiconductor die, interposer, and first encapsulant, wherein the second encapsulant is in direct physical contact with the side surface of the first encapsulant and the side surface of the interposer, and a bottom surface of the second encapsulant is coplanar with the bottom surface of the interposer, and

a first interconnect structure formed on the bottom surface of the interposer; and

a second semiconductor package including,

a second semiconductor die,

a modular interconnect unit disposed within a height of the second semiconductor die, wherein the modular interconnect unit and second semiconductor die are disposed side-by-side,

a third encapsulant deposited over the second semiconductor die and modular interconnect unit, wherein the third encapsulant extends between a side surface of the second semiconductor die and a side surface of the modular interconnect unit, and

a build-up interconnect structure formed on the second semiconductor die, modular interconnect unit, and third encapsulant, wherein a conductive layer of the build-up interconnect structure contacts the modular interconnect unit and the second semiconductor die;

wherein the first semiconductor package is disposed over the interposer opposite the first semiconductor die and the first interconnect structure extends from the interposer to the modular interconnect unit to electrically connect the first semiconductor die to the second semiconductor die through the modular interconnect unit and build-up interconnect structure.

7. The semiconductor device of claim 6, further including a second interconnect structure formed over the build-up interconnect structure opposite the first semiconductor package.

8. The semiconductor device of claim 6, wherein the first interconnect structure includes a plurality of dummy bumps that are electrically isolated from the first semiconductor die.

9. The semiconductor device of claim 6, further including a shielding layer formed over the first semiconductor die and first encapsulant, wherein the second encapsulant is deposited over the shielding layer.

10. The semiconductor device of claim 6, wherein the second encapsulant directly physically contacts the first encapsulant.

11. The semiconductor device of claim 6, wherein the modular interconnect unit includes a core substrate and a conductive via extending through the core substrate.

12. The semiconductor device of claim 6, wherein the third encapsulant extends between the modular interconnect unit and the interposer.

13. The semiconductor device of claim 12, wherein the first interconnect structure extends into an opening of the third encapsulant to contact the modular interconnect unit.

14. The semiconductor device of claim 6, wherein the side surface of the second semiconductor die and the side surface of the modular interconnect unit are substantially parallel and face each other.

15. The semiconductor device of claim 6, wherein the modular interconnect unit is completely outside a footprint of the second semiconductor die.

16. A semiconductor device, comprising:

a first semiconductor die;

a first encapsulant deposited over the first semiconductor die;

a second encapsulant deposited over the first semiconductor die and first encapsulant, wherein the second encapsulant is in direct physical contact with the first encapsulant;

an interconnect structure formed over the first semiconductor die, first encapsulant, and second encapsulant, wherein the interconnect structure includes a plurality of dummy bumps electrically isolated from the first semiconductor die and second semiconductor die; and

a second semiconductor die disposed over the interconnect structure opposite the first semiconductor die.

17. The semiconductor device of claim 16, further including a discrete device disposed in the first encapsulant.

18. The semiconductor device of claim 16, further including a modular interconnect unit disposed adjacent to the second semiconductor die, wherein the second semiconductor die is

electrically connected to the first semiconductor die through the interconnect structure and modular interconnect unit.

19. A semiconductor device, comprising:

a first semiconductor package including,

an interposer,

a first semiconductor die disposed over the interposer,

a first encapsulant deposited over the interposer and first semiconductor die,

a second encapsulant deposited over the first semiconductor die and contacting a surface of the first encapsulant and a surface of the interposer, wherein the second encapsulant covers an entirety of the surface of the first encapsulant and an entirety of the surface of the interposer, and

an interconnect structure formed over the interposer opposite the first semiconductor die; and

a second semiconductor package including,

a second semiconductor die,

a first modular interconnect unit disposed completely outside a footprint of the second semiconductor die, wherein the interconnect structure extends to the first modular interconnect unit,

a third encapsulant deposited over the second semiconductor die and first modular interconnect unit, and

a build-up interconnect structure formed over the second semiconductor die, first modular interconnect unit, and third encapsulant opposite the first semiconductor package.

20. The semiconductor device of claim 19, wherein the first semiconductor package further includes a discrete component disposed over the interposer adjacent the first semiconductor die.

21. The semiconductor device of claim 19, wherein the first semiconductor package further includes a third semiconductor die disposed in the first encapsulant.

22. The semiconductor device of claim 21, wherein the second semiconductor package further includes a second modular interconnect unit, wherein the first semiconductor die is coupled to the build-up interconnect structure through the interconnect structure and first modular interconnect unit and the third semiconductor die is coupled to the build-up interconnect structure through the interconnect structure and second modular interconnect unit.

23. The semiconductor device of claim 19, wherein the interconnect structure includes a plurality of dummy bumps that are electrically isolated from the first semiconductor die.

24. The semiconductor device of claim 19, wherein the build-up interconnect structure physically contacts the second semiconductor die, first modular interconnect unit, and third encapsulant.

25. The semiconductor device of claim 19, wherein a surface of the first modular interconnect unit oriented toward the first semiconductor package is coplanar with a surface of the second semiconductor die oriented toward the first semiconductor package.