precursor may adsorb onto the substrate to fully saturate the surface of the substrate such that the precursor adsorbs onto the exposed surfaces of the core material and exposed regions of the target layer. The duration for exposing the substrate to the spacer material precursor may be between about 0.1 seconds and about 2 seconds.

[0044] The spacer material precursor is selected depending on the material used for the spacer. The spacer material may be silicon oxide or germanium oxide. For silicon oxide spacers, spacer material precursor may be a silicon-containing precursor. Silicon-containing precursors suitable for use in accordance with disclosed embodiments include polysilanes ($H_3Si\text{-}(SiH_2)_n\text{-}SiH_3$), where $n \geq 0$. Examples of silanes are silane (SiH_4), disilane (Si_2H_6), and organosilanes such as methylsilane, ethylsilane, isopropylsilane, t-butylsilane, dimethylsilane, diethylsilane, di-t-butylsilane, allylsilane, *sec*-butylsilane, thexylsilane, isoamylsilane, t-butyldisilane, di-t-butyldisilane, and the like.

[0045] A halosilane includes at least one halogen group and may or may not include hydrogens and/or carbon groups. Examples of halosilanes are iodosilanes, bromosilanes, chlorosilanes and fluorosilanes. Although halosilanes, particularly fluorosilanes, may form reactive halide species that can etch silicon materials when a plasma is struck, a halosilane may not be introduced to the chamber when a plasma is struck in some embodiments, so formation of a reactive halide species from a halosilane may be mitigated. Specific chlorosilanes are tetrachlorosilane, trichlorosilane, dichlorosilane, monochlorosilane, chloroallylsilane, chloromethylsilane, dichloromethylsilane, chlorodimethylsilane, chloroethylsilane, t-butylchlorosilane, di-t-butylchlorosilane, chloroisopropylsilane, chloro-sec-butylsilane, t-butyldimethylchlorosilane, thexyldimethylchlorosilane, and the like.

[0046] An aminosilane includes at least one nitrogen atom bonded to a silicon atom, but may also contain hydrogens, oxygens, halogens, and carbons. Examples of aminosilanes are mono-, di-, tri- and tetra-aminosilane ($H_3Si(NH_2)$, $H_2Si(NH_2)_2$, $HSi(NH_2)_3$ and $Si(NH_2)_4$, respectively), as well as substituted mono-, di-, tri- and tetra-aminosilanes, for example, t-butylaminosilane, methylaminosilane, tert-butylsilanamine, bi(tertiarybutylamino)silane ($SiH_2(NHC(CH_3)_3)_2$ (BTBAS), tert-butyl silylcarbamate, $SiH(CH_3)\text{-}(N(CH_3)_2)_2$, $SiHCl\text{-}(N(CH_3)_2)_2$, $(Si(CH_3)_2NH)_3$ and the like. A further example of an aminosilane is trisilylamine ($N(SiH_3)_3$).

wafers. For example, plasmas for ALD processes may be generated by applying a radio frequency (RF) field to a gas using two capacitively coupled plates. Ionization of the gas between plates by the RF field ignites the plasma, creating free electrons in the plasma discharge region. These electrons are accelerated by the RF field and may collide with gas phase reactant molecules. Collision of these electrons with reactant molecules may form radical species that participate in the deposition process. It will be appreciated that the RF field may be coupled via any suitable electrodes. In various embodiments, a high frequency plasma is used having a frequency of at least about 13.56 MHz, or at least about 27 MHz, or at least about 40 MHz, or at least about 60 MHz. In some embodiments, a microwave-based plasma may be used. Non-limiting examples of electrodes include process gas distribution showerheads and substrate support pedestals. It will be appreciated that plasmas for ALD processes may be formed by one or more suitable methods other than capacitive coupling of an RF field to a gas. In some embodiments, the plasma is a remote plasma, such that an oxidant is ignited in a remote plasma generator upstream of the chamber, then delivered to the chamber where the substrate is housed.

[0052] In operation 312, the process chamber may be purged to remove any excess byproducts from the reaction between the spacer material precursor and the oxidant, and remove excess oxidant that did not react with the spacer material precursor on the substrate surface. The process conditions for operation 312 may be any of those described above with respect to operation 304. In some embodiments, the chamber is purged using an inert gas flowed at a flow rate between about 5 slm and about 30 slm.

[0053] In operation 314, a dopant oxide is deposited over the substrate. It will be understood that in some embodiments, spacer material may be deposited before depositing dopant oxide, while in some embodiments, dopant oxide may be deposited before depositing spacer material. Dopant oxide is deposited using any suitable technique, including but not limited to atomic layer deposition, chemical vapor deposition, sputtering, and spin on methods. The dopant oxide deposited over the substrate may be any of boron oxide, phosphorous oxide, aluminum oxide, arsenic oxide, hafnium oxide, gallium oxide, and combinations thereof. Although embodiments described herein involve boron dopants and phosphorus dopants, it will be understood that suitable precursors for depositing any of the dopant oxide may be used.

under conditions to form a sub-saturated layer of the spacer material precursor on the substrate surface. In some embodiments, the dose phase of an ALD cycle concludes before the precursor contacts the substrate to evenly saturate the surface. For example, the duration of exposure may be reduced in this operation. Typically, the precursor flow is turned off or diverted at this point, and only purge gas flows. By operating in this sub-saturation regime, the ALD process reduces the cycle time and increases throughput. However, because precursor adsorption is not saturation limited, the adsorbed precursor concentration may vary slightly across the substrate surface. Examples of ALD processes operating in the sub-saturation regime are provided in U.S. Patent Application No. 14/061,587, filed October 23, 2013, titled "SUB-SATURATED ATOMIC LAYER DEPOSITION AND CONFORMAL FILM DEPOSITION," which is incorporated herein by reference in its entirety.

[0062] The spacer material precursor selected may be any of those described above with respect to operation 302 of Figure 3.

[0063] In operation 404, the process chamber may be purged to remove excess precursor in gas phase. Operation 404 may involve any of the process conditions and purge gases described above with respect to operation 304 of Figure 3.

[0064] In operation 406, the substrate is exposed to a dopant precursor for a sub-saturated dose to adsorb dopant precursor onto the substrate surface. During this operation, the dopant may adsorb onto active sites on the substrate surface that are not occupied by spacer material precursor. After such a dose, a mostly or fully saturated layer including both spacer material precursor and dopant is on the surface of the substrate. Note that while operations 402 and 406 are discussed in sequence herein, it will be understood that in some embodiments, operation 402 may be performed prior to operation 406, and in some embodiments, operation 406 may be performed prior to operation 402.

[0065] In operation 408, the process chamber may be purged to remove excess dopant in gas phase from the chamber. Purging process conditions and purge gases may be any of those described above with respect to operation 304 of Figure 3. It will be understood that in some embodiments, purge gases and process conditions used for operation 408 may be different from that of operation 404. Further, in some embodiments, purge gases and process conditions used

doped spacer material 514 remaining on the substrate as a mask. Core material 516 is etched at an etch rate at least 5 times faster than the etch rate of the doped spacer material 514. As compared to Figure 5A, the substrate shown in Figure 5D is prepared to be used to etch the target layer 502 as a self-aligned double patterning mask whereby the pitch is reduced by half. The improved etch selectivity maintains the smooth sidewalls of the doped spacer material 514 without degrading the doped spacer material 514.

[0076] In Figure 5E, target layer 512 is etched using the doped spacer material 514 as a mask. Because the etch selectivity of core material to doped spacer material 514 is improved, the doped spacer material 514 used as a mask results in a high quality etch profile in the target layer 512.

[0077] In Figure 5F, the doped spacer material 514 is removed, leaving the etched target layer 512 on the substrate. As compared to Figure 1F, the etched target layer 512 has a good etch profile.

[0078] It will be understood that etch rate and etch selectivity of carbon-containing materials to doped spacer material may be further modulated by changing the temperature of the substrate (e.g., the temperature at which the pedestal holding the substrate is set at), increasing the plasma power, and increasing inert gas flow such as argon gas flow to further reduce the etch rate of doped spacer material. Post-deposition anneals such as described herein may also be used to reduce the etch rate.

APPARATUS

[0079] Figure 6 depicts a schematic illustration of an embodiment of an atomic layer deposition (ALD) process station 600 having a process chamber body 602 for maintaining a low-pressure environment. A plurality of ALD process stations 600 may be included in a common low pressure process tool environment. For example, Figure 7 depicts an embodiment of a multi-station processing tool 700. In some embodiments, one or more hardware parameters of ALD process station 600, including those discussed in detail below, may be adjusted programmatically by one or more computer controllers 650.

[0080] ALD process station 600 fluidly communicates with reactant delivery system 601a for delivering process gases to a distribution showerhead 606. Reactant delivery system 601a includes a mixing vessel 604 for blending and/or conditioning process gases, such as a

to one another. The Faraday shield may prevent metal or other species from depositing on the dielectric window of the plasma chamber.

[0118] Process gases (e.g. argon, fluorocarbons such as C_aF_b, etc.) may be flowed into the processing chamber through one or more main gas flow inlets 860 positioned in the upper chamber and/or through one or more side gas flow inlets 870. Likewise, though not explicitly shown, similar gas flow inlets may be used to supply process gases to a capacitively coupled plasma processing chamber. A vacuum pump, e.g., a one or two stage mechanical dry pump and/or turbomolecular pump 840, may be used to draw process gases out of the process chamber 824 and to maintain a pressure within the process chamber 824. For example, the pump may be used to evacuate the process chamber 824 during a purge operation of ALD. A valve-controlled conduit may be used to fluidically connect the vacuum pump to the processing chamber so as to selectively control application of the vacuum environment provided by the vacuum pump. This may be done employing a closed-loop-controlled flow restriction device, such as a throttle valve (not shown) or a pendulum valve (not shown), during operational plasma processing. Likewise, a vacuum pump and valve controlled fluidic connection to the capacitively coupled plasma processing chamber may also be employed.

[0119] During operation of the apparatus, one or more process gases may be supplied through the gas flow inlets 860 and/or 870. In certain embodiments, process gas may be supplied only through the main gas flow inlet 860, or only through the side gas flow inlet 870. In some cases, the gas flow inlets shown in the figure may be replaced more complex gas flow inlets, one or more showerheads, for example. The Faraday shield 849 and/or optional grid 850 may include internal channels and holes that allow delivery of process gases to the chamber. Either or both of Faraday shield 849 and optional grid 850 may serve as a showerhead for delivery of process gases. In some embodiments, a liquid vaporization and delivery system may be situated upstream of the process chamber 824, such that once a liquid reactant is vaporized, the vaporized reactant is introduced into the chamber via a gas flow inlet 860 and/or 870.

[0120] Radio frequency power is supplied from the RF power supply 841 to the coil 833 to cause an RF current to flow through the coil 833. The RF current flowing through the coil 833 generates an electromagnetic field about the coil 833. The electromagnetic field generates an

inductive current within the upper sub-chamber 802. The physical and chemical interactions of various generated ions and radicals with the wafer 819 selectively etch features of and deposit layers on the wafer.

[0121] If the plasma grid is used such that there is both an upper sub-chamber 802 and a lower sub-chamber 803, the inductive current acts on the gas present in the upper sub-chamber 802 to generate an electron-ion plasma in the upper sub-chamber 802. The optional internal plasma grid 850 limits the amount of hot electrons in the lower sub-chamber 803. In some embodiments, the apparatus is designed and operated such that the plasma present in the lower sub-chamber 803 is an ion-ion plasma.

[0122] Both the upper electron-ion plasma and the lower ion-ion plasma may contain positive and negative ions, though the ion-ion plasma will have a greater ratio of negative ions to positive ions. Volatile etching and/or deposition byproducts may be removed from the lower-sub-chamber 803 through port 822. The chuck 817 disclosed herein may operate at elevated temperatures ranging between about 10°C and about 850°C. The temperature will depend on the process operation and specific recipe.

[0123] Process chamber 824 may be coupled to facilities (not shown) when installed in a clean room or a fabrication facility. Facilities include plumbing that provide processing gases, vacuum, temperature control, and environmental particle control. These facilities are coupled to process chamber 824, when installed in the target fabrication facility. Additionally, process chamber 824 may be coupled to a transfer chamber that allows robotics to transfer semiconductor wafers into and out of process chamber 824 using typical automation.

[0124] In some embodiments, a system controller 830 (which may include one or more physical or logical controllers) controls some or all of the operations of a processing chamber. The system controller 830 may include any one or more characteristics described above with respect to computer controller 650.

[0125] Figure 9 depicts a semiconductor process cluster architecture with various modules that interface with a vacuum transfer module 938 (VTM). The arrangement of transfer modules to "transfer" wafers among multiple storage facilities and processing modules may be referred to as a "cluster tool architecture" system. Airlock 930, also known as a loadlock or transfer module, is

shown in VTM 938 with four processing modules 920a-920d, which may be individual optimized to perform various fabrication processes. By way of example, processing modules 920a-920d may be implemented to perform substrate etching, deposition, ion implantation, wafer cleaning, sputtering, and/or other semiconductor processes. In some embodiments, ALD and selective etching are performed in the same module. In some embodiments, ALD and selective etching are performed in different modules of the same tool. One or more of the substrate etching processing modules (any of 920a-920d) may be implemented as disclosed herein, i.e., for depositing conformal films, selectively depositing films by ALD, etching patterns, and other suitable functions in accordance with the disclosed embodiments. Airlock 930 and process module 920 may be referred to as "stations." Each station has a facet 936 that interfaces the station to VTM 938. Inside each facet, sensors 1-18 are used to detect the passing of wafer 926 when moved between respective stations.

[0126] Robot 922 transfers wafer 926 between stations. In one embodiment, robot 922 has one arm, and in another embodiment, robot 922 has two arms, where each arm has an end effector 924 to pick wafers such as wafer 926 for transport. Front-end robot 932, in atmospheric transfer module (ATM) 940, is used to transfer wafers 926 from cassette or Front Opening Unified Pod (FOUP) 934 in Load Port Module (LPM) 942 to airlock 930. Module center 928 inside process module 920 is one location for placing wafer 926. Aligner 944 in ATM 940 is used to align wafers.

[0127] In an exemplary processing method, a wafer is placed in one of the FOUPs 934 in the LPM 942. Front-end robot 932 transfers the wafer from the FOUP 934 to an aligner 944, which allows the wafer 926 to be properly centered before it is etched or processed. After being aligned, the wafer 926 is moved by the front-end robot 932 into an airlock 930. Because airlock modules have the ability to match the environment between an ATM and a VTM, the wafer 926 is able to move between the two pressure environments without being damaged. From the airlock module 930, the wafer 926 is moved by robot 922 through VTM 938 and into one of the process modules 920a-920d. In order to achieve this wafer movement, the robot 922 uses end effectors 924 on each of its arms. Once the wafer 926 has been processed, it is moved by robot 922 from the process modules 920a-920d to an airlock module 930. From here, the wafer 926 may be moved by the front-end robot 932 to one of the FOUPs 934 or to the aligner 944.

2. An apparatus for patterning substrates, the apparatus comprising:
   (a) one or more process chambers;
   (b) one or more gas inlets into the one or more process chambers and associated flow-control hardware;
   (c) a low frequency radio frequency (LFRF) generator;
   (d) a high frequency radio frequency (HFRF) generator; and
   (e) a controller having at least one processor and a memory, whereby
   the at least one processor and the memory are communicatively connected with one another,
   the at least one processor is at least operatively connected with the flow-control hardware, the LFRF generator, and the HFRF generator, and
   the memory stores computer-executable instructions for controlling the at least one processor to at least control the flow-control hardware, the HFRF generator, and the LFRF generator to:
      (i) deposit over a core material a doped spacer material by:
         i. introducing a first dose of a silicon-containing precursor for a duration insufficient to saturate a surface of the substrate;
         ii. introducing a second dose of a dopant precursor for a duration insufficient to saturate the surface of the substrate to form a partially saturated surface of the silicon-containing precursor and the dopant precursor on the surface of the substrate; and
         iii. introducing an oxidant to form a doped spacer material; and
      (ii) etching the patterned core material selective to the doped spacer to form a mask, wherein etch rate of the patterned core material is between about 5 and about 20 times faster than etch rate of the doped spacer to form a mask; and
      (iii) etching a target layer using the mask.

3. A method of patterning a substrate using positive patterning, the method comprising:
   (a) providing the substrate having a patterned core material;
   (b) depositing a doped spacer conformally over the patterned core material;
   (c) etching the patterned core material selective to the doped spacer to form a mask, wherein etch rate of the patterned core material is between about 5 and about 20 times faster than etch rate of the doped spacer to form a mask; and
   (d) etching a target layer using the mask.

4. The method of claim 1, wherein depositing the doped spacer comprises depositing one or more layers of silicon oxide and depositing one or more layers of a dopant oxide, the dopant selected from the group consisting of boron, gallium, phosphorous, aluminum, and arsenic.

5. The method of claim 1, wherein depositing the doped spacer comprises:
   (i) exposing the substrate to a first dose of a silicon-containing precursor for a duration insufficient to saturate a surface of the substrate;
   (ii) exposing the substrate to a second dose of a dopant precursor for a duration insufficient to saturate the surface of the substrate to form a partially saturated surface of the silicon-containing precursor and the dopant precursor on the surface of the substrate; and
   (iii)exposing the substrate to an oxidant to form a conformal doped silicon oxide material.

6. The method of claim 1, wherein the doped spacer has a dopant density between about 1E20 at/cc and about 2E22 at/cc.

7. The method of claim 1, wherein the doped spacer comprises a germanium-containing material deposited by depositing one or more layers of germanium oxide and the doped spacer is doped with phosphorous or argon.

8. The method of claim 4, further comprising after depositing the doped spacer and prior to selectively etching the patterned core material, annealing the substrate at a temperature