Fig. 1

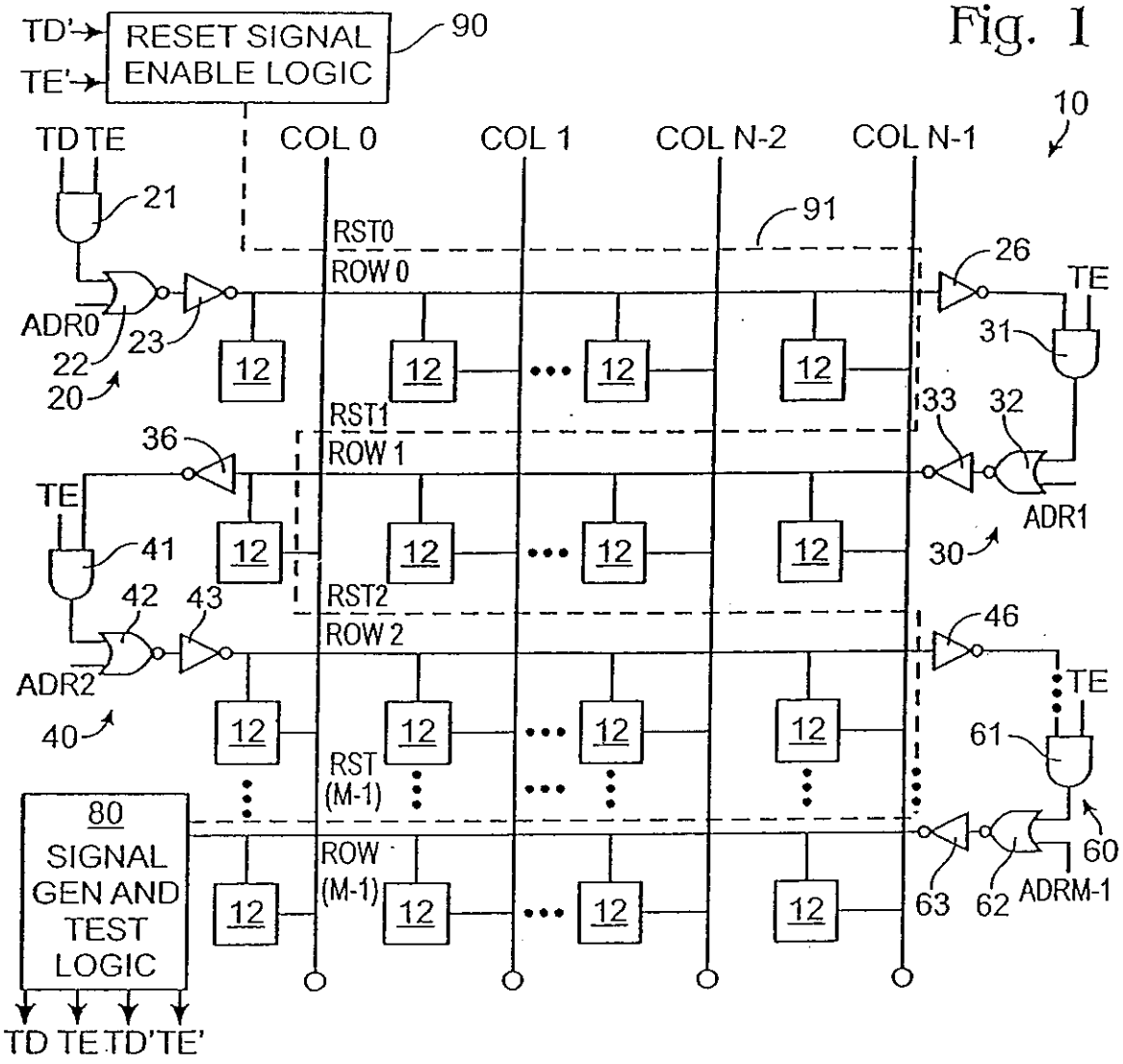

TD'
TE'
RESET SIGNAL ENABLE LOGIC
90
10
TD TE
COL 0
COL 1
COL N-2
COL N-1
21
91
RST0
ROW 0
26
TE
ADR0
22
23
20
12
31
RST1
ROW 1
33
32
36
TE
ADR1
41
30
42
43
RST2
ROW 2
46
ADR2
TE
40
61
RST (M-1)
80
SIGNAL GEN AND TEST LOGIC
ROW (M-1)
60
63
62
ADRM-1
TD TE TD'TE'

Fig. 2

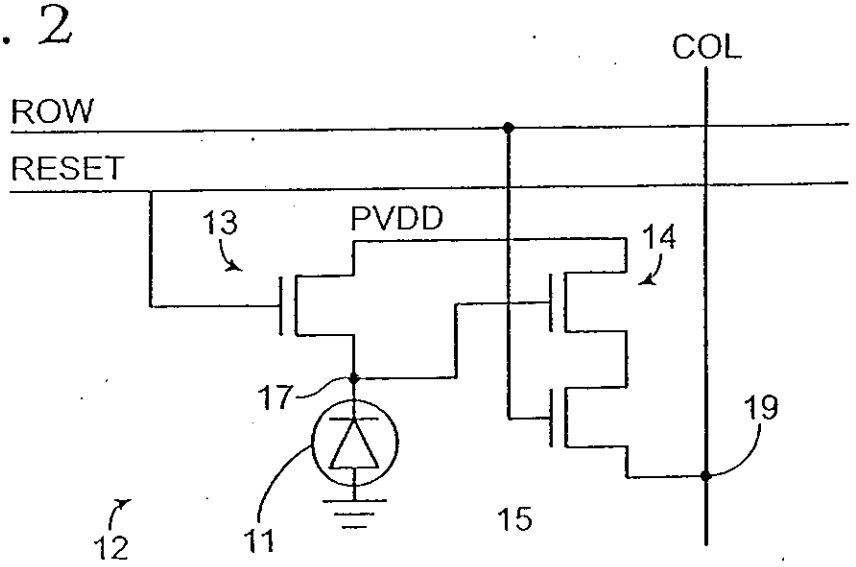

COL
ROW
RESET
13
PVDD
14
17
19
12
11
15

Fig. 3

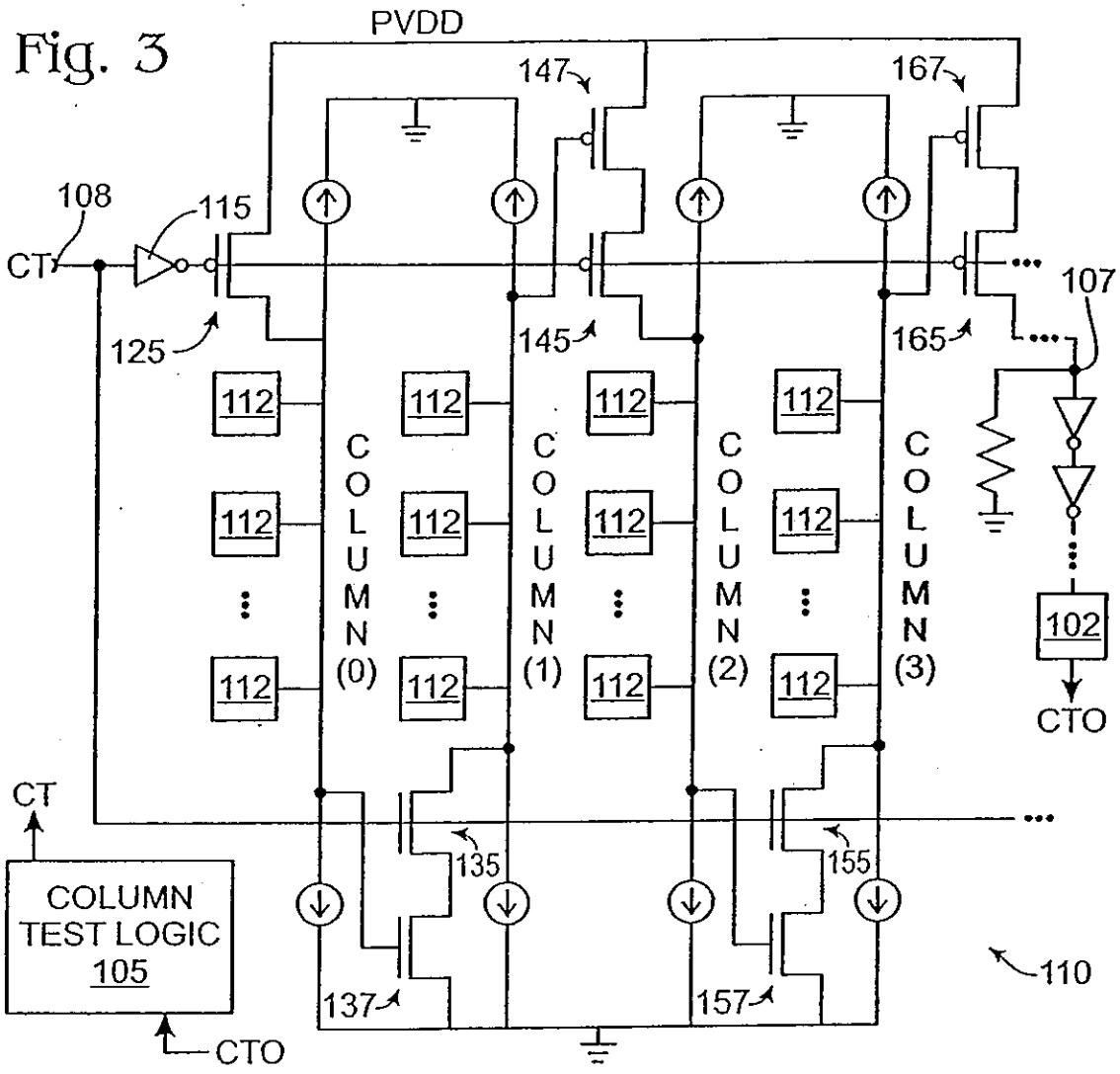
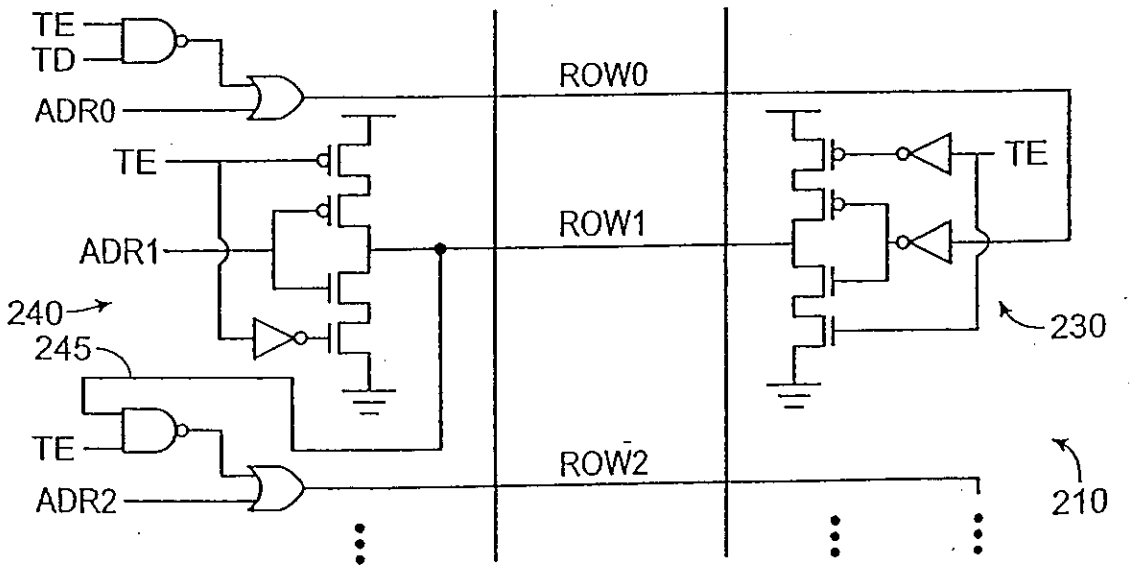

PVDD
147
167
108
115
CT
107
125
145
165
112
COLUMN (0)
COLUMN (1)
COLUMN (2)
COLUMN (3)
102
CTO
CT
135
155
COLUMN TEST LOGIC 105
110
137
157
CTO

Fig. 4


TE
TD
ADR0
ROW0
TE
ADR1
ROW1
TE
240
245
230
TE
ROW2
ADR2
210