PATENT SPECIFICATION (11) 1 536 530

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(21) Application No. 26954/77 (22) Filed 28 Jun. 1977 (19)

(31) Convention Application No. 700276 (32) Filed 28 Jun. 1976 in

(33) United States of America (US)

(44) Complete Specification Published 20 Dec. 1978

(51) INT. CL.² G11B 5/00

(52) Index at Acceptance
G4C 1D 2E 3D MO

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(54) DIGITAL MAGNETIC RECORDING CIRCUITRY

(71) We, HONEYWELL INFORMATION SYSTEMS INC., a Corporation organised and existing under the laws of the State of Delaware, United States of America, of 200 Smith Street, Waltham, Massachusetts 02154, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following Statement:–

The present invention relates generally to magnetic recording and more particularly to apparatus utilized for the recovery of data which is recorded by the double transition recording technique.

Numerous techniques have been developed for representing and recording binary information on a magnetic medium. This factor is particularly true as data processing speeds have increased and the need for higher density magnetic recording has correspondingly increased. One technique is generally referred to as double transition recording, which includes phase encoding and double frequency encoding. In double frequency encoding, clock bits and data bits alternate in a stream of information bits. The data bits can be 0's or 1's while the clock bits are usually present (i.e. 1's). In phase encoding, the polarity of each recorded transition is representative of the bit stored in a given data cell, an additional transition being required between each pair of like bits. The absence of a clock 1 bit is indicative of a change in the binary value of the succeeding data bit.

To facilitate read out of the clock and data bits it is desirable to achieve maximum separation between bits, that is, one half of a cell. The cell includes both a clock period at the beginnning thereof and a data period. However, in much high density recording systems severe shifting of the recorded clock and data bits occurs due to magnetic crowding, mechanical jitter, and effects produced by the electric circuits in the process of recording and sensing the data. This shifting of the recorded bits displaces the clock and data bits from their nominal positions in the stream of information bits and can result in erroneous decoding, that is, can result in erroneous generation of the data or clock bits or in the failure to respond to a data bit.

Various techniques exist in the prior art for detecting information which is recorded by the double transition technique. One such prior art technique utilizes a circuit for generating a constant phase reference signal synchronized to the frequency of the signal waveform representing the data. The data and reference signals are combined to produce a signal for sampling the significant transitions over the entire nominal bit period. Another such prior art technique utilizes a scheme in which a fixed time period is established for a sampling for the presence of a significant transition, wherein a ramp generator may be utilized to determine the time period. Another known prior technique utilizes a frequency tracking phase lock oscillator during read out. Continually synchronized by the read out pulses this so called fly wheel oscillator is used as a timing reference in lieu of the read out pulses themselves which are subject to instantaneous timing fluctuations. Another technique is shown in United States patent number 3,652,943, which includes a delay device in the apparatus thereof for primarily detecting the absence of information in a stream of bits.

The main object of the present invention is to provide improved apparatus for sampling data bits in a stream of information bits which have been recorded by the double transition recording technique.

According to the invention, there is provided apparatus for sampling bits following each other at nominally equal predeter-

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mined intervals of 1 period, comprising delay line means of 1½ periods length into which the bits are fed, and sampling circuitry responsive to the emergence of a 1 bit from the end of the delay line means to determine whether there is a 1 bit in the first 1 period length of the delay line means.

Read circuitry embodying the invention will now be described, by way of example, with reference tm the accompanying drawings, in which: Figure 1 is a typical stream of clock and data bits, and Figure 2 is a block diagram of the circuitry.

The read circuitry to be described operates on data encoded by what is generally termed double frequency recording. In this recording technique, data cells of fixed width are defined by a continuous stream of clock pulses, and each cell contains a data pulse for a data 1 bit or no pulse for a data 0 bit. For recording, the stream of clock and data pulses are used to generate a 2-level recording waveform which changes its level at each pulse; for reading, the signal from the read head is a reproduction (with distortion) of the recording waveform, and the polarity changes can relatively easily be converted into pulses so as to produce a pulse stream which corresponds to the pulse stream from which the recording waveform was obtained. Thus the circuitry to be described will in operation receive a pulse stream which normally consists of clock and data bits alternately, every clock bit being a 1 (pulse present) while the data bits may be 0 or 1. The interval between two successive bits, i.e. a clock bit and the following data bit (or data bit and the following clock bit) will be termed a *period*. Thus two adjacent periods between two clock bits form a *data cell*. As will become apparent, the circuitry has an internal timing source which produces pulses at 8 times the bit frequency, so each period is divided thereby into 8 *sub-periods*.

More specifically, the circuitry is designed to recognize and respond to a bit sequence which consists of an initial *gap*, a *mark* (address mark), and a *field* (data field), as shown in the Figure 1. The gap consists of a sequence of clock 1 bits with data 0 bits, there being at least 3 of each. The address mark starts with two clock 1's and two data 1's, then has an abnormal sequence of three clock 0's and three data 1's – this sequence can only be generated by special mark generating hardware, not by software. The address mark concludes with a sequence of three clock 1 bits and three data bits. This is recognized by software, but is for present purposes equivalent to the start of the data field which follows, in which all clock bits are 1's and the data bits depend on the data recorded.

Referring now to the circuitry (Fig. 2), the pulse stream described aboc is applied as the input. In broad outline, the input is fed to a timing input flip-flop TI, which feeds a first shift register SR1 which is followed by two further shift registers SR2 and SR3 which are also cross-coupled. These shift registers are each of 8 stages, and are driven by an internal timing source PDA which produces PDA pulses at sub-period intervals. These shift registers control the timing of the rest of the circuitry. The input is also fed to a separation input flip-flop SI, which feeds a clock detect flip-flop CD and a data detect flip-flop DD. These two flip-flops feed a pair of two-stage shift registers P1–P2 and Q1–Q2 as shown which in turn feed an address mark detect flip-flop MD. Shift register Q1–Q2 also feeds an AND gate 80 at which the output of the circuitry is produced, this output consisting of the data bits from the input signal.

The various components of the circuitry will now be considered in greater detail. The details of the operation will be discussed later, but it will be noted here that in operation, a pulse passes along register SR2 from stage A9 to stage A16 during each period following a data bit, and a pulse passes along register SR3 from stage A17 to stage A24 during each period following a clock bit; that is, a pulse passes from stage A17 through SR3 and then into SR2 and through to stage A16 during each data cell. Timing signals are produced as this pulse passes through various stages, e.g. stage A12.

Flip-flop SI is set by every input pulse. On the very first input pulse, i.e. the first clock bit of the gap sequence, it remains set for twelve sub-periods and then is reset; thereafter, it is reset four sub-periods after each setting. This resetting is by timing pulses A12 and A20, which are combined in OR gate 23.

Flip-flop TI is set by every input pulse; it sets stage A1 of shift register SR1, and this stage A1 feeds back to flip-flop TI through AND gate 52 to reset it almost immediately. Thus flip-flop TI serves to set each incoming pulse into shift register SR1 as a single bit in that register, that bit then travelling along SR1 during the period begun by that pulse.

Flip-flop CD is set from flip-flop SI in the middle of each period following a clock pulse, by timing signal A20 – this setting occurs before flip-flop SI is reset by the same timing pulse, due to the delay of gate 23 on pulse A20. Flip-flop CD remains set for fourteen sub-periods, and is then reset by timing pulse A18. If a clock pulse is absent at a clock bit, flip-flop CD remains reset.

Flip-flop DD is set from flip-flop SI in the middle of each period following a data pulse, by timing signal A12, provided that the data pulse was preceded by a clock pulse or that the address mark has been detected (by flip-flop MD). (Flip-flop DD is set

before the same timing pulse A12 resets flip-flop SI). It is reset six sub-periods later, by timing signal A18.

It follows that each input pulse sets flip-flop SI, and this is followed by the setting of flip-flop CD if the input pulse is a clock pulse, or of flip-flop DD if the input pulse is a data pulse (and preceded by a clock pulse). The two flip-flops CD and DD are reset together; but one sub-period before this reset, timing pulse A17 is applied to the shift registers P1–P2 and Q1–Q2 to feed the contents of these flip-flops into these two shift registers. The four stages of these shift registers feed an AND gate 76 which feeds the address mark detect flip-flop MD, which is therefore set when the first four bits (1111, clock and data bits alternately) of the address mark have been read and passed into these two shift registers. Once set, flip-flop MD can only be reset by an external signal (not shown) when the processing system receiving the output from the circuitry recognizes and signals that the data field has come to an end. Flip-flop MD enables the AND gate 80, so that once MD is set, the data bits flow from the input through flip-flops SI and DD and the shift register Q1–Q2 to the output.

The operation of the shift registers SR1 and SR3 will now be considered. Take first the situation in the gap when flip-flop MD is reset and there is a stream of clock 1 bits and data 0 bits. Each clock 1 bit in turn travels through SR1 in the period started by that bit. Sicne there are no data 1 bits, flip-flop DD remains reset, thus enabling AND gate 44 and disabling AND gate 46, and AND gate 40 is held disabled by flip-flop MD. Thus as each pulse emerges from SR1, it passes through OR gate 42 into SR2, and as it emerges one period later from SR2 is passes through AND gate 44 and OR gate 48 into SR3; another period later, it emerges from the end of SR3 and is lost. Thus the passage of a pulse from A17 to A24 and then A9 to A16 during each bit cell is established during the gap.

The events during the data field period are broadly similar, with two differences. First, since the data bits may be 1, a data pulse may enter SR1 just as a clock pulse leaves it. This data pulse will emerge from SR1 at the same time as the clock pulse emerges from SR2. Flip-flop DD will have been set by the data pulse, thus disabling gate 44 and enabling gate 46. The clock pulse from stage A16 of SR2 will therefore be prevented from entering SR3, but the data pulse from SR1 will do so instead. This data pulse will also enter SR2, but stage A17 of SR3 feeds stage A9 of SR2 as a reset input, so that the data pulse which has just entered SR2 is immediately cleared from it. Thus the circulation of a pulse in SR2 and SR3 is correctly maintained. The second difference is that if a single clock pulse should accidentally be omitted, the preceding clock pulse will have set flip-flop CD and this flip-flop will still be set when the next, missing clock pulse is due. This enables AND gate 40 (flip-flop MD also being set), so that the pulse just emerging from stage A24 of SR3 recirculates into SR2 instead of being lost.

The operation during the address mark has already been considered to some extent. The 1111 bit sequence at the start of two clock and two data bits, is treated as already described and results in the setting of the mark detect flip-flop MD. The following three clock bits are all 0's, with 1 data bits between them. As described above, each data 1 bit passes through SR1 and emerges when the clock bit is due; for a 0 clock bit, the pulse from SR1 enters SR3, emerges when the next data bit is due, anf recirculates into SR2 as CD is reset. Thus the timing is maintained during the address mark.

The circuitry is thus capable of sampling data bits and clock bits and separating such clock and data bits. The separation of clock and data bits is provided by means of flip-flop SI and the following components and the sampling is provided by means of flip-flop TI and the following components. It can be seen that such sampling will take place even though the data or clock bits are earlier or later than they would be under ideal conditions. For example, with reference to the sampling of a data 1 bit, in the ideal case, when a 1 clock bit is in position A12 the data bit is in position A4. Flip-flop SI remains set by the data bit in position A4 during the entire time that the corresponding pulse is passing through all of the positions A1 to A8 of register SR1. Flip-flop SI will not be reset until a gate delay after a pulse is received in position A12 or in position A20. Thus the data 1 bit when in position A4 under ideal circumstances will be sampled by a signal from position A12 of register SR2 to set flip-flop DD thereby sampling the data transition. If the data bit is late; for example, if the pulse from the clock bit is in position A12 and the data bit has just set flip-flop SI or has just been received in position A1; nevertheless the data transition although late by half a period will be sampled. If the data transition were early; for example, if the pulse from the data bit were in position A8 of register SR1 when the pulse from the clock bit which preceded it were in position A12; the data bit would nevertheless be sampled. As indicated herein before, the width of register SR1 is one period, i.e. the time between successive clock and data bits. Thus the register SR1 provides a timing windown of one half the data cell size. Thus the tolerance of the pre-

sent circuitry is seen to be 25% of the width of a complete data cell.

It will be realized that registers SR2 and SR3 can be replaced by a single 8-stage shift register together with a flip-flop to indicate which half or period of a data cell is occupied, together with suitable further gating circuitry. Thus instead of a pulse passing through SR2 and SR3 alternately, it could pass repeatedly along a single 8-stage shift register with a flip-flop being set and reset for alternate passes.

WHAT WE CLAIM IS:–

1. Apparatus for sampling bits following each other at nominally equal predetermined intervals of 1 period, comprising delay line means of 1½ periods length into which the bits are fed, and sampling circuitry responsive to the emergence of a 1 bit from the end of the delay line means to determine whether there is a 1 bit in the first 1 period length of the delay line means.

2. Apparatus according to claim 1 wherein the sampling circuitry includes a flip-flop which is set by each 1 input bit and is reset by each 1 bit to emerge from the end of the delay line means, and means for determining whether such resetting is from the set state.

3. Apparatus according to either previous claim wherein the sampling circuitry feeds mark detect circuitry which detects a predetermined sequence of bits and an AND gate enabled by the mark detect circuitry.

4. Apparatus according to any previous claim wherein the delay line means comprises a first delay line of 1 period length and a further delay line means comprising the remaining ½ period length and at least a further ½ period length, and means for maintaining a 1 bit pulse circulating continuously through the further delay line means.

5. Apparatus according to claim 4 wherein the further delay line means comprise second and third delay lines each of 1 period length, and the coupling means can couple the end of the first delay line to the beginnings of the second and third and the ends of the second and third to the beginnings of the third and second respectively.

6. Apparatus according to any previous claim wherein the delay line means comprise shift register means, and there is an oscillator operating at a frequency of a multiple of the inverse of said period to drive the shift register means.

7. Apparatus for sampling bits following each other at nominally equal predetermined intervals, substantially as hereinbefore described with reference to the accompanying drawings.

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Printed for Her Majesty's Stationery Office, by Croydon Printing Company Limited, Croydon, Surrey, 1978.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

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