

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN WORD LINE DRIVER CIRCUIT IN MEMORY CIRCUIT

- (71) We, HITACHI LIMITED of 1-5-1 Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—
- 10 The present invention relates to memory circuits and, more particularly, to word line driver circuits which are connected to the output terminals of decoder circuits therefor.
- For driving a word line in an array of memory cells, which are selectively addressed by decoder circuits, two types of driver circuits are well known.
- A first type is a push-pull buffer, shown in Figure 1 of the accompanying drawings.
- 20 The word line driver circuit 5 which is connected between a decoder circuit 1 and an array of memory cells 4 is shown within broken lines. The driver circuit 5 includes a pair of MOSFETs 2 and 3 connected between a potential of $-V_{DD}$ volts and earth. The output of the decoder circuit 5 is applied directly and through an inverter 6 respectively to the gate electrodes of the MOSFETs 2 and 3.
- 30 In this arrangement, if the potential at the output of the decoder circuit 1 is such that the MOSFET 2 is turned on, (i.e. a gating potential is applied) then the MOSFET 3 is turned off because of the action of the inverter 6. In this case, the potential at the drain electrode of the MOSFET 2 ($-V_{DD}$) is applied to the word line 7, which is connected to the memory cell array 4.
- On the other hand, if the potential at the output of the decoder circuit 1 is such that the MOSFET 2 is turned off (0 volts) (i.e. a gating potential is absent) the MOSFET 3 is turned on because of the action of the inverter 6. In this case, the common reference potential (earth) is applied to the

word line 7, thereby preventing the word line driver circuit 5 from floating.

However, with this type of arrangement, an inverter circuit, which serves no function other than to provide an inverted signal, is required, and the operation of the MOSFET 3 is dependent upon the output of the decoder circuit 1. As a result, the integration density of the overall memory circuit suffers.

Another well known word line driver circuit arrangement employs a pair of MOSFETs with a chip-enable signal, and an inverted chip-enable signal supplied to both MOSFETs. Such a circuit is illustrated on page 6 of the publication "Silicon Gate MOS LSI RAM 1103" published by Intel Corporation, 1971. Also, this type of circuit is described in the manual "Semiconductor Memories", Bulletin CW-806, Videotape Course Workbook, by Texas Instruments Incorporated, 1972, particularly between pages 5-17.

This circuit is shown in Figure 2 of the accompanying drawings, wherein, as in the circuit of Figure 1, a pair of MOSFETs 2 and 3 are connected between a decoder circuit 1 and a memory cell array 4. However, in this arrangement, the MOSFET 2, rather than having a fixed potential $-V_{DD}$ has a control signal CE (chip-enable) applied to its drain electrode whilst an inverted chip-

enable signal $\overline{CE}$ is applied to the gate electrode of the MOSFET 3. These signals are supplied simultaneously to the word driver circuit 5 for selectively turning the MOSFET 2 on whilst the MOSFET 3 is turned off, and vice versa. The advantage of this circuit over the circuit of Figure 1 is that the integration density can be improved by elimination of the inverter circuit 6.

However, the memory cell array 4, in the arrangement of Figure 2, is subject to misoperation if the word line 7, which has not been selected by the decoder circuit, floats,

and thus picks up noise sufficient in magnitude to select a memory cell. That is to say, in the absence of a gating potential at the output of the decoder circuit 1,

5 MOSFET 2 is turned off and, accordingly,

if the input $\overline{CE}$ to the MOSFET 3 is inverted, i.e. the MOSFET 3 is not turned on, the word line 7 connected to the memory cell array 4 floats.

10 When the potential of the floating word line 7 reaches or exceeds the level of the address signal required for accessing a memory cell due to noise, a gate of one of the circuits within the memory cell may be rendered conductive, thereby causing misoperation of the circuit, and an undesired memory cell to be addressed.

Accordingly, whilst the circuit of Figure 2 may improve the density of integration of the memory circuit proper, it is subject to misoperation.

20 It is an object of the present invention to provide an improved memory circuit, which permits an increase in the density of integration, and does not suffer from misoperation due to noise.

According to the present invention there is provided a memory circuit including: at least one memory cell for storing information; a first circuit for supplying memory cell selection signals for accessing a memory cell; and means for applying an address signal for controlling said at least one memory cell; and a source follower type driver circuit for selectively gating said address signal to said at least one memory cell in response to said selection signal, said driver circuit comprising: a first field effect transistor of the enhancement type having its gate electrode connected to said first circuit, its source electrode connected to said at least one memory cell, and its drain electrode connected to said means for apply said address signal; and a second field effect transistor having its gate and source electrodes connected to respective sources of reference potential and its drain electrode connected to the source electrode of the first transistor, thereby preventing the potential of the connection point between the two transistors from floating at least when said first field effect transistor is turned off.

The present invention will now be described in greater detail, by way of example, with reference to the remaining figures of the accompanying drawings, wherein:—

Figure 3 is a circuit diagram of a memory circuit incorporating a preferred form of drive circuit;

60 Figure 4 is a detailed circuit diagram of a memory circuit array for use in explaining the operation of the decoder circuit, and the memory circuit employing the novel driver circuit; and

65 Figure 5 is a circuit diagram of a second

embodiment of a driver circuit for use with a memory circuit.

Referring to Figure 3, the memory driver circuit 5, which is connected between the decoder circuit 1 and the memory cell array 4, includes a pair of MOSFETs 12 and 13. The MOSFET 12 is an enhancement P-type, and the drain electrode thereof is connected to a memory cell address voltage or control signal CE. The gate electrode of the MOSFET 12 is connected to the output of the decoder circuit 1, and the source electrode thereof is connected to the word line 7, which is connected both to the memory cell array 4 and to the drain electrode of the MOSFET 13. The MOSFET 13 is a depletion P-type which acts as a load resistance, the source electrode of which is connected to earth, and also to the gate electrode thereof.

In operation, if the decoder circuit 1 applies a gating potential for accessing the memory cells 4 connected to the word line 7 of the driver circuit 5, the MOSFET 12 is turned on, thereby coupling the control signal CE to the word line 7. The MOSFET 13 is permanently turned on because of the connection of its gate electrode to earth potential, and acts as a load resistance between the word line 7 and earth. The potential applied to the word line 7 is determined by the ratio of the 'on' resistance of the MOSFET 12, and the permanent load resistance provided by the MOSFET 13. The on-resistance of the MOSFET 12 is about 60 ohms, whilst the load resistance of the MOSFET 13 is about 4 Kohms. Thus, whilst the MOSFETs 12 and 13 act as a voltage divider for the control signal CE, due to the larger load resistance provided by the MOSFET 13, the potential on the word line 7 due to the control signal CE is sufficient to energize the memory cells 4, selectively addressed by the decoder circuit 1 through the driver circuit 5.

On the other hand, when the decoder circuit 1 provides no output, therefore preventing the MOSFET 12 from being turned on, then relative to the MOSFET 13, the MOSFET 12 is essentially an open circuit, so that the word line 7 is effectively connected to earth. By virtue of the MOSFET 13 being permanently turned on, if an electric charge due to noise, etc. tends to charge the floating gate capacitance of the word line, which word line has not been selected because there is no gating output from the decoder circuit, this electric charge is prevented from building up and leaks to earth through the turned-on depletion MOSFET 13, thereby preventing the memory cells 4 from being misaddressed.

Referring to Figure 4, the decoder circuit 30 of row 1 of the overall memory circuit array comprises MOSFETs 14 to 19. The

MOSFETs 15 to 18 are enhancement P-type, and are connected in parallel with each other. The respective gate electrodes A0 to A3 thereof are connected to receive address signals. The MOSFET 14 is a depletion P-type, and has its source electrode connected to the commonly connected drains of the MOSFETs 15 to 18 and to the gate electrode of a MOSFET 20 included within a driver circuit 40. Similarly, the drain electrode of the enhancement P-type MOSFET 19 is connected to the commonly connected source electrodes of the MOSFETs 15 to 18 and the source electrode of the MOSFET 19 is connected to earth. The drain electrode of the MOSFET 14 is connected to a voltage source $-VDD$ (-10 volts) and the gate electrode thereof is connected to the gate electrode of the MOSFET 20. The gate electrode of the MOSFET 19 is supplied with a pulse signal $\bar{P}$.

The word line driver circuit 40 comprises the enhancement P-type MOSFET 20 and a depletion P-type MOSFET 21 connected in series as shown in Figure 3. The common connection of the MOSFETs 20 and 21 is connected to a word line 24, which drives row 1 of memory cells 50, the word line 24 being connected to the gate electrodes of the MOSFETs 22 and 23 in each respective cell. Information is written into or read out from the respective memory cells when the MOSFETs 22 and 23 are addressed and, thereby, turned on. For each row, a respective decoder and word line driver circuit are used.

In operation, assuming that row 1 has been selected, the gate electrode of each of the MOSFETs 15 to 18 is supplied with an address input, so as to turn off each of these MOSFETs. Whilst each of the MOSFETs 15 to 18 is supplied with an address input, so as to turn off each of these MOSFETs, whilst each of the MOSFETs 15 to 18 is turned off, the voltage applied to the drain electrode of the MOSFET 14 ($-VDD$) is applied to the output terminal of the decoder circuit 30 of row 1. As a result, the MOSFET 20 is turned on, thereby coupling a control signal CE of -10 volts to the drain electrode of the MOSFET 20. In turn, the word line 24 receives an appropriate fraction of the -10 volts, because of the voltage dividing effect provided by the resistances of the turned on MOSFET 20, and the permanently turned on MOSFET 21, and applies this fraction to the gate electrodes of the MOSFET 22 and 23, thereby selectively addressing the memory cells 50 of row 1.

On the other hand, if row 1 is not selected, for example, when MOSFET 15 is turned on whilst an inverted pulse signal $\bar{P}$ of -10 volts is applied to the gate electrode of the

MOSFET 19, then the output of the decoder circuit 30 falls to earth potential through the MOSFETs 15 and 19. As a result, the MOSFET 20 is turned off, therefore the potential of the control signal input CE is not applied to the word line 24.

Since the MOSFET 21 is permanently turned on, the potential of the word line 24 is substantially earth, thereby causing the MOSFETs 22 and 23 to be turned off.

Thus, since the word line 24 cannot float, misoperation of the cells 50 is prevented.

In the embodiment described in Figure 3, each of the MOSFETs 12 and 13 is of the P-type. However, N-type MOSFETs may be employed with appropriate voltage polarities reversed.

Furthermore, referring to Figure 5, in place of a depletion P-type MOSFET 13, used in the circuit shown in Figure 3, an enhancement P-type MOSFET 13' may be used as the load resistance. However, the gate electrode thereof is not connected in common with the source electrode to earth, but is connected to a voltage supply of $-VGG$ volts, so that the MOSFET 13' will be permanently turned on.

WHAT WE CLAIM IS:—

1. A memory circuit including: at least one memory cell for storing information; a first circuit for supplying memory cell selection signals for accessing a memory cell; and means for applying an address signal for controlling said at least one memory cell; and a source follower type driver circuit for selectively gating said address signal to said at least one memory cell in response to said selection signal, said driver circuit comprising: a first field effect transistor of the enhancement type having its gate electrode connected to said first circuit, its source electrode connected to said at least one memory cell, and its drain electrode connected said means for applying said address signal; and a second field effect transistor having its gate and source electrodes connected to respective sources of reference potential and its drain electrode connected to the source electrode of the first transistor, thereby preventing the potential of the connection point between the two transistors from floating at least when said first field effect transistor is turned off.

2. A memory circuit according to Claim 1, wherein said second field effect transistor is of the depletion P-type, and said first and second sources of reference potential are the same source of reference potential.

3. A memory circuit according to Claim 2, wherein said same source of reference potential is earth.

4. A memory circuit according to Claim 1, wherein said second field effect transistor is of the enhancement P-type, and said first source of reference potential is earth, and said second source of reference potential is a



MOSFETs 15 to 18 are enhancement P-type, and are connected in parallel with each other. The respective gate electrodes A0 to A3 thereof are connected to receive address signals. The MOSFET 14 is a depletion P-type, and has its source electrode connected to the commonly connected drains of the MOSFETs 15 to 18 and to the gate electrode of a MOSFET 20 included within a driver circuit 40. Similarly, the drain electrode of the enhancement P-type MOSFET 19 is connected to the commonly connected source electrodes of the MOSFETs 15 to 18 and the source electrode of the MOSFET 19 is connected to earth. The drain electrode of the MOSFET 14 is connected to a voltage source $-VDD$ (-10 volts) and the gate electrode thereof is connected to the gate electrode of the MOSFET 20. The gate electrode of the MOSFET 19 is supplied with a pulse signal $\bar{P}$.

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2. A memory circuit according to Claim 1, wherein said second field effect transistor is of the depletion P-type, and said first and second sources of reference potential are the same source of reference potential.

3. A memory circuit according to Claim 2, wherein said same source of reference potential is earth.

4. A memory circuit according to Claim 1, wherein said second field effect transistor is of the enhancement P-type, and said first source of reference potential is earth, and said second source of reference potential is a

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negative potential.

5. A memory circuit constructed and arranged to operate substantially as herein described, with reference to and as illustrated in Figure 3 or Figure 4 or Figure 5 of the accompanying drawings.

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