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(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR MEMORY APPARATUS

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195 Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor memory apparatus.

In computers and related applications there is a need for large information capacity semiconductor memories in which information can be temporarily stored and read out within a useful period of time. To meet such requirements, it is necessary that each basic memory cell be of a sufficiently simple structure to permit a relatively large number to be fabricated and interconnected on a single monolithic integrated circuit chip.

Hitherto, memory cells have used charge storage diodes for retaining information bits. One serious disadvantage of such memory cells is that the maximum storage time is limited to the minority carrier lifetime of the diodes used. Another disadvantage is that, as the physical size of the diodes and the write current used decreases, the magnitude of the stored charge which serves as the output signal decreases, thereby necessitating sensitive amplifiers to detect the small current differences between a stored "1" and "0".

Copending application no. 47391/70 (serial no. 1323577) describes how the storage time can be extended through the use of two serially connected diodes which have different minority carrier lifetimes.

U.S. patent no. 3675025 describes a light activated memory cell which utilizes a single transistor having an uncontacted photosensitive base. Signal light received over a period

of time on the photosensitive base causes a build up of charge on the base which flows into the emitter-base junction when the transistor is turned on and gives rise to a collector current that is beta times the light signal created base current. This amplification of the output signal is very desirable; however, in many applications it is not practical to use any other input signal than an electrical one that is physically connected to the cell.

One solution to this problem is the use of a transistor having a contacted base, collector, and emitter. This solution works well for a single cell but is impractical to implement in a large memory because the making of three electrical contacts to each memory cell unduly increases the size of the integrated circuit chip and the complexity of the fabrication process.

According to a first aspect of this invention semiconductor memory apparatus comprises a plurality of memory cells, each of which comprises an NPN junction transistor having an uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, first means for selectively changing a stored "0" to a "1" in said cells comprising means for increasing the collector potential of the transistor of the or each selected cell from an initial value to a value sufficient to bias the collector-base junction to avalanche breakdown and to increase the base potential sufficiently to forward-bias the emitter-base junction, thereby causing transistor conduction, and for the decreasing the collector potential to its initial value, whereby transistor conduction is terminated leaving holes trapped within the transistor, whereupon the base returns to a different, "1", potential, and second means for reading out stored information. The second means may comprise a conduction detector circuit for coupling to the emitter of the

transistor of the or each cell whose information is to be read out, and means for increasing the collector potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in that cell, and for then lowering the collector potential to its initial value, whereby the base assumes its "0" potential, and there may be provided a plurality of conduction paths for coupling said memory cells to said first and second means.

According to a second aspect of this invention semiconductor memory apparatus comprises a plurality of memory cells, each of which comprises a PNP junction transistor having an uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, first means for selectively changing a stored "0" to a "1" in said cells comprising means for decreasing the collector potential of the transistor of the or each selected cell from an initial value to a value sufficient to bias the collector-base junction to avalanche breakdown and to decrease the base potential sufficiently to forward-bias the emitter-base junction, thereby causing transistor conduction, and for then increasing the collector potential to its initial value, whereby transistor conduction is terminated leaving electrons trapped within the transistor, whereupon the base returns to a different, "1", potential, and second means for reading out stored information. The second means may comprise a conduction detector circuit for coupling to the emitter of the transistor of the or each cell whose information is to be read out, and means for decreasing the collector potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in the cell, and for then increasing the collector potential to its initial value, whereby the base assumes its "0" potential, and there may be provided a plurality of conduction paths for coupling said memory cells to said first and second means.

According to a third aspect of this invention semiconductor memory apparatus comprises a plurality of memory cells, each of which comprises an NPN junction transistor having an uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, first means for selectively changing a stored "0" to a "1" in said cells comprising means for decreasing the collector potential of the transistor of the or each selected cell from an initial value to a value that causes the collector-base junction to be forward-biased and the base potential to decrease in potential toward a potential greater than that necessary

to bias the emitter-base junction to avalanche breakdown, thereby causing the emitter-base junction to operate in avalanche breakdown and preventing the base potential from decreasing further, and for then increasing the collector potential to its initial value, whereupon the base assumes a different, "1", potential, and second means for reading out stored information. The second means may comprise a conduction detector circuit for coupling to the emitter of the transistor of the or each cell whose information is to be read out, and means for increasing the collector potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in the cell, and for then decreasing the collector potential to its initial value, whereby the base assumes its "0" potential, and there may be provided a plurality of conduction paths for coupling said memory cells to said first and second means.

According to a fourth aspect of this invention semiconductor memory apparatus comprises a plurality of memory cells, each of which comprises a PNP junction transistor having an uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, first means for selectively changing a stored "0" to a stored "1" in said cells comprising means for increasing the collector potential of the transistor of the or each selected cell from an initial value to a value that causes the collector-base junction to be forward-biased and the base potential to increase in potential toward a potential greater than that necessary to bias the emitter-base junction to avalanche breakdown, thereby causing the emitter-base junction to operate in avalanche breakdown and preventing the base potential from increasing further, and for then decreasing the collector potential to its initial value, whereupon the base assumes a different, "1", potential, and second means for reading out stored information. The second means may comprise a conduction detector circuit for coupling to the emitter of the transistor of the or each cell whose information is to be read out, and means for decreasing the collector potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in the cell, and for then increasing the collector potential to its initial value, whereby the base assumes its "0" potential, and there may be provided a plurality of conduction paths for coupling said memory cells to said first and second means.

According to a fifth aspect of this invention semiconductor memory apparatus comprises a plurality of NPN memory cells, each

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of which comprises a junction transistor having two electrically isolated emitters, an uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, and a resistor connected between the first emitter and the collector, first means for selectively changing a stored "0" to a "1" in said cells comprising means for adjusting each emitter potential of the transistor of the or each selected cell from an initial value to a value sufficient to bias the first emitter-base junction to avalanche breakdown and to increase the base potential sufficiently to forward-bias the collector-base junction and the second emitter-base junction, thereby causing the transistor to conduct in saturation, and for then returning each emitter potential to its initial value, whereby transistor conduction is terminated leaving holes trapped within the transistor, whereupon the base returns to a different, "1", potential, and second means for reading out stored information. The second means may comprise a conduction detector circuit for coupling to the second emitter of the transistor of the or each cell whose information is to be read out, and means for increasing the first emitter potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in the cell, and for then decreasing the emitter potential to its initial value, whereby the base assumes its "0" potential, and there may be provided a plurality of conduction paths for coupling said memory cells to said first and second means.

According to a sixth aspect of this invention semiconductor memory apparatus comprises a plurality of PNP memory cells, each of which comprises a junction transistor having two electrically isolated emitters, an uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, and a resistor connected between the first emitter and the collector, first means for selectively changing a stored "0" to a "1" in said cells comprising means for adjusting each emitter potential of the transistor of the or each selected cell from an initial value to a value sufficient to bias the first emitter-base junction to avalanche breakdown and to decrease the base potential sufficiently to forward-bias the collector-base junction and the second emitter-base junction, thereby causing the transistor to conduct in saturation, and for then returning each emitter potential to its initial value, whereby transistor conduction is terminated leaving electrons trapped within the transistor, whereupon the base returns to a different, "1", potential, and second means for reading out stored information. The second means may

comprise a conduction detector circuit for coupling to the second emitter of the transistor of the or each cell whose information is to be read out, and means for decreasing the first emitter potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in the cell, and for then increasing the emitter potential to its initial value, whereby the base assumes its "0" potential, and there may be provided a plurality of conduction paths for coupling said memory cells to said first and second means.

The invention will now be described with reference to the accompanying drawings in which:

Fig. 1 is a schematic diagram of a two-terminal NPN transistor memory cell;

Fig. 2 illustrates a memory apparatus in accordance with the invention using a plurality of such memory cells;

Fig. 3 illustrates another memory apparatus in accordance with the invention using PNP transistor memory cells;

Fig. 4 is a schematic diagram of another two-terminal NPN transistor memory cell;

Fig. 5 illustrates a memory apparatus in accordance with the invention using a plurality of such other cells; and

Fig. 6 illustrates another memory apparatus in accordance with the invention using PNP transistor memory cells.

Referring now to Fig. 1, an NPN transistor 10 includes a collector terminal 12, an emitter terminal 14, and an uncontacted base 16. A circuit 18 is connected to emitter terminal 14 and acts as a conduction detector and a low impedance path to ground potential. A voltage pulse circuit 20 is connected to the collector terminal 12. The capacitances C_{BO} and C_{BE} associated with the collector-base junction and the base-emitter junction, respectively, are shown external to the transistor in order to simplify the description of the mode of operation which appears below. These capacitances serve as low impedance ac paths between the collector, base, and emitter.

The potential of the base 16 floats and is electrically set to one of two values, which represent, respectively, the storage of a "1" and "0" in the cell, by applying a positive polarity voltage pulse to the collector terminal 12.

In operation, to write a "1" on a base containing a "0", an approximately ground based write voltage pulse having a positive polarity is applied to the collector terminal 12 by the voltage pulse circuit 20. The leading edge of the write pulse causes the base potential to rise with respect to the emitter terminal potential, such that the emitter-base junction becomes forward-biased and limits any further increase in the base potential. As

the leading edge of the write pulse reaches its maximum amplitude, the collector-base junction is biased to avalanche breakdown and acts as a low impedance path between the collector terminal and the uncontacted base. The base can now receive current from the voltage pulse source via the broken-down collector-base junction. Transistor conduction occurs since there is a source of base current and the emitter-base junction is forward-biased.

The trailing edge of the write pulse rapidly cuts off the avalanche breakdown operation of the collector-base junction, thereby cutting off the supply of the base current and therefore rapidly terminating transistor conduction.

The rapid termination of transistor conduction causes an equal number of electrons and holes to be temporarily trapped within the transistor. The electrons, being majority carriers in the N-type semiconductor collector, traverse the collector at approximately the speed of light and exit the transistor via the collector contact into the voltage pulse circuit. The holes, being minority carriers in the N-type semiconductor emitter, are unable to quickly traverse the emitter and exit the transistor via the emitter terminal into the conduction detector circuit. They must first recombine with electrons in order to effectively exit the transistor. Some holes are able to exit the transistor due to leakage. The effective lifetime of the holes existing in the transistor after conduction ceases is a function of the recombination and leakage rates.

The trailing edge of the write pulse, in addition to terminating transistor conduction, causes the base potential to fall toward the "0" or to a more negative potential. The decrease in base potential is partially negated by the flow of holes into the base that cause it to assume a potential more positive than the "0" potential. This resulting potential is defined as the "1" potential.

It is necessary for the fall time of the trailing edge of the write pulse to be equal to or less than the effective lifetime of the holes in order for them to be effective in negating the effect of the trailing edge of the write pulse on the base potential. In a preferred embodiment, the effective lifetime of the holes is approximately 50 nanoseconds and the fall time of the trailing edge of the write pulse is approximately 10 nanoseconds.

In order to detect the base potential and thereby determine the stored information in the cell, an approximately ground based read voltage pulse of positive polarity and insufficient amplitude to bias the collector-base junction to avalanche breakdown is applied to the collector terminal by the voltage pulse circuit. The leading edge of the read pulse causes the base potential to rise sufficiently with respect to the emitter terminal potential to forward-bias the emitter-base junction

sufficiently to allow transistor conduction if, and only if, the base was previously at the "1" potential. Transient transistor conduction upon the application of a read pulse to the memory cell is interpreted as a "1", whereas nontransistor conduction is interpreted as a "0".

The pulse width of the read pulse is such that transient transistor conduction, which occurs if the cell was previously at the "1" potential, ceases prior to the start of the trailing edge of the read pulse. Upon termination of the transient transistor conduction, the emitter-base junction is left forward-biased, but not sufficiently to permit conduction. The trailing edge of the read pulse then lowers the base potential to the "0" potential. Therefore, the reading out of a stored "1" from the cell causes the writing of a "0" into the cell.

If a read pulse is applied to a memory cell containing a stored "0", the leading edge of the pulse raises the base potential with respect to the emitter potential sufficiently to forward-bias the emitter-base junction but not sufficiently to allow transistor conduction. The trailing edge of the read pulse then lowers the base potential back to the "0" potential. It is, therefore, apparent that the reading out of a stored "1" or "0" from the cell causes the writing of a "0" into the cell.

If a read pulse is applied to a memory cell that contains a stored "0" some current flow due to the voltage change across the series combination of C_{CB} and C_{BE} is detected by the conduction detector voltage control source. The transistor does not conduct because the base potential does not become positive enough to cause the emitter-base junction to be sufficiently forward-biased to permit conduction. If $C_{BO} = C_{BE}$, then the induced current through them is directly proportional to $C_{BO}/2$. This current is the output signal which represents a stored "0".

If a read pulse is applied to a memory cell that contains a stored "1", an initial current identical to that corresponding to a stored "0" will be detected but, in response to the read pulse, the base potential rapidly increases so as to forward-bias the emitter-base junction which constitutes a low impedance shunt across C_{BE} which limits any further change in potential across C_{BE} . The current now induced in C_{BO} is directly proportional to C_{BO} , and not to $C_{BO}/2$, as is the case for a stored "0". This induced current in C_{BO} flows into the low impedance emitter-base junction, is amplified by a factor of $\beta + 1$ and is detected by the conduction detector circuit that is connected to the emitter. This current is the output signal which represents a stored "1".

The current detected for a stored "1" is, therefore, proportional to $C_{BO}(\beta + 1)$, as compared to a "0" current proportional only to

$C_{BO}/2$. This means that the ratio of the output signal for a "1" to a "0" is approximately $2(\beta+1):1$. A β of even 9 results in a 20:1 difference between a "1" and "0" output signal.

If C_{BO} is greater than C_{BE} , as is the case in many integrated circuit transistors, the current signal representative of a stored "0" is primarily determined by C_{BE} while the current representative of a "1" level is primarily determined by C_{BO} and the beta of the transistor. If $C_{BO}=10 C_{BE}$, the ratio of a "1" signal to "0" signal is $10(\beta+1):1$. For a β of nine this means a ratio of 100:1. Even if C_{BO} is smaller than C_{BE} , there will still be a relatively large difference between the "1" and "0" output currents due to the $\beta+1$ multiplication of the base current.

In one embodiment of the invention each cell comprises an NPN transistor having an uncontacted base. The collector-base junction of the transistor has a breakdown potential of 9.3 volts. A ground based positive polarity voltage pulse having an amplitude of 10 volts is used as the write pulse. A ground based positive polarity voltage pulse having an amplitude of 5 volts is used as the read pulse, and the "0" base potential is approximately -2.1 volts, and the "1" base potential approximately 0 volts.

Relatively large variations in pulse supply voltages can be tolerated with little effect on circuit performance. For example, a write pulse with an amplitude greater than 10 volts can be used with little effect on the value of the "1" base potential. This increased amplitude write pulse causes an increase in collector current that causes a greater number of holes to be temporarily trapped in the transistor after conduction terminates. These additional holes negate the increased amplitude of the trailing edge of the write pulse and thereby maintain the value of "1" base potential at approximately 0 volts.

A read voltage pulse whose amplitude is greater than 5 volts, but smaller than 9.3 volts, causes the "0" base potential to be more negative than -2.1 volts; an amplitude of less than 5 volts but more than 2 volts causes the "0" potential to be more positive than -2.1 volts but less positive than 0 volts the "1" potential.

The conduction detector circuit acts as a low impedance path between the emitter and ground potential in addition to detecting current through the parasitic capacitances and the emitter. As current through the transistor seeks to increase in response to an increased amplitude write pulse, the potential drop across the conduction detector circuit increases, thereby raising the emitter potential with respect to the base potential. This reduces the forward-bias potential across the emitter-base junction limiting the amount of current that flows in the transistor.

As has been described, the read operation causes a "0" to be stored in the cell. At the termination of the read operation the collector and emitter are at approximately ground potential and the base potential is approximately -2.1 volts, the "0" potential. The collector-base and emitter-base junctions are therefore reverse-biased and represent high impedance paths to charge stored on the base. If these reverse-biased junctions were of infinitely high impedance the charge stored in the base, which causes the base potential to be at -2.1 volts, would remain in the base indefinitely, and therefore the information stored in the cell could be read out at any later time. The impedances associated with the reverse-biased junctions, however, do not have infinitely high impedance and therefore charge stored on the base will leak into these reverse-biased junctions and the base potential will reach the same potential as the collector and emitter, 0 volts. If a stored "0" is not detected before the charge leaks from the base and raises the base potential to 0 volts, a "1" will be detected instead of a "0", since the "1" base potential corresponds to a base potential of 0 volts. Stored "1"s are never destroyed unless intentionally removed from the cell.

By using air insulated integrated circuit techniques, it is possible to construct a single memory cell, including wiring, in just one millionth of a square inch. One thousand and twenty-four memory cells can be fabricated and interconnected on a single integrated circuit chip having an area of approximately 0.1 square inch.

An advantage of this cell is that only one voltage pulse circuit, which supplies only positive polarity pulses, is needed.

Referring now to Fig. 2 an array of NPN transistors 10 forms a bit organized memory. The array is arranged in M rows and N columns of individual NPN transistors which are interconnected to form a memory having $M \times N$ memory cells. All of the collector terminals 12 in a common column are interconnected; all of the emitter terminals 14 in a common row are interconnected. Voltage pulse circuits 20 are electrically connected to the common collector terminals 12. Circuits 18, which acts as conduction detectors are low impedance paths to ground potential, are electrically connected to the common emitter terminals 14 through switches 22. The operation of each component cell of the multicell memory is the same as that of the single memory cell of Fig. 1.

In operation, to write a "1" into a pre-selected cell, an approximately ground based positive going write voltage pulse of sufficient amplitude to bias the collector-base junction to avalanche breakdown is applied to the column to which the cell is connected. All other columns are held at ground potential.

The switch corresponding to the row connected to the preselected cell is closed, all other switches are left open.

To read out information stored in a preselected cell and write a "0" into the cell, the same procedure for writing a "1" into the cell is followed except that a voltage pulse of smaller amplitude than the write voltage pulse is used.

The above-mentioned write and read operations allow information to be written into or read out of a preselected cell without destroying information stored in all other cells of the memory array. This feature allows the memory to be used as a bit organized memory.

Referring now to Fig. 3, an array of PNP transistors 24 forms a bit organized memory and again is arranged in M rows and N columns of individual PNP transistors which are interconnected to form a memory having $M \times N$ memory cells. All of the collector terminals 26 in a common column are interconnected; all of the emitter terminals 28 in a common row are interconnected. Voltage pulse circuits 20 are electrically connected to the common collector terminals 26. Circuits 18, which act as conduction detectors and low impedance paths to ground potential, are electrically connected to the common emitter terminals 28 through switches 22.

The operation of this memory is the same as that of the memory of Fig. 2 except that the polarity of the read and write voltage pulses must be reversed. The resulting "0" base potential is more positive than the "1" base potential. Electrons, which are temporarily trapped within the transistor following the termination of transistor conduction, flow into the base and cause the base to assume the "1" potential.

As will now be explained, however, a "1" may be stored in a cell containing a "0" in another way.

Referring again to Fig. 1, in order to write a "1" on a base containing a "0", an approximately ground based write voltage pulse having a negative polarity is applied to the collector terminal 12 by the voltage pulse circuit 20. The leading edge of the write pulse causes the collector-base junction to be forward-biased and the base potential to decrease with respect to the emitter potential such that the emitter-base junction is biased to avalanche breakdown limiting any further decrease in base potential with respect to emitter potential.

Current flows from ground through the series combination of the conduction detector, broken down emitter-base junction, and forward-biased collector-base junction into the voltage pulse circuit. This is opposite to the flow of collector current through a transistor.

The trailing edge of the write pulse first increases the base and emitter potential until avalanche breakdown ceases and then raises

the base potential to a potential more positive than the "0" potential. This resulting base potential is defined as the "1" potential.

Another factor which causes the "1" base potential to be a more positive value than indicated above is the presence of holes within the transistor which, upon the termination of current flow through the transistor, flow into the base and raise its potential.

The rapid termination of current flow through the forward-biased collector-base junction causes holes to be temporarily trapped within the junction. This is commonly known as minority carrier storage. These holes, in order to exit the transistor, must recombine with electrons and then exit the transistor via the collector terminal into the voltage pulse circuit. Some holes are able to exit the transistor due to leakage. The effective lifetime of these trapped holes is a function of the recombination and leakage rates.

Again, in order to take advantage of the effect of these holes, it is necessary for the fall time of the trailing edge of the write pulse to be equal to or less than the effective lifetime of the holes. In a preferred embodiment, the effective lifetime of the holes is approximately 50 nanoseconds and the fall time of the trailing edge of the write pulse is approximately 10 nanoseconds.

Detection of the base potential and thereby determination of the stored information in the cell using an approximately ground based read voltage pulse of positive polarity applied to the collector terminal by the voltage pulse circuit is substantially as previously described in detail. The amplitude of this pulse is, of course, insufficient to bias the collector-base junction to avalanche breakdown.

In one embodiment of the invention adapted to operate in this manner, each cell comprises an NPN transistor having an uncontacted base. The collector-base junction has a breakdown potential of 11 volts. The emitter-base junction has a breakdown potential of 6.5 volts. A ground based negative polarity voltage pulse having an amplitude of 9 volts is used as the write pulse. A ground based positive polarity voltage pulse having an amplitude of 9 volts is used as the read pulse. The "0" base potential is approximately -4.1 volts and the "1" base potential is approximately 0 volts. This 4.1 volt difference between a "1" and "0" compares favourably with presently used DTL and T²L bipolar memory cells.

Relatively large variations in pulse supply voltages can be tolerated with little effect on circuit performance. For example, a negative polarity write pulse having an amplitude of greater than 9 volts can be used with little detrimental effect to the value of the "1" base potential.

Relatively wide variations in the amplitude of the read pulse are possible without any

serious detrimental effect to operation. A read voltage pulse whose amplitude is greater than 9 volts, but less than 11 volts, causes the "0" base potential to be more negative than -4.1 volts; an amplitude of less than 9 volts, but more than 3 volts, causes the "0" potential to be more positive than -4.1 volts but less positive than 0 volts, the "1" potential.

In another embodiment of the invention adapted to operate in this manner each cell comprises an NPN transistor having an uncontacted base and equal avalanche breakdown potentials of 6.5 for the collector-base junction and the emitter-base junction. A ground based negative polarity voltage pulse having an amplitude of 6 volts is used as the write pulse. A ground based positive polarity voltage pulse having an amplitude of 6 volts is used as the read pulse. The "0" base potential is approximately -4.7 volts and the "1" base potential is approximately 0 volts.

A major advantage of this embodiment is that the emitter-base junction operates only momentarily in avalanche breakdown. This means that there is almost no current flowing through the collector-base junction and therefore there is negligible minority carrier storage. Therefore, there is no restriction on the fall time of the trailing edge of the write pulse.

As has been described, the read operation causes a "0" to be stored in the cell. At the termination of the read operation the collector and emitter are at approximately ground potential and the base potential is approximately -4.1 volts, the "0" potential. The collector-base and emitter-base junctions are therefore reverse-biased and represent high impedance paths to charge stored on the base. Once again, because the impedances associated with the reverse-biased junctions do not have infinitely high impedance, charge stored on the base will leak off into these reverse-biased junctions and the base potential will reach the same potential as the collector and emitter, 0 volts. If a stored "0" is not detected before the charge leaks from the base and raises the base potential to 0 volts, a "1" will be detected instead of a "0", since a "1" base potential corresponds to a base potential of 0 volts. Stored "1's" are never destroyed unless intentionally removed from the cell.

By using air insulated integrated circuit techniques it is possible to construct a single memory cell, including wiring in just one millionth of a square inch. One thousand and twenty-four memory cells can be fabricated and interconnected on a single integrated circuit chip having an area of approximately 0.1 square inch.

Referring again to Fig. 2, each memory cell in the bit organized memory may be adapted to operate in the manner just described. Thus to write a "1" into a preselected cell an approximately ground based negative

going write voltage pulse is applied to the column in which the cell is connected. All other columns are held at ground potential. The switch corresponding to the row connected to the preselected cell is closed; all other switches are left open.

In order to read out information stored in a preselected cell and write a "0" into the cell, the same procedure for writing a "1" is followed except that a voltage pulse of opposite polarity to that of the write voltage pulse is used.

Once again these write and read operations allow information to be written into or read out of a preselected cell without destroying information stored in all other cells of the memory array. This feature allows the memory to be used as a bit organized memory.

Referring again to Fig. 3, instead of an array of NPN transistors, an array of PNP transistors 24 forms the bit organized memory. The operation of this memory is the same as just described with reference to Fig. 2 except that the polarities of the read and write voltage pulses must be reversed. The resulting "0" base potential is more positive than the "1" base potential. Electrons, which are temporarily trapped within the transistor following the termination of current flow through the forward-biased collector-base junction, flow into the base and cause the base to assume the "1" potential.

Referring now to Fig. 4, an NPN transistor 110 includes a collector terminal 112, a first emitter terminal 113, a second emitter terminal 114, a resistor 115 coupled between terminals 112 and 113, and an uncontacted base 116. A voltage pulse circuit 120 is connected to emitter terminal 113. A circuit 118 is connected to emitter terminal 114 and acts as a conduction detector and voltage pulse circuit. The parasitic capacitances C_{BO} , C_{BE} , and C_{BB} associated with the collector-base

junction, the first emitter-base junction, and the second emitter-base junction, respectively, are shown external to the transistor in order to simplify the following description of the operation. These capacitances serve as low impedance ac paths between the collector, base and emitters.

The potential of the base 116 floats and is set to one of two values, which represent respectively the storage of a "1" and "0" in the cell by applying appropriate polarity and amplitude voltage pulses to the emitter terminals 113 and 114.

To write a "1" on a base containing a "0", a positive based write voltage pulse having a positive polarity is applied to emitter terminal 113 by the voltage pulse circuit, and a positive based voltage write pulse having a negative polarity is applied to emitter terminal 114 by the conduction detector voltage pulse

circuit. The leading edges of the two write pulses cause the first emitter-base junction to be biased to avalanche breakdown and the base potential to rise so as to forward-bias the second emitter-base junction. The broken down emitter-base junction acts as a low impedance path between the first emitter terminal and the uncontacted base. The base can now receive current from the voltage pulse circuit via the broken down emitter-base junction. Transistor conduction occurs since there is a supply of base current and the second emitter-base junction is forward-biased. The transistor operates in a saturation mode of operation since the resistor coupled between the first emitter and collector is of sufficient ohmic value to drop the collector potential below the base potential, thereby forward-biasing the collector-base junction.

As is well known, when the supply of base current to a transistor operating in saturation is suddenly cut off, holes flow into the base temporarily raising the base potential thereby permitting conduction to continue for a period of time. This time period is determined by the time it takes the holes within the transistor to recombine with electrons and thereby effectively exit the transistor. Some of the holes exit the transistor due to leakage. The effective lifetime of the holes existing in the transistor after conduction ceases is a function of the recombination and leakage rates.

The trailing edges of the write pulses terminates transistor conduction by lowering the bias across the first emitter-base junction causing it to cease to operate in avalanche breakdown, thereby cutting off the supply of base current to the transistor and terminating transistor conduction. The net effect of the trailing edges of the write pulse on the base is to decrease its potential below the "0" potential; however, the holes within the transistor flow into the base and override any decrease in base potential. They in fact cause the base to increase in potential to a potential more positive than the "0" potential. This potential is defined as the "1" potential.

It is necessary that the fall times of the trailing edges of the write pulses be equal to or less than the effective lifetime of the holes in order for the base potential to be raised to the "1" potential and not lowered in potential below the "0" potential. In a preferred embodiment the lifetime of the minority carriers is approximately 50 nanoseconds and the fall times are approximately 10 nanoseconds.

In order to detect the base potential and thereby determine the stored information in the cell, a positive based read voltage pulse having a positive polarity is applied to emitter terminal 113 by the voltage pulse circuit while emitter terminal 114 is held at a positive potential by the conduction detector voltage pulse circuit. The leading edge of the read

pulse causes the base potential to rise sufficiently with respect to the emitter terminal potential to forward-bias the emitter-base junction sufficiently to allow transistor conduction if, and only if, the base was previously at the "1" potential. Transient transistor conduction upon the application of a read pulse to the memory cell is interpreted as a "1", whereas nontransistor conduction is interpreted as a "0".

The pulse width of the read pulse is such that transient transistor conduction, which occurs if the cell was previously at the "1" potential, ceases prior to the start of the trailing edge of the read pulse. Upon termination of transient transistor conduction the second emitter-base junction is left forward-biased, but not sufficiently to permit conduction. The trailing edge of the read pulse then lowers the base potential down to the "0" potential. Therefore, the reading out of a stored "1" from the cell is equivalent to the writing of a "0" into the cell.

If a read pulse is applied to a memory cell containing a stored "0", the leading edge of the pulse raises the base potential with respect to the second emitter potential sufficiently to forward-bias the second emitter-base junction, but not sufficiently to allow transistor conduction. The trailing edge of the read pulse then lowers the base potential back to the "0" potential. It is, therefore, apparent that the reading out of a stored "1" or "0" from the cell causes the writing of a "0" into the cell.

If a read pulse is applied to a memory cell that contains a stored "0", some current flow, due to the voltage change across the series combination of C_{BE1} and C_{BE2} , is detected by

the conduction detector voltage control source. Practically no current flows in C_{BC} due to the relatively large ohmic value of the resistor which shunts the first emitter and the collector. There is no transistor conduction because the base potential does not become positive enough to cause the second emitter-base junction to be sufficiently forward-biased to permit conduction. If $C_{BE1} = C_{BE2}$, then the induced

current is directly proportional to $C_{BE1}/2$.

This current is the output signal representing a stored "0".

If a read pulse is applied to a memory cell that contains a stored "1", an initial current identical to that corresponding to a stored "0" will be detected. In response to the read pulse, the base potential rapidly increases so as to forward-bias the second emitter-base junction. The forward-biased emitter-base junction is a low impedance shunt across C_{BE2} that limits any further

change in potential across C_{BE_2} . The current now induced in C_{BE_1} is directly proportional to C_{BE_1} and not to $C_{BE_1}/2$, as is the case for a stored "0". This induced current in C_{BE_1}

- 5 flows into the forward-biased second emitter-base junction, is amplified by a factor of $\beta+1$ and is detected by the conduction detector voltage pulse circuit that is connected to emitter terminal 114. This current is the
10 output signal which represents a stored "1".

The current detected for a stored "1" is, therefore, proportional to $C_{BE_1}(\beta+1)$, as compared to a "0" current proportional only to $C_{BE_1}/2$. This means that the ratio of the

- 15 output signal for a "1" to a stored "0" is approximately $2(\beta+1):1$. A β of even 9 results in a 20:1 difference between a "1" and "0".

- 20 In one embodiment of the invention each cell comprises an NPN transistor having two electrically separate emitters and an uncontacted base. A resistor of 5,000 ohms is connected between the first emitter and the collector. The reverse breakdown potential of the emitter-base junction is approximately
25 6.5 volts. The amplitude of the positive polarity write voltage pulse applied to emitter terminal 113 is 5 volts; the amplitude of the negative polarity write voltage pulse applied to terminal 114 is 3 volts. The base level of both pulses is +3 volts. The read voltage pulse is identical to the positive polarity write voltage pulse. The "1" base potential is approximately +3.4 volts and the "0" base
30 potential is approximately +.9 volts.

- 35 Relatively large variations in read or write pulse amplitudes can be tolerated with little effect on performance. For example, write pulses with amplitudes greater than 5 volts and 3 volts, respectively, can be used with little effect on the value of the "1" base potential. For example, an increased amplitude of the write pulse applied to emitter
40 terminal 113 causes an increase in collector current that causes a greater number of holes to be temporarily trapped in the transistor after saturation conduction terminates. These additional holes negate the increased amplitude of the trailing edge of the write pulses and thereby maintain the "1" base potential at +.9 volt.

- 45 As has been described, the read operation causes a "0" to be stored in the cell. At the termination of the read operation the potential of two emitters and collector is +3 volts and the potential of the base is +.9 volt, the "0" potential. The emitter-base junctions and the collector-base junction are therefore reverse-biased and represent high impedance
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paths to charge stored on the base. Once again the impedances associated with the reverse-biased junctions do not have infinitely high impedance and therefore charge stored on the base will leak into these reverse-biased junctions and the base potential will reach the same potential as the emitters and collector, +3 volts. If a stored "0" is not detected before the charge leaks from the base, a "1" will be detected instead of a "0", since a base potential of +3 volts is sufficiently close to +3.4 volts, the "1" potential, to be mistaken for a "1". Stored "1's" are never destroyed unless intentionally removed from the cell.

By using standard integrated circuit techniques, it is possible to construct such a memory cell, including wiring, in just ten millionths of a square inch. One hundred memory cells can be fabricated and interconnected on a single integrated circuit chip having an area of approximately 0.1 square inch.

An advantage of this memory cell is that the saturation operation produces a relatively large number of holes within the transistor after the supply of base current is cut off. These holes are able to cause a relatively large increase in the base potential which allows relatively wide tolerances on the amplitudes of the write pulses.

Referring now to Fig. 5, an array of transistors 110 forms a bit organized memory. The array is arranged in M rows and N columns of individual NPN transistors which are interconnected to form a memory having $M \times N$ memory cells. All of the emitter terminals 113 in a common column are interconnected; all of the emitter terminals 114 in a common row are interconnected. Voltage pulse circuits 120 are electrically connected to the common emitter terminals 113. Circuits 118, which act as conduction detectors and voltage pulse circuits are electrically connected to the common emitter terminals 114 through switches 122.

In operation, to write a "1" into a preselected cell, a positive based write pulse having a positive polarity is applied to the column to which emitter terminal 113 of the preselected cell is electrically connected and a positive based write pulse having a negative polarity is electrically connected to the row containing emitter terminal 114 of the preselected cell. All other columns are held at a positive potential. The switch corresponding to the row connected to the preselected cell is closed; all other switches are left open.

To read out information stored in a preselected cell and write a "0" into the cell, the same procedure for writing a "1" into the cell is used except that emitter terminal 114 is held at a positive potential instead of being pulsed negatively.

The above-mentioned write and read opera-

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tions allow information to be written into or read out of a preselected cell without destroying information stored in all other cells of the memory array. This feature allows the memory to be used as a bit organized memory.

One undesirable feature associated with this embodiment is that the writing of a "1" into a preselected cell will cause all other cells in the common row to conduct for a period of time. The base potential of each of these cells will be first lowered, permitting conduction, and then raised, cutting off conduction. This causes some change in the value of "1" and "0" potentials, but still leaves the "1" potential as the more positive of the two. As a practical matter these variations in the "1" and "0" base potential can be tolerated without any serious detrimental effect to circuit performance.

Referring now to Fig. 6, an array of PNP transistors 124 forms a bit organized memory. The array is organized in M rows and N columns of individual PNP transistors which are interconnected to form a memory having M×N cells. All of the emitter terminals 126 in a common column are interconnected; all of the emitter terminals 128 in a common row are interconnected. Voltage pulse circuits 120 are electrically connected to the common emitter terminals 128. Circuits 118, which act as conduction detectors and voltage pulse circuits, are electrically conducted to the common emitter terminals 128 through switches 122.

The operation of this memory is the same as that of the memory of Fig. 5 except that the polarities of the read and write voltage pulses must be reversed. The "0" base potential is more positive than the "1" base potential. Electrons, which are temporarily trapped within the transistor following the termination of saturation conduction, flow into the base and cause the base to assume the "1" potential.

The embodiments described are not of course limiting. Various modifications will occur to those skilled in the art. For example, the bit organized memory can be easily converted into a word organized memory.

WHAT WE CLAIM IS:—

1. Semiconductor memory apparatus comprising a plurality of memory cells, each of which comprises an NPN junction transistor having an uncontacted base the potential of which, in operation, floats at two different value which represent, respectively, the storage of a "1" and "0" in the cell, first means for selectively changing a stored "0" to a "1" in said cells comprising means for increasing the collector potential of the transistor of the or each selected cell from an initial value to a value sufficient to bias the collector-base junction to avalanche break-

down and to increase the base potential sufficiently to forward-bias the emitter-base junction, thereby causing transistor conduction, and for then decreasing the collector potential to its initial value, whereby transistor conduction is terminated leaving holes trapped within the transistor, whereupon the base returns to a different, "1", potential, and second means for reading out stored information.

2. Apparatus as claimed in claim 1 wherein said second means comprises a conduction detector circuit for coupling to the emitter of the transistor of the or each cell whose information is to be read out, and means for increasing the collector potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in that cell, and for then lowering the collector potential to its initial value, whereby the base assumes its "0" potential, and there is provided a plurality of conduction paths for coupling said memory cells to said first and second means.

3. Semiconductor memory apparatus comprising a plurality of memory cells, each of which comprises a PNP junction transistor having an uncontacted base the potential of which, in operation, floats at two different value which represent, respectively, the storage of a "1" and "0" in the cell, first means for selectively changing a stored "0" to a "1" in said cells comprising means for decreasing the collector potential of the transistor of the or each selected cell from an initial value to a value sufficient to bias the collector-base junction to avalanche breakdown and to decrease the base potential sufficiently to forward-bias the emitter-base junction, thereby causing transistor conduction, and for then increasing the collector potential to its initial value, whereby transistor conduction is terminated leaving electrons trapped within the transistor, whereupon the base returns to a different, "1" potential, and second means for reading out stored information.

4. Apparatus as claimed in claim 3 wherein said second means comprises a conduction detector circuit for coupling to the emitter of the transistor of the or each cell whose information is to be read out, and means for decreasing the collector potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in the cell, and for then increasing the collector potential to its initial value, whereby the base assumes its "0" potential, and there is provided a plurality of conduction paths for coupling said memory cells to said first and second means.

5. Semiconductor memory apparatus comprising a plurality of memory cells, each of



tions allow information to be written into or read out of a preselected cell without destroying information stored in all other cells of the memory array. This feature allows the memory to be used as a bit organized memory.

One undesirable feature associated with this embodiment is that the writing of a "1" into a preselected cell will cause all other cells in the common row to conduct for a period of time. The base potential of each of these cells will be first lowered, permitting conduction, and then raised, cutting off conduction. This causes some change in the value of "1" and "0" potentials, but still leaves the "1" potential as the more positive of the two. As a practical matter these variations in the "1" and "0" base potential can be tolerated without any serious detrimental effect to circuit performance.

Referring now to Fig. 6, an array of PNP transistors 124 forms a bit organized memory. The array is organized in M rows and N columns of individual PNP transistors which are interconnected to form a memory having $M \times N$ cells. All of the emitter terminals 126 in a common column are interconnected; all of the emitter terminals 128 in a common row are interconnected. Voltage pulse circuits 120 are electrically connected to the common emitter terminals 128. Circuits 118, which act as conduction detectors and voltage pulse circuits, are electrically conducted to the common emitter terminals 128 through switches 122.

The operation of this memory is the same as that of the memory of Fig. 5 except that the polarities of the read and write voltage pulses must be reversed. The "0" base potential is more positive than the "1" base potential. Electrons, which are temporarily trapped within the transistor following the termination of saturation conduction, flow into the base and cause the base to assume the "1" potential.

The embodiments described are not of course limiting. Various modifications will occur to those skilled in the art. For example, the bit organized memory can be easily converted into a word organized memory.

WHAT WE CLAIM IS:—

1. Semiconductor memory apparatus comprising a plurality of memory cells, each of which comprises an NPN junction transistor having an uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, first means for selectively changing a stored "0" to a "1" in said cells comprising means for increasing the collector potential of the transistor of the or each selected cell from an initial value to a value sufficient to bias the collector-base junction to avalanche break-

down and to increase the base potential sufficiently to forward-bias the emitter-base junction, thereby causing transistor conduction, and for then decreasing the collector potential to its initial value, whereby transistor conduction is terminated leaving holes trapped within the transistor, whereupon the base returns to a different, "1", potential, and second means for reading out stored information.

2. Apparatus as claimed in claim 1 wherein said second means comprises a conduction detector circuit for coupling to the emitter of the transistor of the or each cell whose information is to be read out, and means for increasing the collector potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in that cell, and for then lowering the collector potential to its initial value, whereby the base assumes its "0" potential, and there is provided a plurality of conduction paths for coupling said memory cells to said first and second means.

3. Semiconductor memory apparatus comprising a plurality of memory cells, each of which comprises a PNP junction transistor having an uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, first means for selectively changing a stored "0" to a "1" in said cells comprising means for decreasing the collector potential of the transistor of the or each selected cell from an initial value to a value sufficient to bias the collector-base junction to avalanche breakdown and to decrease the base potential sufficiently to forward-bias the emitter-base junction, thereby causing transistor conduction, and for then increasing the collector potential to its initial value, whereby transistor conduction is terminated leaving electrons trapped within the transistor, whereupon the base returns to a different, "1" potential, and second means for reading out stored information.

4. Apparatus as claimed in claim 3 wherein said second means comprises a conduction detector circuit for coupling to the emitter of the transistor of the or each cell whose information is to be read out, and means for decreasing the collector potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in the cell, and for then increasing the collector potential to its initial value, whereby the base assumes its "0" potential, and there is provided a plurality of conduction paths for coupling said memory cells to said first and second means.

5. Semiconductor memory apparatus comprising a plurality of memory cells, each of



which comprises an NPN junction transistor having a uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, first means for selectively changing a stored "0" to a "1" in said cells comprising means for decreasing the collector potential of the transistor of the or each selected cell from an initial value to a value that causes the collector-base junction to be forward-biased and the base potential to decrease in potential toward a potential greater than that necessary to bias the emitter-base junction to avalanche breakdown, thereby causing the emitter-base junction to operate in avalanche breakdown and preventing the base potential from decreasing further, and for then increasing the collector potential to its initial value, whereupon the base assumes a different, "1", potential, and second means for reading out stored information.

6. Apparatus as claimed in claim 5 wherein said second means comprises a conduction detector circuit for coupling to the emitter of the transistor of the or each cell whose information is to be read out, and means for increasing the collector potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in the cell, and for then decreasing the collector potential to its initial value, whereby the base assumes its "0" potential, and there is provided a plurality of conduction paths for coupling said memory cells to said first and second means.

7. Semiconductor memory apparatus comprising a plurality of memory cells, each of which comprises a PNP junction transistor having an uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, first means for selectively changing a stored "0" to a stored "1" in said cells comprising means for increasing the collector potential of the transistor of the or each selected cell from an initial value to a value that causes the collector-base junction to be forward-biased and the base potential to increase in potential toward a potential greater than that necessary to bias the emitter-base junction to avalanche breakdown, thereby causing the emitter-base junction to operate in avalanche breakdown and preventing the base potential from increasing further, and for then decreasing the collector potential to its initial value, whereupon the base assumes a different, "1", potential, and second means for reading out stored information.

8. Apparatus as claimed in claim 7 wherein said second means comprises a conduction detector circuit for coupling to the emitter of the transistor of the or each cell whose

information is to be read out, and means for decreasing the collector potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in the cell, and for then increasing the collector potential to its initial value, whereby the base assumes its "0" potential, and there is provided a plurality of conduction paths for coupling said memory cells to said first and second means.

9. Semiconductor memory apparatus comprising a plurality of NPN memory cells, each of which comprises a junction transistor having two electrically isolated emitters, an uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, and a resistor connected between the first emitter and the collector, first means for selectively changing a stored "0" to a "1" in said cells comprising means for adjusting each emitter potential of the transistor of the or each selected cell from an initial value to a value sufficient to bias the first emitter-base junction to avalanche breakdown and to increase the base potential sufficiently to forward-bias the collector-base junction and the second emitter-base junction thereby causing the transistor to conduct in saturation, and for then returning each emitter potential to its initial value, whereby transistor conduction is terminated leaving holes trapped within the transistor, whereupon the base returns to a different, "1", potential, and second means for reading out stored information.

10. Apparatus as claimed in claim 9 wherein said second means comprises a conduction detector circuit for coupling to the second emitter of the transistor of the or each cell whose information is to be read out, and means for increasing the first emitter potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in the cell, and for then decreasing the emitter potential to its initial value, whereby the base assumes its "0" potential, and there is provided a plurality of conduction paths for coupling said memory cells to said first and second means.

11. Semiconductor memory apparatus comprising a plurality of PNP memory cells, each of which comprises a junction transistor having two electrically isolated emitters, an uncontacted base the potential of which, in operation, floats at two different values which represent, respectively, the storage of a "1" and "0" in the cell, and a resistor connected between the first emitter and the collector, first means for selectively changing a stored "0" to a "1" in said cells comprising means for adjusting each emitter potential of the transistor of the or each selected cell from



an initial value to a value sufficient to bias the first emitter-base junction to avalanche breakdown and to decrease the base potential sufficiently to forward-bias the collector-base junction and the second emitter-base junction, thereby causing the transistor to conduct in saturation, and for then returning each emitter potential to its initial value, whereby transistor conduction is terminated leaving electrons trapped within the transistor, whereupon the base returns to a different, "1", potential, and second means for reading out stored information.

12. Apparatus as claimed in claim 11 wherein said second means comprises a conduction detector circuit for coupling to the second emitter of the transistor of the or each cell whose information is to be read out, and means for decreasing the first emitter potential of the transistor of the or each cell from an initial value to a value sufficient to cause transient transistor conduction only if a "1" is stored in the cell, and for then increasing the emitter potential to its initial value, whereby the base assumes its "0" potential, and there is provided a plurality of conduction paths for coupling said memory cells to said first and second means.

13. Apparatus as claimed in any one of claims 2, 4, 6, 8, 10 and 12 wherein said first and second means comprise a voltage pulse circuit adapted to supply voltage pulses of different amplitudes and, where required, different polarities.

14. Apparatus as claimed in any one of claims 2, 4, 6, 8, 10, 12 and 13 wherein the or each conduction detector circuit is coupled to a reference ground potential.

15. Apparatus as claimed in claim 14 wherein the or each conduction detector circuit is of low impedance for coupling the or each emitter coupled thereto to said reference ground potential.

16. Apparatus as claimed in any one of claims 2, 4, 6, 8, 10, 12, 13, 14 and 15 comprising electrically actuatable switches which, in conjunction with said first and second means and said conduction paths, are arranged to selectively connect the or each detector circuit to the or each emitter, whereby a "1" or "0" can be selectively stored in and selectively read from said memory cells.

17. Memory apparatus comprising a plurality of memory cells substantially as herein described with reference to Figs. 1 to 3 of the accompanying drawings.

18. Memory apparatus comprising a plurality of memory cells substantially as herein described with reference to Figs. 4 to 6 of the accompanying drawings.

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