WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a stack structure including interlayer insulating layers and electrode patterns which are alternately stacked on each other; and

a support passing through the stack structure,

wherein each of the electrode patterns includes a first conductive pattern, penetrated by the support, at least one second conductive pattern, extending along a side portion of the stack structure, and at least one third conductive pattern disposed between the first conductive pattern and the support, and

wherein the first conductive pattern includes a first conductive material and each of the second and third conductive patterns includes a second conductive material having a lower resistance than the first conductive material.

2. The semiconductor device of claim 1, wherein the first conductive pattern extends between the second conductive pattern and the third conductive pattern.

3. The semiconductor device of claim 1, wherein the second conductive pattern is coupled to the third conductive

pattern.

4. The semiconductor device of claim 1, further comprising channel structures passing through the stack structure.

5. The semiconductor device of claim 1, wherein the support includes protrusions protruding towards both sides of the stack structure to form a T-shape.

6. The semiconductor device of claim 5, wherein the third conductive pattern extends along a sidewall of at least one of the protrusions.

~~7. A semiconductor device, comprising:~~

~~interlayer insulating layers stacked to be spaced apart from each other;~~

~~a support passing through the interlayer insulating layers;~~

~~at least one opening passing through the interlayer insulating layers to expose a sidewall of the support; and~~

~~electrode patterns filling spaces between the interlayer insulating layers.~~

~~8. The semiconductor device of claim 7, the~~

~~semiconductor device further comprises slits passing through the interlayer insulating layer,~~

~~wherein the at least one opening is formed along the sidewall of the support which faces at least one of the slits.~~

~~9. The semiconductor device of claim 8, wherein each of the electrode patterns comprises:~~

~~a first conductive pattern penetrated by the support;~~

~~a second conductive patterns disposed adjacent to each of the slits and extending along a side portion of the first conductive pattern which faces each of the slits; and~~

~~a third conductive pattern disposed adjacent to one of the at least one opening.~~

~~10. The semiconductor device of claim 9, wherein the first conductive pattern includes a first conductive material, and~~

~~wherein each of the second and third conductive patterns includes a second conductive material having a lower resistance than the first conductive material.~~

~~11. The semiconductor device of claim 9, wherein the first conductive pattern extends between the second conductive pattern and the third conductive pattern.~~

~~12. The semiconductor device of claim 9, wherein the second conductive pattern is coupled to the third conductive pattern.~~

~~13. The semiconductor device of claim 9, wherein the support includes protrusions protruding towards the slits to form a T-shape, and~~

~~wherein the third conductive pattern extends along a sidewall of at least one of the protrusions.~~

~~14. The semiconductor device of claim 7, further comprising channel structures passing through the interlayer insulating layers and the electrode patterns.~~

~~15. A method of manufacturing a semiconductor device, the method comprising:~~

~~forming a stack structure including interlayer insulating layers and sacrificial layers, which surround a support and are alternately stacked on each other;~~

~~forming slits which pass through the stack structure, wherein the support is disposed between the slits;~~

~~forming a first opening which passes through the stack structure, wherein the first opening opens a side portion of the support;~~

~~forming second openings by removing the sacrificial layers through the slits and the first opening; and~~

~~forming an electrode pattern in each of the second openings through the slits and the first opening.~~

~~16. The method of claim 15, wherein the forming of the electrode pattern comprises:~~

~~forming a first conductive material filling each of the second openings through the slits and the first opening;~~

~~forming a first conductive pattern by partially etching the first conductive material through the slits and the first opening, wherein the first conductive pattern is exposed by a corresponding one of portions of the second openings, the portions of the second openings adjacent to the slits and the first opening;~~

~~filling the portions of the second openings with a second conductive material through the slits and the first opening; and~~

~~forming a second conductive pattern adjacent to each of the slits, and a third conductive pattern adjacent to the first opening by etching the second conductive material.~~

~~17. The method of claim 16, wherein the second conductive material has a lower resistance than the first conductive material.~~

~~18. The method of claim 16, wherein the first conductive material includes a titanium nitride layer, and~~

~~wherein the second conductive material includes tungsten.~~

~~19. The method of claim 16, wherein the second conductive pattern and the third conductive pattern are coupled to each other.~~

~~20. The method of claim 16, wherein the second conductive pattern and the third conductive pattern are separated from each other by the first conductive pattern.~~