

CLAIMS

1. A microcontroller comprising:
 - a CPU;
 - a controller;
 - a timer circuit;
 - a first register in the CPU;
 - a second register electrically connected to the timer circuit; and
 - a power gate configured to supply power to the CPU, the timer circuit, the first register and the second register,

wherein the microcontroller is configured to be in an operation mode,

wherein the operation mode includes at least:

 - a first mode, the first mode being a mode where the CPU, the timer circuit, the first register, the second register and the controller operate;
 - a second mode, the second mode being a mode where the timer circuit, the second register and the controller operate; and
 - a third mode, the third mode being a mode where the controller operates,

wherein the microcontroller is configured to shift from the first mode to one of the second mode and the third mode by an instruction of the CPU,

wherein the microcontroller is configured to shift from the second mode to the first mode by the controller in accordance with a first signal supplied from the timer circuit,

wherein the microcontroller is configured to shift from the third mode to the first mode by the controller in accordance with a second signal supplied to the controller, and

wherein the first register and the second register each comprises:

 - a first volatile memory; and
 - a first nonvolatile memory comprising a first transistor, wherein a channel formation region of the first transistor comprises a first multilayer film,

wherein the first multilayer film has a structure in which a first oxide layer, an oxide semiconductor layer, and a second oxide layer are stacked in number order, and

wherein the first oxide layer has a larger energy gap than the oxide semiconductor layer.

2. The microcontroller according to claim 1,
 wherein the CPU and the first register do not operate in the second mode, and
 wherein the CPU, the first register, the timer circuit, and the second register do not operate in the third mode.

3. The microcontroller according to claim 1, further comprising:
 an I/O port;
 a third register electrically connected to the I/O port;
 a comparator; and
 a fourth register electrically connected to the comparator,
 wherein the I/O port, the third register, the comparator, and the fourth register operate in the first mode, and do not operate in the second and third modes.

4. The microcontroller according to claim 1, further comprising:
 an interrupt controller; and
 a fifth register electrically connected to the interrupt controller,
 wherein the interrupt controller and the fifth register operate in the first mode, and do not operate in the second and third modes.

5. The microcontroller according to claim 1, further comprising:
 an interrupt controller; and
 a fifth register electrically connected to the interrupt controller,
 wherein the interrupt controller and the fifth register operate in the first mode, and do not operate in the second and third modes, and
 wherein the fifth register comprises:

a second volatile memory; and
a second nonvolatile memory comprising a second transistor, wherein
a channel formation region of the second transistor comprises a second
multilayer film.

6. The microcontroller according to claim 1, further comprising:
a RAM electrically connected to the CPU,
wherein the RAM comprising a third transistor, and
wherein a channel formation region of the third transistor comprises a third
multilayer film.

7. The microcontroller according to claim 1, wherein the timer circuit is
configured to output the first signal at regular intervals.

8. The microcontroller according to claim 1,
wherein the first nonvolatile memory is configured to back up a data stored in
the first volatile memory before power supply is stopped by the power gate, and
wherein the data backed up in the first nonvolatile memory is written into the
first volatile memory in a case where power supply is started again by the power gate.

9. The microcontroller according to claim 1, wherein the first multilayer film
comprises indium, gallium, and zinc.

10. The microcontroller according to claim 1,
wherein the first oxide layer or the second oxide layer comprises indium
more than or equal to 1.5 times of the amount of the oxide semiconductor layer
interposed between the first oxide layer and the second oxide layer.

11. A microcontroller comprising:
a CPU;
a controller;

a timer circuit;
 a first register in the CPU;
 a second register electrically connected to the timer circuit; and
 a power gate configured to supply power to the CPU, the timer circuit, the first register and the second register,
 wherein the microcontroller is configured to be in an operation mode,
 wherein the operation mode includes at least:

- a first mode, the first mode being a mode where the CPU, the timer circuit, the first register, the second register and the controller operate;
- a second mode, the second mode being a mode where the timer circuit, the second register and the controller operate; and
- a third mode, the third mode being a mode where the controller operates,

wherein the microcontroller is configured to shift from the first mode to one of the second mode and the third mode by an instruction of the CPU,
 wherein the microcontroller is configured to shift from the second mode to the first mode by the controller in accordance with a first signal supplied from the timer circuit,
 wherein the microcontroller is configured to shift from the third mode to the first mode by the controller in accordance with a second signal supplied to the controller,
 wherein the first register and the second register each comprises:

- a first volatile memory; and
- a first nonvolatile memory comprising a first transistor and a fourth transistor,

wherein a channel formation region of the first transistor comprises a first multilayer film, and wherein a channel formation region of the fourth transistor comprises single crystal silicon,
 wherein the first multilayer film has a structure in which a first oxide layer, an oxide semiconductor layer, and a second oxide layer are stacked in number order, and

wherein the first oxide layer has a larger energy gap than the oxide semiconductor layer.

12. The microcontroller according to claim 11,
wherein the CPU and the first register do not operate in the second mode, and
wherein the CPU, the first register, the timer circuit and the second register
do not operate in the third mode.

13. The microcontroller according to claim 11, further comprising:
an I/O port;
a third register electrically connected to the I/O port;
a comparator; and
a fourth register electrically connected to the comparator,
wherein the I/O port, the third register, the comparator, and the fourth register
operate in the first mode, and do not operate in the second and third modes.

14. The microcontroller according to claim 11, further comprising:
an interrupt controller; and
a fifth register electrically connected to the interrupt controller,
wherein the interrupt controller and the fifth register operate in the first mode,
and do not operate in the second and third modes.

15. The microcontroller according to claim 11, further comprising:
an interrupt controller; and
a fifth register electrically connected to the interrupt controller,
wherein the interrupt controller and the fifth register operate in the first mode,
and do not operate in the second and third modes, and
wherein the fifth register comprises:
a second volatile memory; and

a second nonvolatile memory comprising a second transistor, wherein a channel formation region of the second transistor comprises a second multilayer film.

16. The microcontroller according to claim 11, further comprising:
a RAM electrically connected to the CPU,
wherein the RAM comprising a third transistor, and
wherein a channel formation region of the third transistor comprises a third multilayer film.

17. The microcontroller according to claim 11, wherein the timer circuit is configured to output the first signal at regular intervals.

18. The microcontroller according to claim 11,
wherein the first nonvolatile memory is configured to back up a data stored in the first volatile memory before power supply is stopped by the power gate, and
wherein the data backed up in the first nonvolatile memory is written into the first volatile memory in a case where power supply is started again by the power gate.

19. The microcontroller according to claim 11, wherein the first multilayer film comprises indium, gallium, and zinc.

20. The microcontroller according to claim 11,
wherein the first oxide layer or the second oxide layer comprises indium more than or equal to 1.5 times of the amount of the oxide semiconductor layer interposed between the first oxide layer and the second oxide layer.