ELECTRONIC PART

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to an electronic part, especially to such an electronic part as being called a package, which comprises a lead frame, an organic substrate, a ceramic substrate, and the like.

DESCRIPTION OF THE RELATED ART

In late years, various electric parts so-called an IC package are known as one loaded with, for example, a semiconductor chip. For instance, a package comprises of a lead frame, organic substrate, ceramic substrate, and the like can be enumerated. Such an electronic part referred to as a package have been improved on a daily basis in response to a requirement for high-density packaging, more specifically the improvement includes miniaturization and increase in the number of pins, and the demand has been becoming stricter.

Such an IC package is basically an electric part formed by a chip having joining terminals and a substrate comprising a chip-mounting section, on which the chip is mounted via the joining terminals and packaging terminals for mounting the chip on the substrate. For the electric part having such a formation, solders and bonding wires have been used as a jointing material, which have been established as a joint technology indispensable when an IC package is mounted on a substrate, for example a printed wiring board.

In regard to the surface mount technology for an electronic part, for instance in a case of a lead frame, in order to improve a joining characteristic of a wire bonded and of a soldered junction terminal, there is known a

formation where nickel plating film, palladium plating film, and gold plating film are formed in this order on a surface of a copper, which composes a terminal (see Patent Document 1: Japanese Patent Application Laid-open No. 8438/1997).

Thus, a palladium plating film is used to prevent a substrate or basis material copper from diffusing and ensure joint via soldering or wire bonding. However, with the miniaturization of electronic and semiconductor parts and progress in mounting technology thanks to density growth, demands of these jointing characteristic have been becoming severe increasingly.

To meet the demands, there has been proposed a technology in which elements for example tellurium or antimony are added to a palladium plating film to form a joint of an outer lead of a lead frame (see Patent Document 2: Japanese Patent Application Laid-open No. 232311/1994). Such a palladium plating film, if subjected to a certain degree of thermal history, can achieve a good junction characteristic.

SUMMARY OF THE INVENTION

However, under the present set of circumstances where reduction of area or of film thickness of a joining area in itself is under way in step with the miniaturization and high density of a package, it is demanded a junction technique, which achieves a good junction state even when the joining area is subjected to high-temperature thermal history. Especially, in a junction to a solder, it is an actual condition that there is a strong demand for an electronic part, from the standpoint of improved production efficiency, which is provided with joining areas having superior thermal resistance that allows good junction even when the joining areas are subjected to high-temperature thermal history.

The present invention has been made against the above-described background, and it is an object of the present invention to provide an electronic part comprising: a chip having joining terminals; and a substratum having a chip-mounting section on which the chip is mounted via the joining terminals and packaging terminals by which the chip is mounted on a substrate, wherein a junction characteristic via for example soldering has been further improved. Especially, it is a more specific object of the invention to provide an IC package, which has a superior heat resistance when solder is employed for junction.

In order to solve the above problems, the present inventors had been making intensive studies on palladium plating films. Consequently, they discovered a junction characteristic where solder or bonding wire is employed would be dramatically improved when the joining terminals or packaging terminals in an electronic part is formed with palladium plating films to which germanium has been added, and arrived at the present invention.

The present invention provides an electronic part, which comprises: a chip having joining terminals; and a substratum having a chip-mounting section on which the chip is mounted via the joining terminals and packaging terminals by which the chip is mounted on a substrate, characterized in that at least any of the said joining terminals of the chip, the said chip-mounting section of and packaging terminals of the substrate are formed with palladium plating films, which contain germanium. The present invention can materialize an electronic part having a very high heat resistance in terms of a junction via soldering and wire bonding.

In the an electronic part according to the present invention, it is desirable if a nickel plating film has been formed as an undercoat for a palladium plating film. It is possible to form directly a palladium plating film

onto a conductive part such as copper, however an electronic part having a superior heat resistance can be established more assuredly if the conductive part is coated with a nickel plating as an undercoat, and then a germanium-containing palladium plating film is formed on it, thereby forming joining terminals of the chip, chip-mounting section of and packaging terminals of the substrate.

It is desirable if the palladium plating film has a thickness between 0.001 and 5μm, and desirable if the germanium content of the palladium plating film is between 1 and 10000ppm. The reason for the former is that when the film thickness is less than 0.001μm, a barrier effect of the palladium plating film will be reduced, thereby a superior heat resistance could not be materialized, and when the thickness exceeds 5μm, increased amount of palladium will also increase the cost, thereby making it impractical. The reason for the latter is that when the germanium content of the palladium plating film is less than 1ppm, a barrier effect of the palladium plating film will be reduced, thereby a superior heat resistance could not be materialized, and when the content exceeds 10000ppm, it may adversely affect a wire bonding characteristic and that of soldering.

The present invention is very suitable to an electronic part, which is a package comprising any of a lead frame, an organic substrate, or a ceramic substrate. In a case where the electronic part of the present invention is an IC package of a lead frame type, a germanium-containing palladium plating film will be formed onto an inner lead or onto an outer lead. Further, in a case of an IC package comprising an organic substrate or a ceramic substrate, a germanium-containing palladium plating film will be formed onto such sections referred to as a pad, pin, and land. That is to say, when a chip is loaded onto or connected to a substratum in forming an electronic part, or when an electronic part is mounted on a substrate or the like, a

heat-resistance-improved electronic part will be provided if germanium-containing palladium plating films are formed onto joining areas, which are being joined via soldering or wire bonding. It is also effective to form a germanium-containing palladium plating film onto each connecting area on a substrate on which an electronic part should be mounted.

In forming the electronic part of the present invention, it is desirable to use a germanium-containing palladium plating solution in a palladium plating solution, which contains soluble palladium salt and electrically conductive salt. More specifically, the applicable palladium plating solution is that the amount of the soluble palladium salt is 0.1 g/L to 50 g/L in terms of a reduced value of palladium metal, the amount of the electrically conductive salt is 10 g/L to 400 g/L, and the amount of the germanium is 0.1 mg/L to 1000 mg/L.

As the soluble palladium salt of the palladium plating solution, it is preferable if amino group-based palladium complex or ammonia-based palladium complex is contained, and more particularly, it can be selected for use from the group consisting of palladium chloride, dichloroethylenediamine palladium (II), dichlorodiammine palladium (II), dinitrodiammine palladium (II), tetraammine palladium (II) nitrate, tetraammine palladium (II) sulfate, oxalatodiammine palladium (II), tetraammine palladium (II) oxalate and tetraammine palladium (II) chloride. It is also permissible to combine two or more of these elements. As the electrically conductive salt, ammonium chloride, ammonium nitrate, ammonium sulfate, or the like are applicable.

The present invention can materialize an electronic part having a high heat resistance and a superior junction characteristic in a junction via soldering or wire bonding in a package comprising any of a lead frame, an organic substrate, or a ceramic substrate.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a flowchart of fabrication of a sample for evaluating solder wettability.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described below on the basis of actual examples carried out.

In the embodiments, a junction to a solder is formed by using a palladium plating solution of the present invention, the evaluation of solder wettability is performed, and a description will be given of results of an investigation into the effectiveness of a palladium plating film.

In the evaluation of solder wettability, a Cu alloy-based lead frame on the surface of which a junction was formed by the plating treatment of a nickel plating film, a palladium plating film and a gold plating film in order was used as an evaluation sample. Each of the plating treatment conditions used in forming this junction is described below.

<Nickel plating treatment> (Target film thickness: 0.7 μm)
SULFAMEX 100 (made by Electroplating Engineers of Japan Ltd., liquid composition: a plating solution containing nickel sulfamate)

Liquid temperature	50°C
Current density	3 A/dm^2

<Palladium plating treatment> (Target film thickness: 0.03 μm)

Dichlorodiamminepalladium (on a Pd metal basis)	4 g/L
Ammonia solution	20 ml/L
Ammonium chloride	100 g/L
Germanium oxide (on a Ge metal basis)	10, 100, 500 mg/L
pH	8.5

Liquid temperature	55°C
Current density	0.75 A/dm^2

<Gold plating treatment> (Target film thickness: 0.007 μm)

POSTFLASH 100 (made by Electroplating Engineers of Japan Ltd., a plating solution containing potassium gold cyanide)

Liquid temperature	50°C
Current density	0.05 A/dm^2

An evaluation sample for the evaluation of solder wettability was prepared by performing each of the above-described plating treatment on the surface of a lead frame according to the flow of steps shown in FIG. 1.

The first electrolytic degreasing treatment shown in Fig. 1 (EETOREX 12, made by Electroplating Engineers of Japan Ltd., liquid temperature: 60°C, applied voltage: 6 V, immersion time: 30 seconds) was performed as a pretreatment for removing pollutants, oxides and the like on the lead frame surface.

As the evaluation sample, three kinds in all were prepared in which a palladium plating film was formed by changing the amount of added germanium in the plating solution at there levels of 10, 100 and 500 mg/L (Embodiments 1 to 3 in Fig. 1).

[Table 1]

	Amount of added germanium
Embodiment 1	10 mg/L
Embodiment 2	100 mg/L
Embodiment 3	500 mg/L

An evaluation sample (a conventional example) was prepared by using a conventional palladium plating solution. In this conventional example, the following palladium plating was performed, and all other conditions, such as the nickel plating treatment, gold plating conditions, flow of steps and the like, were the same as in the case of the evaluation samples of the above-described embodiments.

<Palladium plating treatment of conventional example> (Target film thickness: 0.03 μm)

Dichlorodiamminepalladium (on a Pd metal basis)	10 g/L
Ammonia solution	20 ml/L
Ammonium chloride	100 g/L
pH	8.5
Liquid temperature	55°C
Current density	0.75 A/dm^2

Furthermore, to make a comparison, an evaluation sample (a comparative example) was prepared by using a palladium plating solution containing tellurium (Te). In this comparative example, the following palladium plating was performed, and all other conditions, such as the nickel plating treatment, gold plating conditions, flow of steps and the like, were the same as in the case of the evaluation samples of the above-described embodiments. Incidentally, in the palladium plating film of this comparative example, the amount of co-deposited tellurium in the film was 29 ppm.

<Palladium plating treatment of comparative example> (Target film thickness: 0.03 μm)

Dichlorodiamminepalladium (on a Pd metal basis)	4 g/L

Ammonia solution	20 ml/L
Ammonium chloride	100 g/L
Tellurium	50 mg/L
pH	8.5
Liquid temperature	55°C
Current density	0.75 A/dm^2

For each of the above-described evaluation samples, a solder wettability evaluation test was carried out. This solder wettability evaluation test is a test in which after the immersion of an evaluation sample in a solder bath, the time required until the force received from the solder bath becomes 0 (zero) is measured and this time is evaluated as solder wettability (what is called a zero cross time (ZCT) test). Concrete conditions are as follows.

<Solder wettability evaluation test conditions>

- Flux: Rosin flux
- Solder bath: 63% tin-37% lead, liquid temperature 230 ± 5°C
- Sample immersion rate: 2 mm/second
- Sample immersion depth: 2 mm
- Number of immersed samples: 1 sample

In the above-described solder wettability evaluation, the test was carried out by holding each heat temperature of the samples at 380 ± 5°C for 1 minute and at 400 ± 5°C for 30 seconds. Incidentally, for each of the samples, measurements were made three times under the same conditions. The results of the measurements are shown in Table 2 (heating conditions: 380 ± 5°C) and Table 3 (heating conditions: 400 ± 5°C).

[Table 2]

	Zero cross time (seconds)		
	Minimum value	Maximum value	Average value
Embodiment 1	0.46	0.53	0.49
Embodiment 2	0.49	0.54	0.50
Embodiment 3	0.41	0.51	0.46
Conventional Example	2.09	4.03	3.06
Comparative Example	1.43	1.46	1.44

(Heating conditions: 380 ± 5°C, holding for 1 minute)

[Table 3]

	Zero cross time (seconds)		
	Minimum value	Maximum value	Average value
Embodiment 1	0.31	0.40	0.36
Embodiment 2	0.45	0.47	0.46
Embodiment 3	0.35	0.46	0.38
Conventional Example	3.72	5.00	4.36
Comparative Example	1.41	1.54	1.47

(Heating conditions: 400 ± 5°C, holding for 30 seconds)

Tables 2 and 3 show the maximum time, minimum time and average time of the three measurements in each of the evaluation samples. As is apparent from Tables 2 and 3, it became clear that in each of the evaluation samples of Embodiments 1 to 3, at both of the heating temperatures of 380°C and 400°C the zero cross time is short and variations among the measurements are small, and that the evaluation samples show stable solder wettability. That is, it became clear that even when a high-temperature thermal history is added, the wettability by a solder is excellent. On the other hand, in the conventional example, the zero cross time was long and the variations among the measurements were large. In the comparative

example, there was observed a tendency that the zero cross time becomes long when a high-temperature thermal history is added.

Subsequently, in the above-described solder wettability evaluation test, some evaluation samples were subjected to heating treatment at higher 430 ± 5°C for 30 seconds and these samples were investigated. The results are described. The three evaluation samples of Embodiment 2, the conventional example and comparative example were used in this test. The conditions other than the heating conditions are the same as each of the above-described conditions. The results are shown in Table 4.

[Table 4]

	Zero cross time (seconds)		
	Minimum value	Maximum value	Average value
Embodiment 2	0.62	0.67	0.63
Conventional Example	5.00	5.00	5.00
Comparative Example	5.00	5.00	5.00

(Heating conditions: 430 ± 5°C, holding for 30 seconds)

As shown in Table 4, in the evaluation samples of the conventional example and the comparative example, the zero cross time was not less than 5 seconds in all cases and the solder wettability showed very bad results. On the other hand, in the case of Embodiment 2, the zero cross time was 0.63 seconds on the average and it became clear that the evaluation sample has excellent solder wettability even after the heat treatment at 430°C. From the above-described results of Tables 2 to 4, it became apparent that with a lead frame employing the palladium plating film in this embodiment, the junction is stable even when it is subjected to a high-temperature thermal history, with the result that the junction has excellent solder wettability.

This suggests that even in a case where a lead-free solder having a higher melting point than conventional solders and having a high reflow temperature during melting is used, the exfoliation phenomenon and problems such as junction failures do not occur in the junction of this embodiment. A lead frame having a palladium plating film of this embodiment permits thin-film designs of a palladium plating film and enables costs to be reduced.

Lastly, for the palladium plating film of Embodiment 2, the plating film composition was investigated. As a result, it became clear that germanium is co-deposited in the palladium of the parent phase in an amount of 4000 ppm. Incidentally, for the analysis method adopted, the amount of palladium contained in a prescribed amount of palladium film was measured by an ICP (inductively-coupled plasma) analysis.

WHAT IS CLAIMED IS:

1. An electronic part comprising: a chip having joining terminals; and a substratum having a chip-mounting section on which the chip is mounted via the joining terminals and packaging terminals by which the chip is mounted on a substrate, wherein at least any of a group consisting of said joining terminals of the chip, chip-mounting section of the substrate, and packaging terminals is/are formed with a germanium-containing palladium plating film.

2. The electronic part as defined in claim 1, wherein a nickel plating film has been formed as an undercoat for said palladium plating film.

3. The electronic part as defined in claim 1, wherein said palladium plating film has a thickness between 0.001 and 5μm, and a germanium content of the palladium plating film is between 1 and 10000ppm.

4. The electronic part as defined in claim 2, wherein said palladium plating film has a thickness between 0.001 and 5μm, and a germanium content of the palladium plating film is between 1 and 10000ppm.

5. The electronic part as defined in claim 1, wherein said electronic part is a package, which comprises any of a lead frame, an organic substrate, or a ceramic substrate.

6. The electronic part as defined in claim 2, wherein said electronic part is a package, which comprises any of a lead frame, an organic substrate, or a ceramic substrate.

7. The electronic part as defined in claim 3, wherein said electronic part is a package, which comprises any of a lead frame, an organic substrate, or a ceramic substrate.

8. The electronic part as defined in claim 4, wherein said electronic part is a package, which comprises any of a lead frame, an organic substrate, or a ceramic substrate.