

A MULTIMODE I/O SIGNALING CIRCUIT

Field of the Invention

This invention relates to a circuit used to provide I/O signals between a first and a second device. More particularly, this invention relates to a circuit that can be
5 configured to operate in one of multiple modes using one path through the circuit. Still more particularly, this invention relates to an I/O circuit in meter electronics of a Coriolis Mass flowmeter that minimizes the number of terminals needed in the meter electronics to support different secondary devices that operate in different modes.

Problem

10 It is known to use Coriolis effect mass flowmeters to measure mass flow and other information of materials flowing through a pipeline as disclosed in U.S. Patent No. 4,491,025 issued to J.E. Smith, et al. of January 1, 1985 and Re. 31,450 to J.E. Smith of February 11, 1982. These flowmeters have one or more flow tubes of a curved configuration. Each flow tube configuration in a Coriolis mass flowmeter has
15 a set of natural vibration modes, which may be of a simple bending, torsional, radial, or coupled type. Each flow tube is driven to oscillate at resonance in one of these natural modes. The natural vibration modes of the vibrating, material filled systems are defined in part by the combined mass of the flow tubes and the material within the flow tubes. Material flows into the flowmeter from a connected pipeline on the inlet
20 side of the flowmeter. The material is then directed through the flow tube or flow tubes and exits the flowmeter to a pipeline connected on the outlet side.

A driver applies a force to the flow tube. The force causes the flow tube to oscillate. When there is no material flowing through the flowmeter, all points along a flow tube oscillate with an identical phase. As a material begins to flow through the
25 flow tube, Coriolis accelerations cause each point along the flow tube to have a different phase with respect to other points along the flow tube. The phase on the inlet side of the flow tube lags the driver, while the phase on the outlet side leads the driver. Sensors are placed at two different points on the flow tube to produce sinusoidal signals representative of the motion of the flow tube at the two points. A
30 phase difference of the two signals received from the sensors is calculated in units of time.

The phase difference between the two sensor signals is proportional to the mass flow rate of the material flowing through the flow tube or flow tubes. The mass

flow rate of the material is determined by multiplying the phase difference by a flow calibration factor. This flow calibration factor is determined by material properties and cross sectional properties of the flow tube.

5 Meter electronics including a processor and connected memory receive the sensor signals and execute instructions to determine the mass flow rate and other properties of the material flowing through the tube. Th meter electronics can also use the signals to monitor the properties of Coriolis flowmeter components. The meter electronics can then transmit this information to a secondary processing device. It is also possible for the meter electronics to receive signals from the secondary device
10 for the purpose of modifying flowmeter operation. For purposes of the present discussion, a secondary processing device is any system capable of receiving signals from and/ or transmitting signals to the meters electronics. The actual functions and operation of secondary devices is not covered in the scope of this invention.

15 It is a problem in the Coriolis flow meter field in particular and other fields in general that different types of secondary processing devices may be connected to the electronics. Each different type of secondary processing device may communicate in one of several different modes. Some examples of different modes include but are not limited to digital signaling, 4-20 milliamp analog signaling, active discrete signaling, passive discreet signaling, active frequency signaling, and passive frequency
20 signaling. For each mode supported by the meter electronics or another electronic device in another field, the electronics must have at least one terminal and typically two terminals connected to the circuitry needed to support the mode.

The need for separate circuits for each mode supported by the electronics is a problem. If the electronics are to be adaptable to provide signals in different modes
25 to support different modes, an additional circuit must be added for each mode supported by the electronics. Each additional circuit adds to both the material cost and assembly cost of the electronics. Furthermore, unless a specific circuit for a specific mode is added, the specific mode cannot be supported by the meter electronics. There is a need in Input/Output (I/O) signaling art in general and in the
30 Coriolis flowmeter art in particular for a system that reduces the amount of circuitry in an I/O circuit while maximizing the number of modes supported by the circuitry.

SOLUTION

The above and other problems are solved and an advance in the art is achieved through the provision of an I/O signaling circuit that is capable of operating in a plurality of modes while using a single path through the circuitry to transmit
5 signals to and/or receive signals from a secondary device. This allows each I/O circuit in a device to operate in any one of a plurality of modes which reduces the number of circuits needed to provide I/O signaling between a first and a second device.

An I/O signaling circuit that is capable of operating in a plurality of modes while
10 using a single path through the circuit operates in the following manner. A power supply is connected to a positive output terminal. A variable impedance device, such as a transistor, is connected in the circuit between the positive terminal and a negative terminal. A second variable impedance device connects the negative terminal to a fixed resistor. The fixed resistor is then connected to ground.

15 The first variable impedance device can be opened or closed to complete a circuit between the positive and negative terminals inside the I/O circuit in order to control the voltage between the positive and negative terminals. The second variable impedance device controls the flow of current from the power supply to ground. The two variable impedance devices are controlled in the following manner to configure
20 the I/O signaling circuit to operate in a particular mode. A controller executes instructions that determine the mode in which signals are to be transmitted and generates signals that configure a circuit.

The controller generates a first signal that is applied to the first variable impedance device. The first signal causes the first variable impedance device to
25 complete or break a circuit which in turn controls the current flowing through the secondary device from the positive terminal to the negative terminal. In the preferred embodiment, the first signal is a digital signal that opens and closes a p-channel MOSFET transistor.

A second signal is also generated by the controller. The second signal is
30 applied to the second variable impedance. The second signal causes the second variable impedance device to change the amount of current that flows through the second variable impedance device into ground. As the current flows to ground, the

resistor connected to the second variable impedance device causes a voltage which is applied to an Operational Amplifier (Op-Amp) and is made available to an Analog to Digital (A/D) converter. The Op-Amp also receives the second signal which is an analog signal. The Op-Amp generates a control voltage which is then applied to the
5 second variable impedance device to control the current flowing from the power supply to the resistor. The first and second signals are varied by the controller to transmit or receive signals in a desired mode as set out below.

This invention is an integrated I/O signaling circuit capable of operating in one of a plurality of modes having a power receiving circuit that receives power, a high
10 potential terminal that connects to a load and a low potential terminal (254) that connects to the load. A first aspect of this invention is configuration circuitry through the I/O signaling circuit connecting said power receiving circuit to the high potential terminal, and the low potential terminal to provide a current to the high potential terminal and the low potential terminal over a single path through said configuration
15 circuitry wherein the configuration circuitry configures the single path to provide current in a one of the plurality of modes responsive to the configuration circuitry receiving an input.

A second aspect of this invention is that the configuration circuitry includes current flow control circuitry for controlling current flow between the power receiving
20 circuit and ground and voltage control circuitry for controlling the voltage between the high potential terminal and the low potential terminal.

Another aspect of this invention is that the current flow control circuitry includes a first resistor and a first transistor connected to the low potential terminal and an input of the first resistor.

25 Another aspect of this invention is that the current flow control circuitry also includes a pick-off proximate the input of the first resistor and an operational amplifier that receives an analog control signal from a processor and a voltage from the pick-off and generates a control voltage that is applied to a gate of the first transistor which controls the current flow through the first transistor.

30 Another aspect of this invention is that the current flow control circuitry also includes a first monitor path connected to the pick-off.

Another aspect of this invention is that the voltage control circuitry includes a second transistor connected between the high potential terminal and the low potential terminal that receives a digital input and establishes a circuit path between the high potential terminal and the low potential terminal.

5 Another aspect of this invention is that the voltage control circuitry also includes a first biasing resistor connected between the power receiving circuit and a gate of the second transistor to bias the second transistor and a positive rail.

Another aspect of this invention is that the voltage control circuitry also includes a second biasing resistor that receives the input signal from a processor and has an
10 output connected to the gate of the second transistor.

Another aspect of this invention wherein the second transistor is a source to drain transistor and the power receiving circuit includes a fuse connected between an output of the second transistor and the low potential terminal.

Another aspect of this invention is that the power receiving circuit includes
15 a diode that prevents current from flowing into a low impedance power supply connected to the power receiving circuit when said power supply is off.

Another aspect of this invention is that the plurality of modes include a 4-20 milliamp Output mode.

Another aspect of this invention is that the plurality of modes include a 4-20
20 milliamp Input mode.

Another aspect of this invention is that the plurality of modes include an active discrete output mode.

Another aspect of this invention is that the plurality of modes include a passive discrete output mode.

25 Another aspect of this invention is that the plurality of modes include an active frequency output mode.

Another aspect of this invention is that the plurality of modes include a passive frequency output mode.

Another aspect of this invention is that the plurality of modes include a digital
30 mode.

Another aspect of this invention is that the plurality of modes include an active input discrete mode.

Another aspect of this invention is that the plurality of modes include a passive discrete input mode.

Another aspect of this invention is that the plurality of modes include a passive frequency input mode.

- 5 Another aspect of this invention is that the plurality of modes include an active frequency input mode.

Another aspect of this invention is that the integrated I/O signaling circuit is incorporated into meter electronics of a Coriolis mass flowmeter.

- 10 These and other advantages of the present invention will be apparent from the drawings and a reading of the detailed description thereof.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a Coriolis flow meter common in the prior art;

FIG. 2 is a block diagram of the meter electronics in the Coriolis flowmeter;

FIG. 3 is a diagram of an I/O signaling circuit of this invention; and

- 15 FIG. 4 is a flow diagram of the process of configuring the I/O signaling circuit to operate in a selected mode.

DETAILED DESCRIPTION

Coriolis Flowmeter in General -FIG. 1

- 20 FIG. 1 illustrates a Coriolis flowmeter 5 comprising a flowmeter assembly 10 and meter electronics 20. Meter electronics 20 is connected to meter assembly 10 via leads 100 to provide density, mass flow rate, volume flow rate, totalized mass flow and other information over path 26. It should be apparent to those skilled in the art that the present invention can be used by any type of Coriolis flowmeter regardless of the number of drivers or the number of pick-off sensors.

- 25 Flowmeter assembly 10 includes a pair of flanges 101 and 101', manifold 102 and flow tubes 103A and 103B. Connected to flow tubes 103 A and 103 B are driver 104 and pick-off sensors 105 and 105'. Brace bars 106 and 106' serve to define the axes W and W' about which each flow tube 103A and 103B oscillates.

- 30 When flowmeter assembly 10 is inserted into a pipeline system (not shown) which carries the material being measured, material enters flowmeter assembly 10 through flange 101, passes through manifold 102 where the material is directed to

enter flow tubes 103A and 103B, flows through flow tubes 103 A and 103B and back into manifold 102 where it exits meter assembly 10 through flange 101'.

Flow tubes 103A and 103B are selected and appropriately mounted to manifold 102 so as to have substantially the same mass distribution, moments of inertia, and elastic modules about bending axes W-W and W'-W' respectively. The flow tubes extend outwardly from the manifold in an essentially parallel fashion.

Flow tubes 103A-B are driven by driver 104 in opposite directions about their respective bending axes W and W' and at what is termed the first out of bending fold of the flowmeter. Driver 104 may comprise one of many well known arrangements, such as a magnet mounted to flow tube 103A and an opposing coil mounted to flow tube 103B. An alternating current is passed through the opposing coil to cause both tubes to oscillate. A suitable drive signal is applied by meter electronics 20, via lead 110 to driver 104. The description of FIG. 1 is provided merely as an example of the operation of a Coriolis flowmeter and is not intended to limit the teaching of the present invention.

Meter electronics 20 receives the right and left velocity signals appearing on leads 111 and 111', respectively. Meter electronics 20 produces the drive signal on lead 110 which causes driver 104 to oscillate flow tubes 103A and 103B. The present invention as described herein, can produce multiple drive signals from multiple drivers. Meter electronics 20 process left and right velocity signals to compute mass flow rate and provide the validation system of the present invention. Path 26 provides an input and an output means that allows meter electronics 20 to interface with an operator.

Meter Electronics 20 in General - FIG. 2

FIG. 2 illustrates a block diagram of the components of an exemplary embodiment of meter electronics 20 which perform the processes related to the present invention. It will be noted by those skilled in the art that the components of meter electronics 20 shown are for exemplary purposes only. It is possible to use other types of processors and electronics in conjunction with the present invention. Processor 201 reads instructions for performing the various functions of the flowmeter including but not limited to computing mass flow rate of a material, computing volume flow rate of a material, and computing density of a material from a Read Only Memory (ROM) 220 via path 221. The data as well as instructions for performing the various

functions are stored in a Random Access Memory (RAM) 230. Processor 201 performs read and write operations in RAM memory 230 via path 231.

Paths 111 and 111' transmit the left and right velocity signals from flowmeter assembly 10 to meter electronics 20. The velocity signals are received by analog to digital (A/D) convertor 203 in meter electronic 20. A/D convertor 203 converts the left and right velocity signals to digital signals usable by processor 201 and transmits the digital signals over path 213 to I/O bus 210. The digital signals are carried by I/O bus 210 to processor 201. Driver signals are transmitted over I/O bus 210 to path 212 which applies the signals to digital to analog (D/A) convertor 202. The analog signals from D/A convertor 202 are transmitted to driver 104 via path 110.

Path 26 carries signals to secondary processing device 260 which allow meter electronics 20 and secondary processing device 260 to communicate. Path 26 includes paths 261 and 262 which are connected to positive potential terminal 253 and negative potential terminal 254 of I/O signaling circuit 250. I/O signaling circuit 250 is a circuit that provides I/O signals in meter electronics 20. One skilled in the art will recognize that meter electronics 20 may have more than one I/O signaling circuit 250. However, only one I/O circuit 250 is shown is for purposes of clarity. Furthermore, one skilled in the art will recognize that the functions and circuitry of I/O signaling circuit 250 can be provided by any combination of circuits that can provide the functionality of I/O signaling circuit 250.

I/O signaling circuit 250 receives and transmits signals to I/O bus 210 via path 214. One skilled in the electronic signaling arts will appreciate that I/O signaling circuit 250 can be used in other devices requiring I/O signaling and is not limited to use in Coriolis flowmeter electronics 20. Path 214 includes a power supply path 240, a first data path 241, and a second data path 242. One skilled in the art will recognize that the first and second data paths 241 and 242 can be a plurality of lines in bus 214 carrying data to circuit 250 or multiplexed signals over the same lines. Power supply path 240 is connected to positive potential terminal 253 by current flow control circuitry 251 and voltage control circuitry 252 of circuit 250. Negative potential terminal 254 is connected to current flow circuitry 251 and voltage control circuitry 252 to return the current flow from secondary processing device 260 to circuit 250.

Current flow control circuitry 251 is circuitry that controls the flow of current through I/O signaling circuit 250 to ground. Input 241 is received by current flow control circuitry 251 and causes the amount of current flowing to ground to be adjusted. Voltage control circuitry 252 receives second input 242 and adjusts the voltage applied to secondary processing device 260 in response to the received signal.

I/O signaling circuit 250 is different from other I/O circuits of the prior art in that circuit 250 can be configured in the below described manner to provide I/O signals in one of multiple modes supported by a system with current flowing through circuit 250 over a single path. This reduces the number of circuit paths through I/O signaling circuit 250 which in turn reduces the number of components needed to manufacture circuit 250. The configuration of I/O signaling circuit 250 is performed by processor 201 which executes instructions to generate and transmit the proper signals to configure I/O signaling circuit 250 for operation in the desired mode. The below description of an exemplary embodiment demonstrates how I/O signal can be configured to perform in a specific mode to using one path through circuit 250.

I/O Signaling Circuit 250- FIG. 3

FIG. 3 illustrates a preferred exemplary embodiment of I/O circuit 250. One skilled in the art will recognize that there are other possible circuit configurations that can be used to gain the same results. I/O signaling circuit 250 receives power over path 300 from a power supply. In this embodiment, the power supply is a unipolar power supply.

Path 300 passes through diode 301 which prevents current from flowing into the power supply when the power supply is off. Diode 301 is a conventional diode such as diode 1N4001 produced by Motorola Corp. Path 300 is then connected to the terminal with the most positive potential, positive potential terminal 253. A second terminal is the most negative potential terminal and is named negative potential terminal 254. Positive potential terminal 253 and negative potential terminal 254 connect to secondary processing device 260 to allow current to flow from I/O signaling circuit 250, through secondary processing device 260 and back to circuit 250. Those skilled in the art will recognize that can also flow in the opposite direction.

A first variable impedance device 310 is connected between positive potential terminal 253 and negative potential terminal 254 inside I/O circuit 250. In this exemplary embodiment, first variable impedance device is a p-channel MOSFET transistor such as transistor 4P06 produced by Motorola Corp.

5 First variable impedance device 310 is connected to path 300 via path 309 and thermal protection element 312 via path 311. Thermal protection element 312 protects the circuitry from over current as described below. Thermal protection element 312 is an auto-resettable fuse such as part # SMD050 produced by Raychem. The output of thermal protection element 312 is connected to the path 313.

10 In this embodiment, voltage control circuitry 252 is provided by first variable impedance device 310. A digital signal is applied by the processor 201 via path 330 to open and close variable impedance device 310. Resistor 305 is connected between path 300 and 330. Path 330 flows through resistor 325. Resistors 305 and 325 bias variable impedance device from path 300. Resistors 305 and 325 are
15 conventional resistors such as a ten Kohm metal film. It is possible to use many different strength resistor in the present invention.

Negative potential terminal 254 is also connected to comparator 340 via path 335. Comparator 340 senses the voltage level present at terminal 254 with respect to terminal 253. Path 335 passes through comparator 340 and carries the signals to
20 I/O bus 210 via path 391 and transmitted to processor 201.

A second variable impedance device 345 is connected to path 335 that returns from negative potential terminal 254. In this exemplary embodiment, second variable impedance device 345 is a n-channel MOSFET transistor. Resistor 350 is connected between second variable impedance device via enhancement mode path 349 and
25 ground.

Pick-off path 355 provides the voltage across resistor 350 to Op-Amp 360. Pick-off path 355 also provides the voltage across resistor 350 to a monitor(not shown). The monitor (Not Shown) is an analog to digital convertor that converts the voltage received over path 355 into digital signals that can be read by processor 201.
30 The digital signals are then transmitted to processor 201 via I/O bus 210.

Op-amp 360 receives an analog control signal from the processor over path 362 and the voltage across resistor 350 over path 355. Op- Amp 360 compares the



received signal with the voltage from resistor 350 and generates a control voltage that is applied to second impedance device 345 via path 361. The control voltage controls the amount of current that flows through second impedance device 345 to ground.

5 Second variable impedance device 345 and the attached circuitry are the current flow control circuitry 251 of FIG. 2. The analog signal applied to Op-Amp 260 is converted to a voltage that can be applied to second variable impedance device 345. The first and second variable impedance devices 310 and 345 are then adjusted by the signals from the processor to operate in one selected mode.

10 I/O signaling circuit 250 can be configured in the following modes by applying the following signals to the above described circuitry. The following examples are not meant to limit the functionality of I/O circuit 250. It is left to those skilled in the art to program processor 201 to operate in modes other than the exemplary modes given below.

15 A first mode that I/O signaling circuit 250 can be configured to provide is an analog 4-20 milli-Amp output. In order to provide the 4-20 milliamp output, processor 201 does not apply a signal to first variable impedance device 310 which causes first variable impedance device 310 to remain open. The processor 201 applies a scaled, linear variable voltage to Op-Amp 360 which creates a control voltage that is applied to second variable impedance device which adjusts the current flowing from the power
20 supply to ground. The strength of the signal is adjusted to encode the data in the current flowing through secondary processing device 260. This allows processor 201 to change the current flowing from the positive potential terminal 253 to the negative potential terminal 254 and through secondary processing device 260. Secondary processing device 260 can then read the current being applied to determine the data
25 being transmitted.

I/O signaling system can also be used as a 4-20 milli-Amp input. To configure circuit 250 to operate as a 4-20 milli-Amp input, processor 201 does not apply a signal to first variable impedance device 310. The lack of a signal cause the first variable impedance device to remain open. Processor 250 applies a constant maximum
30 voltage signal to Op-Amp 340 which causes a constant control voltage to be generated and applied to second variable impedance device 345. This allows the current flowing to be limited by 250, but controlled by secondary processing device



260. Processor 250 receives current flow over path 335 from negative potential terminal 254 and current flow received contains the data from secondary processing device 260.

Discrete data is a mechanism for indicating a digital state. A discrete value is a one or a zero in digital terms and is indicated by the voltage across terminal 253 and 254 through secondary processing device 260. I/O signaling circuit 250 can be employed to encode discrete data. In order to provide an active discrete input mode, processor 201 applies a constant maximum voltage to Op-Amp 360 which in turn generates a constant control voltage over second variable impedance device 345. The discrete value is then applied by asserting or de-asserting a signal to first variable impedance device 310. The signal causes first variable impedance device 310 to open and close which changes the voltage state between positive potential terminal 253 to negative potential terminal 254 presented to secondary processing device 260. The voltage indicates the data being transmitted. I/O signaling circuit 250 can also be configured in operate in an active discrete input mode for receiving data by applying a maximum voltage signal to Op-Amp 360 to generate a constant control voltage to second variable impedance device 345. Data is then detected by the voltage detected over path 335 by comparator 340.

In a passive discrete output mode, processor 201 applies 0 voltage to Op-Amp 360 which generates a control voltage that prevents current from flowing to ground. Data is encoded by asserting or de-asserting a signal applied to first variable impedance device 310 to open or close the first variable impedance device 310. I/O signaling circuit 250 can also be configured to operate in a passive discrete input mode for receiving data by processor 201 applying a 0 voltage signal to Op-Amp 360 to generate a constant control voltage for second variable impedance device 345. Data is then detected on the current received over path 335 through Op-Amp 340.

I/O signaling circuit 250 can also be configured to operate in active and passive frequency input and output modes. In a frequency mode, the data is a n encoded analog value. Processor 201 configures I/O circuit 250 to operate in an active frequency output mode in the following manner. Processor 201 applies a maximum voltage to second variable impedance device 345. In order to encode data for secondary processing device 260, processor 201 applies a frequency signal to first

variable impedance device 310 which changes the voltage across secondary processing device 260. I/O signaling circuit 250 can also be configured in operate in an active frequency input mode for receiving data by applying a maximum voltage signal to Op-Amp 360 to produce a constant control voltage for second variable
5 impedance device 345. Data is then detected on the current received over path 335 through comparator 340.

Processor 201 can also configure I/O circuit 250 to operate in a passive frequency output mode. Processor 201 applies a 0 volt signal to second variable impedance device 345. In order to encode data into the current applied to secondary
10 processing device 260, processor 201 applies a frequency signal to first variable impedance device 310. I/O signaling circuit 250 can also be configured in operate in a passive frequency input mode for receiving data by applying a 0 voltage signal to Op-Amp 360 to generate a constant control voltage for second variable impedance device 345. Data is then detected on the current received over path 335 through Op-
15 Amp 340.

I/O signaling circuit 250 can also be configured to transmit and receive digital data. One such digital protocol is the Bell 202 digital communications protocol. In order to configure I/O signaling circuit to operate in the digital mode, processor 201 does not apply a signal to first variable impedance device 310 to prevent first
20 impedance device 310 from completing a circuit between positive potential terminal 253 and negative potential terminal 254. A scaled, linear variable signal is applied to Op-Amp 345 with 1200Hz/ 2200Hz data superimposed on the signal. Transmit data is received over path 335 through comparator 340.

Method for Configuring an I/O circuit- FIG. 4.

FIG. 4 illustrates the operational steps taken by processor 201 in a process for configuring I/O signaling circuit 250. Process 400 begins in step 401 by determining which mode I/O signaling circuit 250 is to support. In step 402 the signals needed to configure the circuit are applied to I/O signaling circuit 250. In step 403, processor 201 determines whether the mode to be supported is an input or an output mode. If
25 the mode to be supported is an input mode, processor 201 reads the pertinent signals from I/O signaling circuit 250 in step 420. Step 420 is repeated until the mode of circuit 250 is changed by processor 201.
30

If the signaling mode to be supported is an input mode, steps 410-412 are executed. In step 410, processor 201 receives the data to be output. The signal encoded data is generated in step 411 and applied to I/O signals circuit 250 in step 412. Steps 410-412 are repeated until circuit 250 is configured to operate in another mode.

The above is a description of an I/O signaling circuit having a single path through the circuit that can be configured to operate in one of a plurality of modes. It is expected that those skilled in the art can and will design alternative I/O signaling circuits that infringe on this invention as set forth in the claims below either literally or through the Doctrine of Equivalents.



What is Claimed is:

1. An integrated I/O signaling circuit (250) capable of operating in one of a plurality of modes having a power receiving circuit (300) that receives power, a high potential terminal(253)that connects to a load and a low potential terminal (254) that connects to a load, said I/O signal circuit comprising:

5 configuration circuitry (251-252) through said I/O signaling circuit (250) connecting said power receiving circuit to said high potential terminal(253), and said low potential terminal (254) to provide a current to said high potential terminal (253) and low potential terminal (254) over a single path through said configuration circuitry (252) wherein said configuration circuitry configures said single path to provide current
10 in a one of said plurality of modes responsive to said configuration circuitry receiving an input.

2. The integrated I/O signaling circuit (250) of claim 1 wherein said configuration circuitry (254) comprises:

current flow control circuitry (251) for controlling current flow between said power receiving circuitry and ground; and

5 voltage control circuitry (252) for controlling the voltage between said high potential terminal (253) and said low potential terminal (254).

3. The integrated I/O signaling circuit (250) of claim 2 wherein said current flow control circuitry (251) comprises:

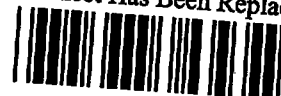
a first resistor (350); and

a first transistor (345) connected to said low potential terminal and an input of
5 said first resistor.

4. The integrated I/O signaling circuit (250) of claim 3 wherein said current flow control circuitry further comprises:

a pick-off (355) proximate said input of said first resistor (350); and

an operational amplifier (360) that receives an analog control signal (362) and
5 a voltage (354) from said pick-off (355) and generates a control voltage that is applied





to a gate of said first transistor which controls the current flow said through said first transistor (345).

5. The integrated I/O signaling circuit (250) of claim 4 wherein said current flow control circuitry further comprises:

a first monitor path (357) connected to said pick-off (355).

6. The integrated I/O signaling circuit (250) of claim 2 where said voltage control circuitry (252) comprises:

a second transistor (310) connected between said high potential terminal (253) and said low potential terminal (254) that receives a digital input and establishes a circuit path (309) between said high potential terminal (253) and said low potential terminal (254).

7. The integrated I/O signaling circuit (250) of claim 6 wherein said voltage control circuitry (252) further comprises:

a first biasing resistor (305) connected between said power receiving circuitry (300) and a gate of said second transistor (310) to bias said second transistor (310) and a positive rail.

8. The integrated I/O signaling circuit (250) of claim 7 wherein said voltage control circuitry (252) further comprises:

a second biasing resistor (325) that receives said input signal and has an output connected to said gate of said second transistor (310).

9. The integrated I/O signaling circuit of claim 6 wherein said second transistor (310) is a source to drain transistor and said power receiving circuitry further comprises:

a fuse (312) connected between an output of said second transistor (310) and a said low potential terminal (253).





10. The circuit of claim 1 wherein said power receiving circuitry comprises:
a diode (301) that prevents current from flowing into a low impedance power supply connected to said power receiving circuitry (300) when said power supply is off.

11. The circuit of claim 1 wherein said plurality of modes includes:
a 4-20 milliamp Output mode.

12. The circuit of claim 1 wherein said plurality of modes includes:
a 4-20 milliamp Input mode.

13. The circuit of claim 1 wherein said plurality of modes includes:
an active discrete output mode.

14. The circuit of claim 1 wherein said plurality of modes includes:
a passive discrete output mode.

15. The circuit of claim 1 wherein said plurality of modes includes:
an active frequency output mode.

16. The circuit of claim 1 wherein said plurality of modes includes:
a passive frequency output mode.

17. The circuit of claim 1 wherein said plurality of modes includes:
a digital mode.

18. The circuit of claim 1 wherein said plurality of modes includes:
an active input discrete mode.

19. The circuit of claim 1 wherein said plurality of modes includes:
a passive discrete input mode.





20. The circuit of claim 1 wherein said plurality of modes includes:
a passive frequency input mode.

21. The circuit of claim 1 wherein said plurality of modes includes:
an active frequency input mode.

22. The circuit of claim 1 wherein said integrated I/O signaling circuit (250) is
incorporated into meter electronics (20) of a Coriolis mass flowmeter (5).

23. A method (400) for configuring an integrated I/O signaling circuit (250) to
operate in one of a plurality of modes comprising the steps:

5 applying (402) a first input to a first transistor (310) connected between a high
potential terminal (253) and a low potential terminal (254) to control voltage between
said high potential terminal (253) and low potential terminal (254);

 applying (402) a second input to a gate of a second transistor (345) connected
between said low potential terminal (253) and a resistor (353) connected to ground
wherein said second transistor (345) controls the flow of current received from a power
supply (300) into ground; and

10 applying (412) power to said circuit responsive to said circuit receiving said first
and second inputs.

24. The method of claim 23 further comprising the steps of:

 determining (401) which one of a plurality of modes is to be provided by said
integrated I/O circuit (250);

5 generating (411) a first input with a processor responsive to a determination of
said one of said plurality of modes to be provided;

 generating (411) a second input with a processor responsive to a determination
of said one of said plurality of modes to be provided; and

 transmitting (412) said first input to said first transistor and said second input
to said transistor.

