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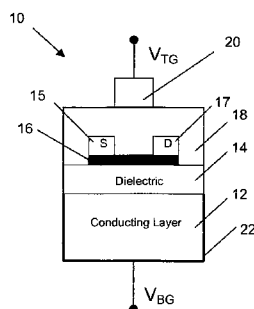


FIGURE 1A

(57) Abstract: The disclosed memory cell (10) comprises a graphene layer (16) having controllable resistance states representing data values of the memory cell (10). In one exemplary embodiment a non-volatile memory is provided by having a ferroelectric layer (18) control the resistance states. In the exemplary embodiment, binary '0's and '1's are respectively represented by low and high resistance states of the graphene layer (16), and these states are switched in a non-volatile manner by the polarization directions of the ferroelectric layer (18).