Title: A Planarization Technique for DRAM Cell Capacitor Electrode.

Abstract of the Invention.

A method of forming a DRAM includes forming a transfer FET on a substrate, the FET having a gate on a gate oxide layer above the substrate and a first and second source/drain region in the substrate on either side of a channel region under the gate. The first and second source/drain regions are typically exposed or nearly exposed in a spacer etch process. A silicon nitride etch stop layer is deposited over the entire structure and then a thick layer of oxide is deposited on the device. Chemical mechanical polishing is performed to provide a planar surface on the thick oxide layer. An opening is formed through the thick layer of oxide above the first source/drain region, stopping at the etch stop layer. The etch stop layer is removed within the opening in the thick layer of oxide and the underlying thin oxide layer is etched. A capacitor electrode can then be formed in contact with the exposed portion of the first source/drain region. A similar self-aligned method can be used to form the bit line contact for the device using the etch stop layer as a stop for the bit line contact etch. Practice of the method provides a manufacturing method having improved reliability and ease of use.

(Figure 10)