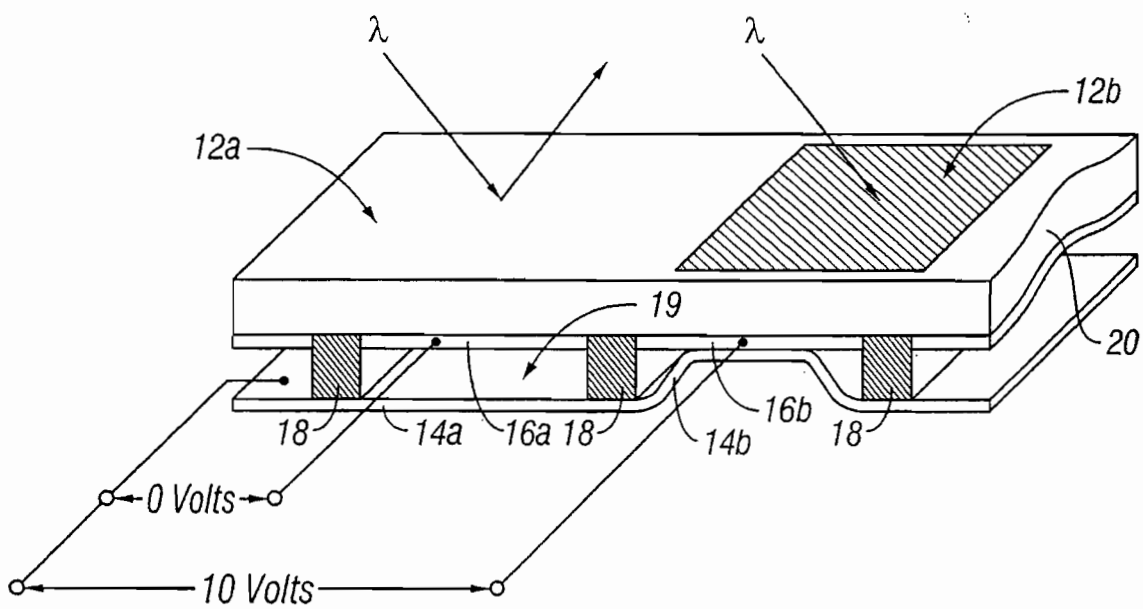


FIG. 1

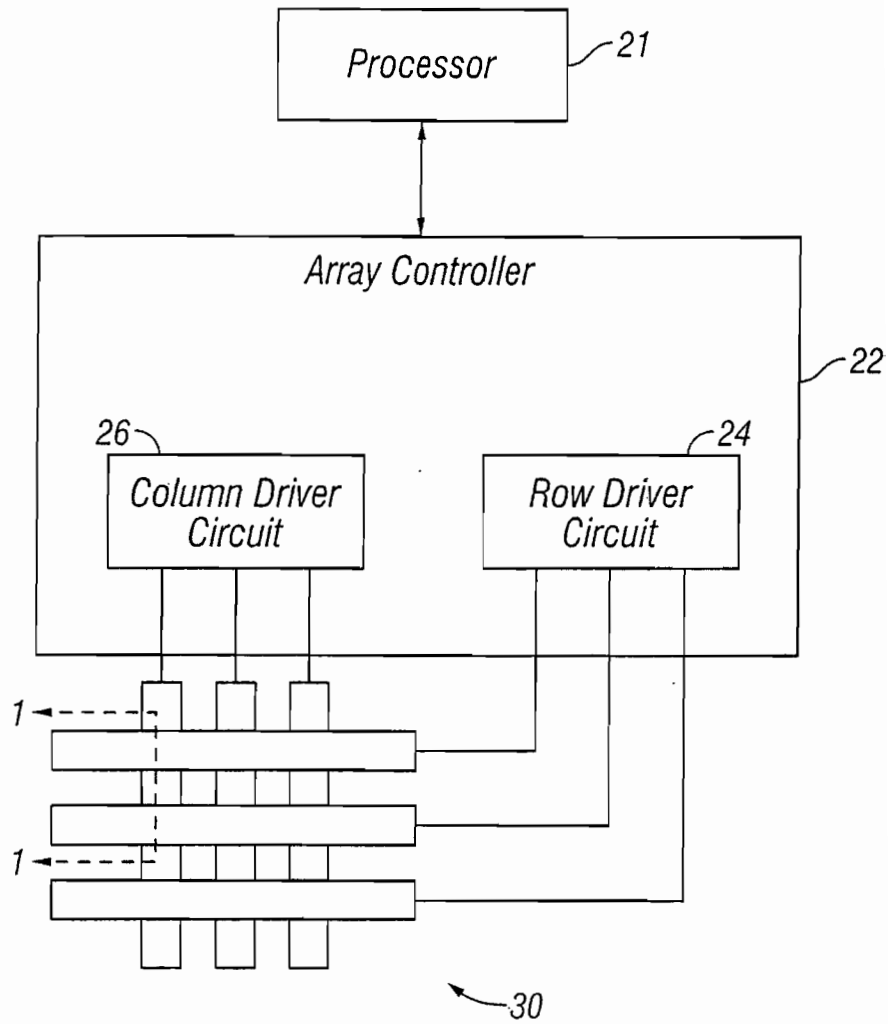

Processor
21
Array Controller
22
26
Column Driver Circuit
24
Row Driver Circuit
1
1
30

FIG. 2

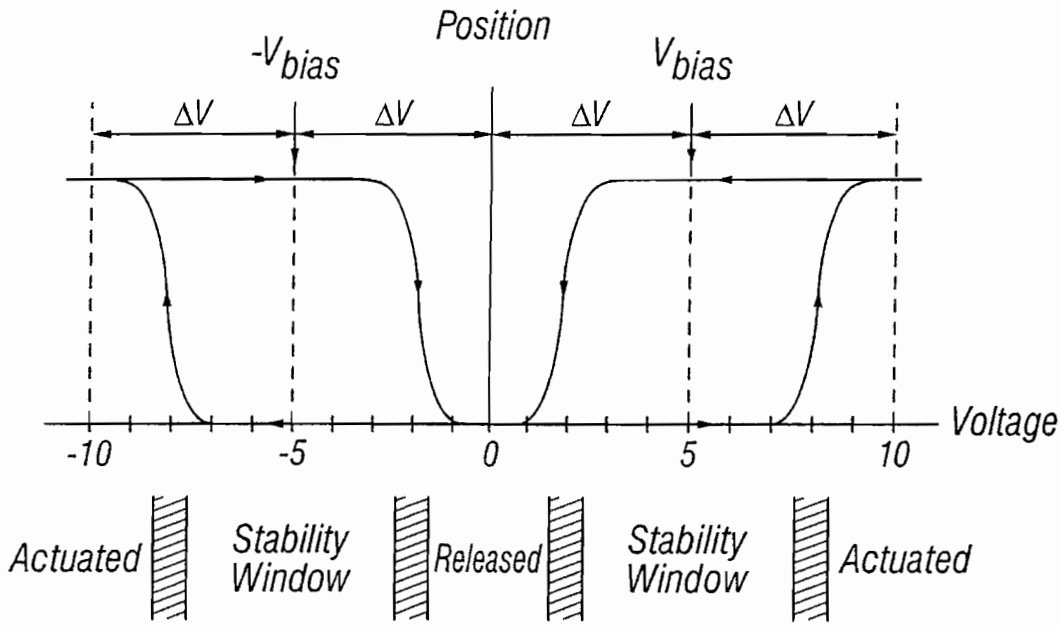


FIG. 3

Row Output Signals	Column Output Signals: $+V_{bias}$	Column Output Signals: $-V_{bias}$
0	Stable	Stable
$+\Delta V$	Release	Actuate
$-\Delta V$	Actuate	Release

FIG. 4

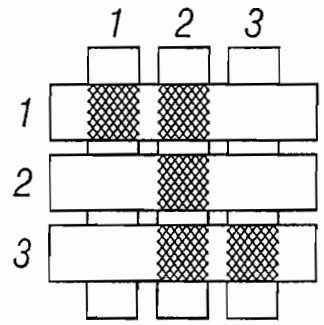

1
2
3
1
2
3

FIG. 5A

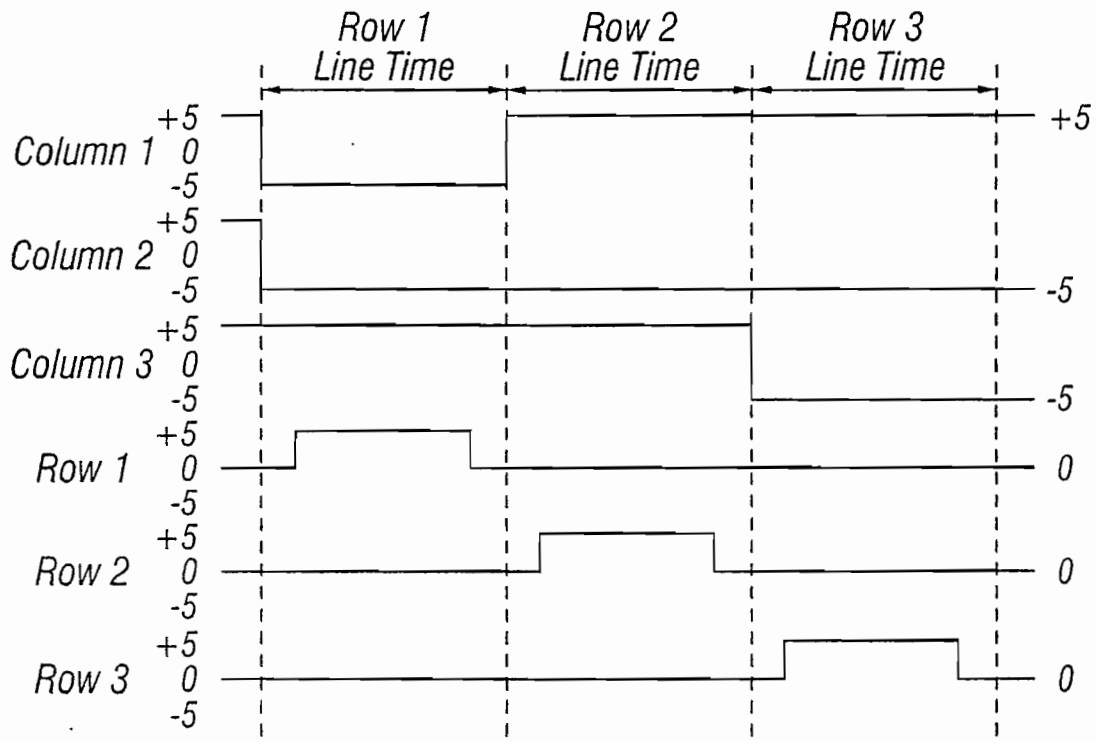

Row 1 Line Time
Row 2 Line Time
Row 3 Line Time
Column 1
Column 2
Column 3
Row 1
Row 2
Row 3
+5
0
-5
+5
-5
-5
0
0
0

FIG. 5B

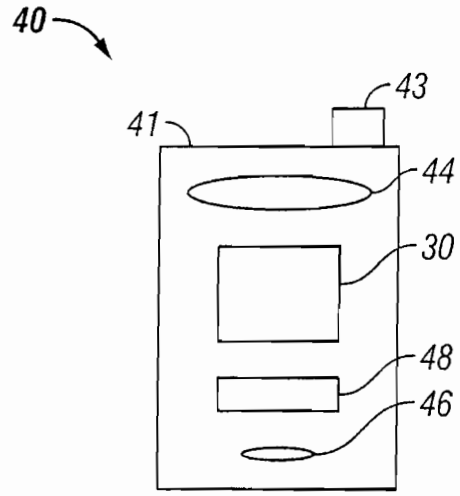

40
41
43
44
30
48
46

FIG. 6A

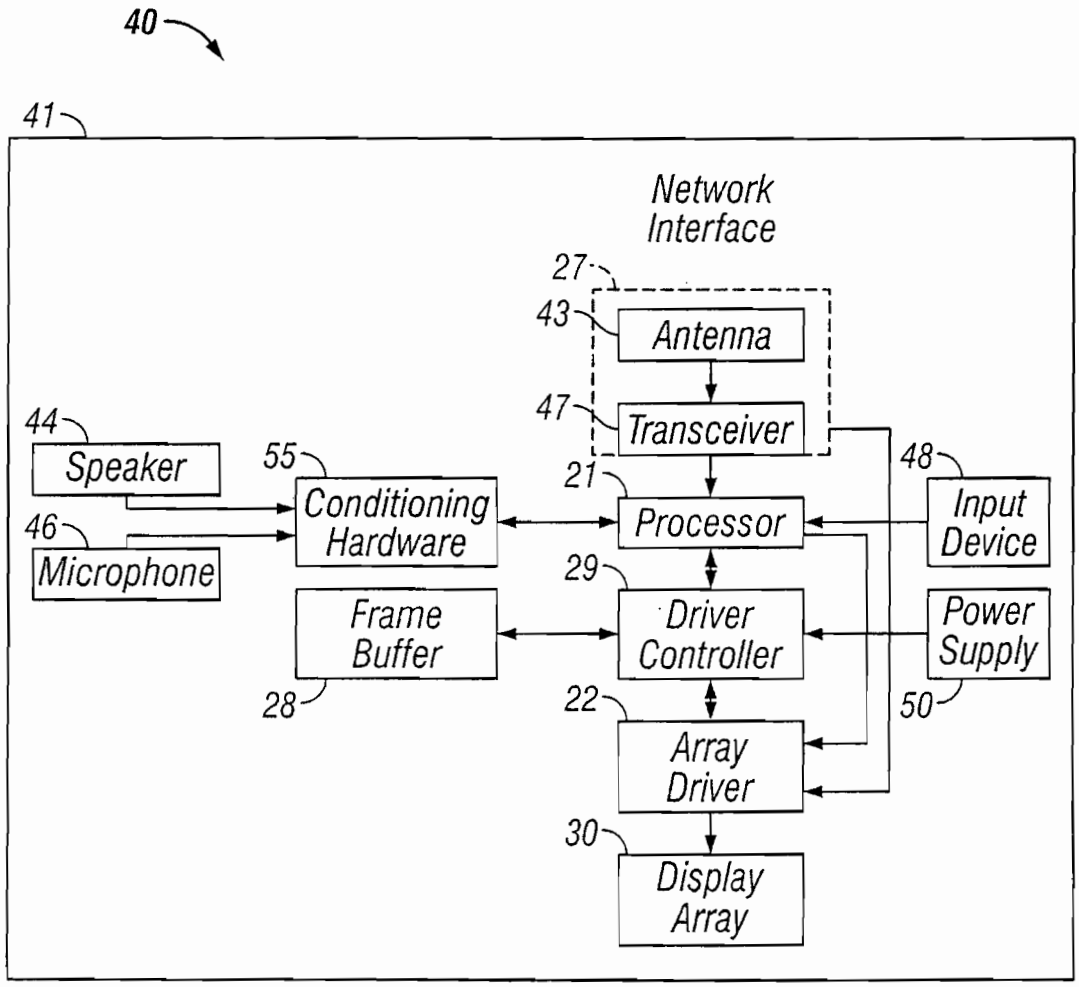

40
41
Network Interface
27
43
Antenna
47
Transceiver
44
Speaker
55
Conditioning Hardware
21
Processor
48
Input Device
46
Microphone
29
Driver Controller
Frame Buffer
Power Supply
28
22
50
Array Driver
30
Display Array

FIG. 6B

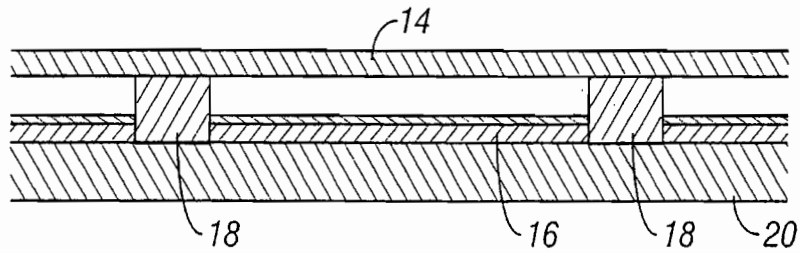


FIG. 7A

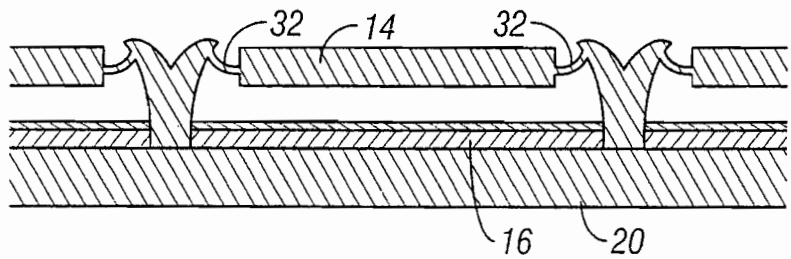


FIG. 7B

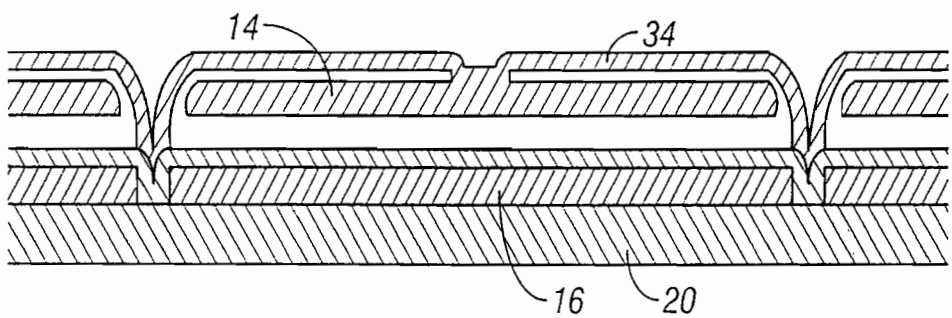


FIG. 7C

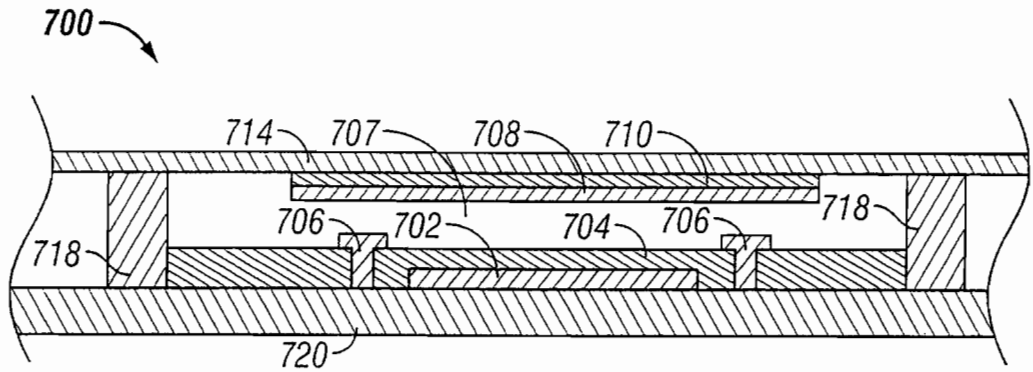


FIG. 8A

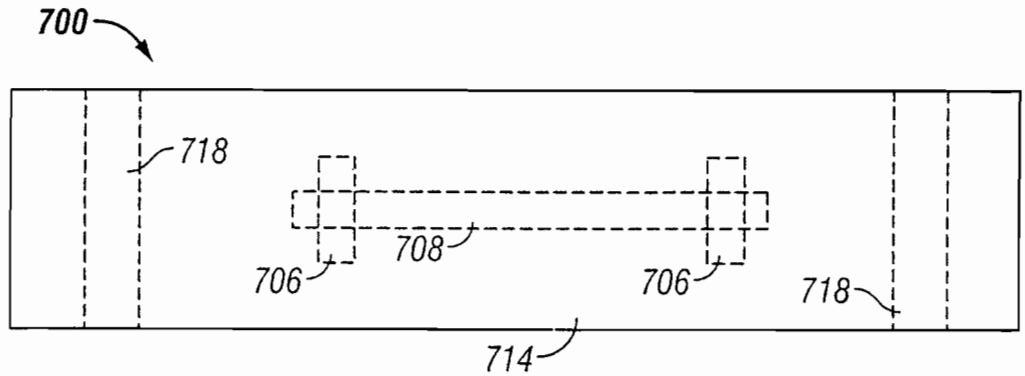


FIG. 8B

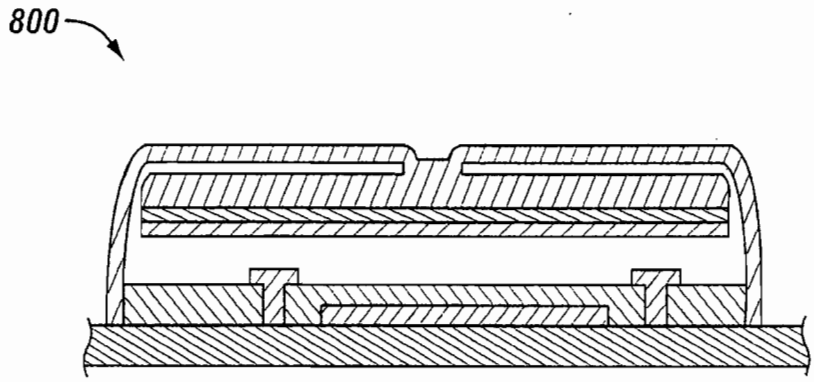


FIG. 9

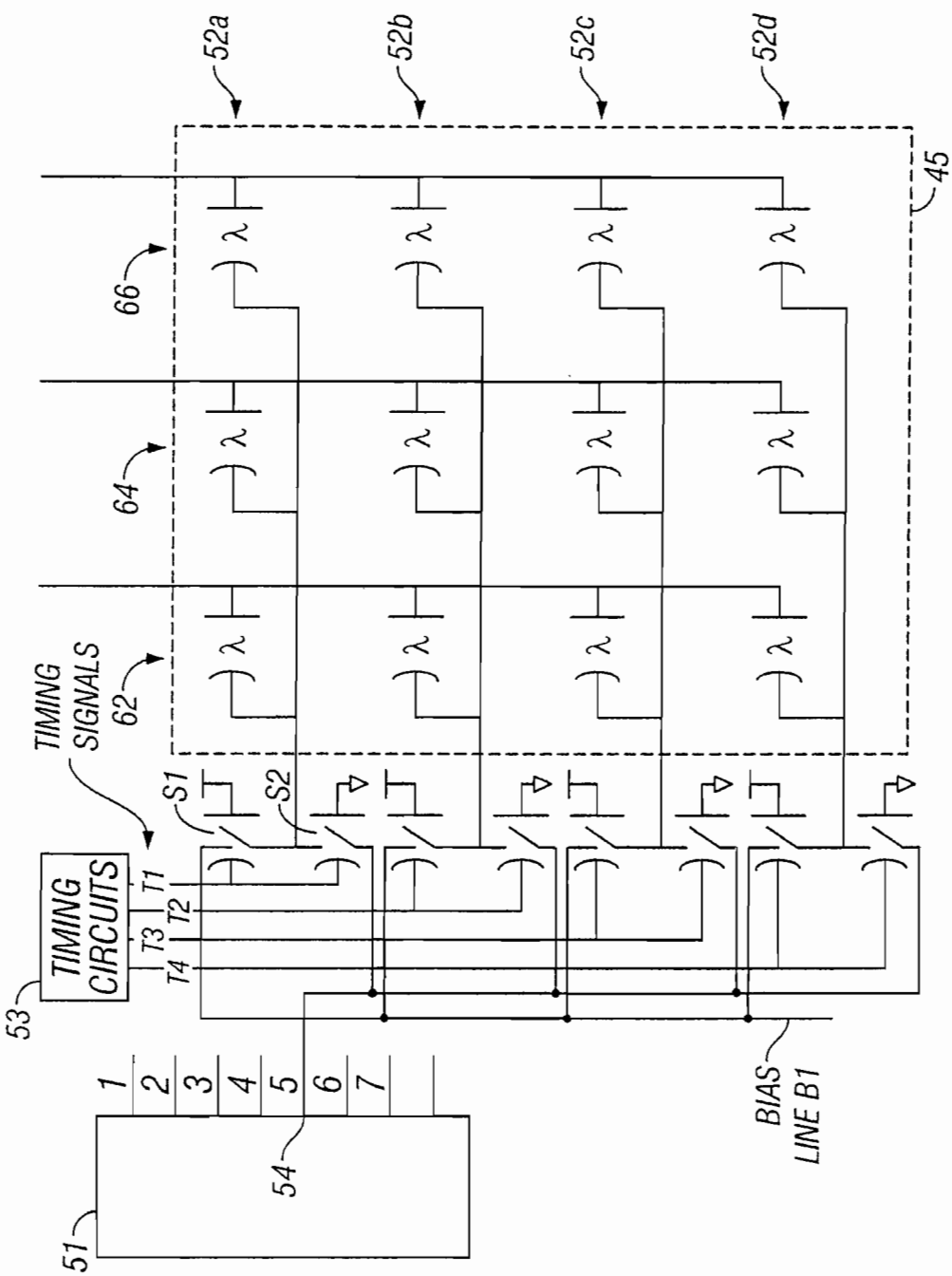

52a
52b
52c
52d
45
66
64
62
λ
TIMING SIGNALS
S1
S2
TIMING CIRCUITS
T1
T2
T3
T4
53
1
2
3
4
5
6
7
54
51
BIAS LINE B1

FIG. 10A

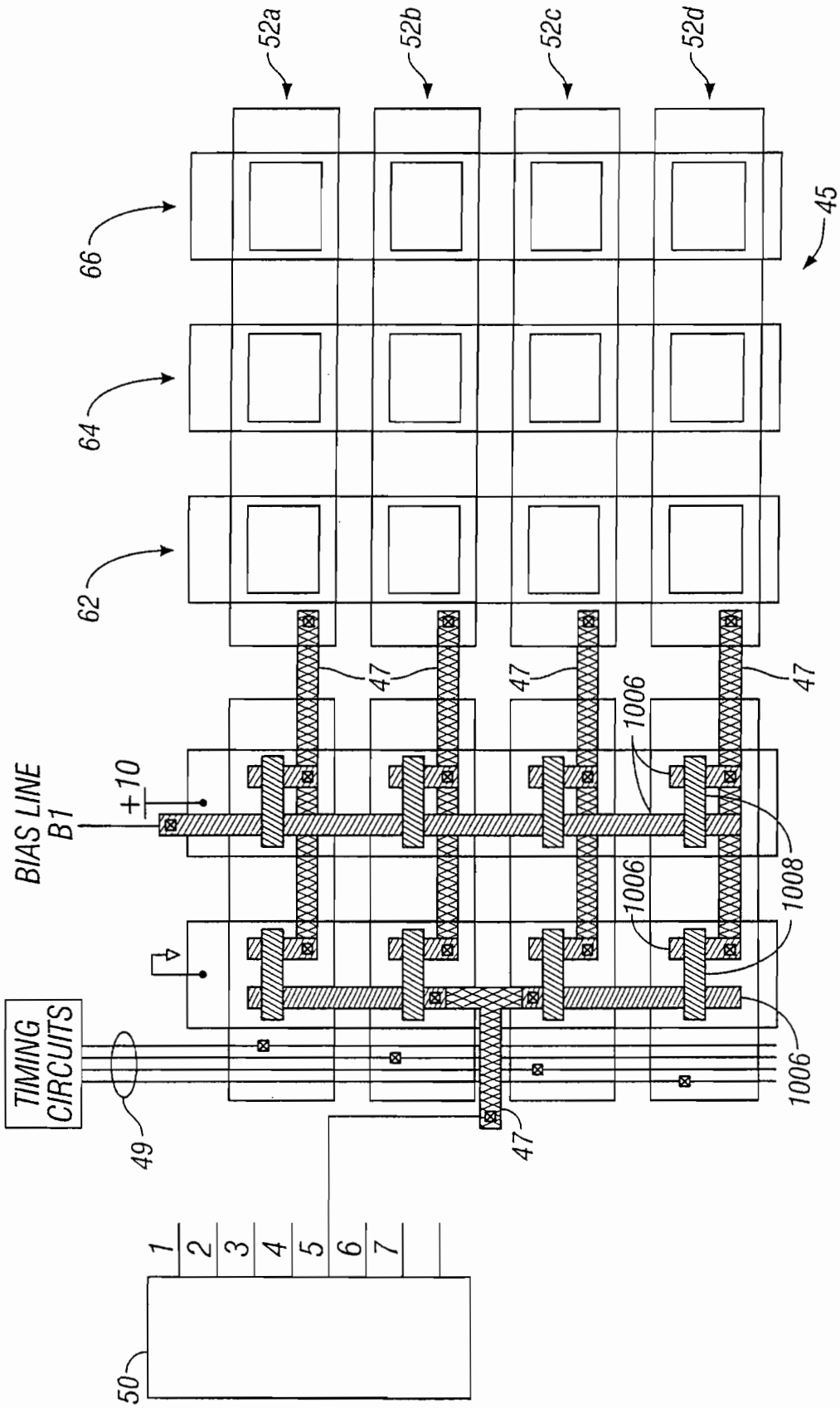

52a
52b
52c
52d
45
66
64
62
47
47
47
1006
1006
1006
1008
BIAS LINE
B1
+10
TIMING
CIRCUITS
49
47
1
2
3
4
5
6
7
50

FIG. 10B

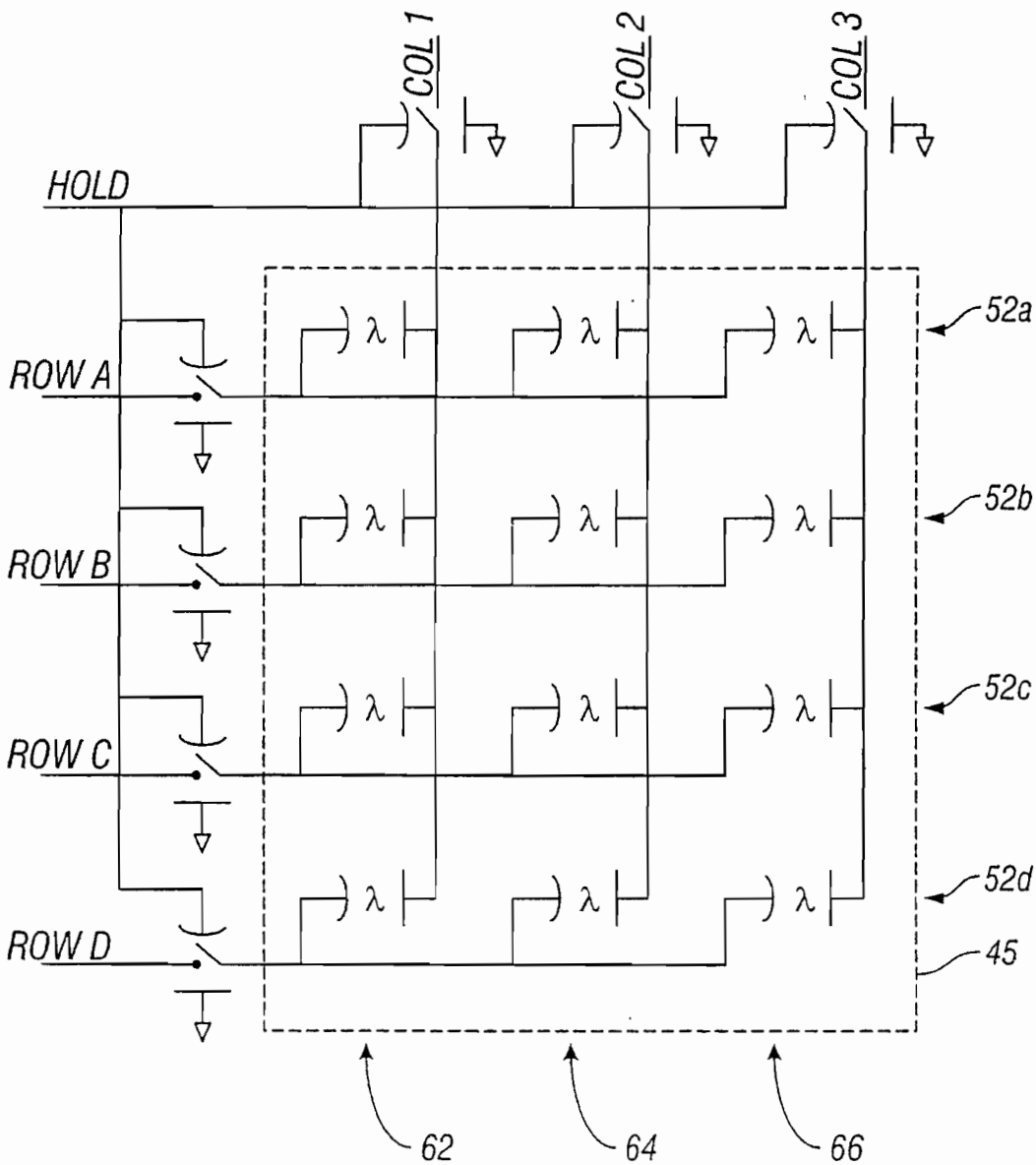

COL 1
COL 2
COL 3
HOLD
ROW A
ROW B
ROW C
ROW D
λ
52a
52b
52c
52d
45
62
64
66

FIG. 11A

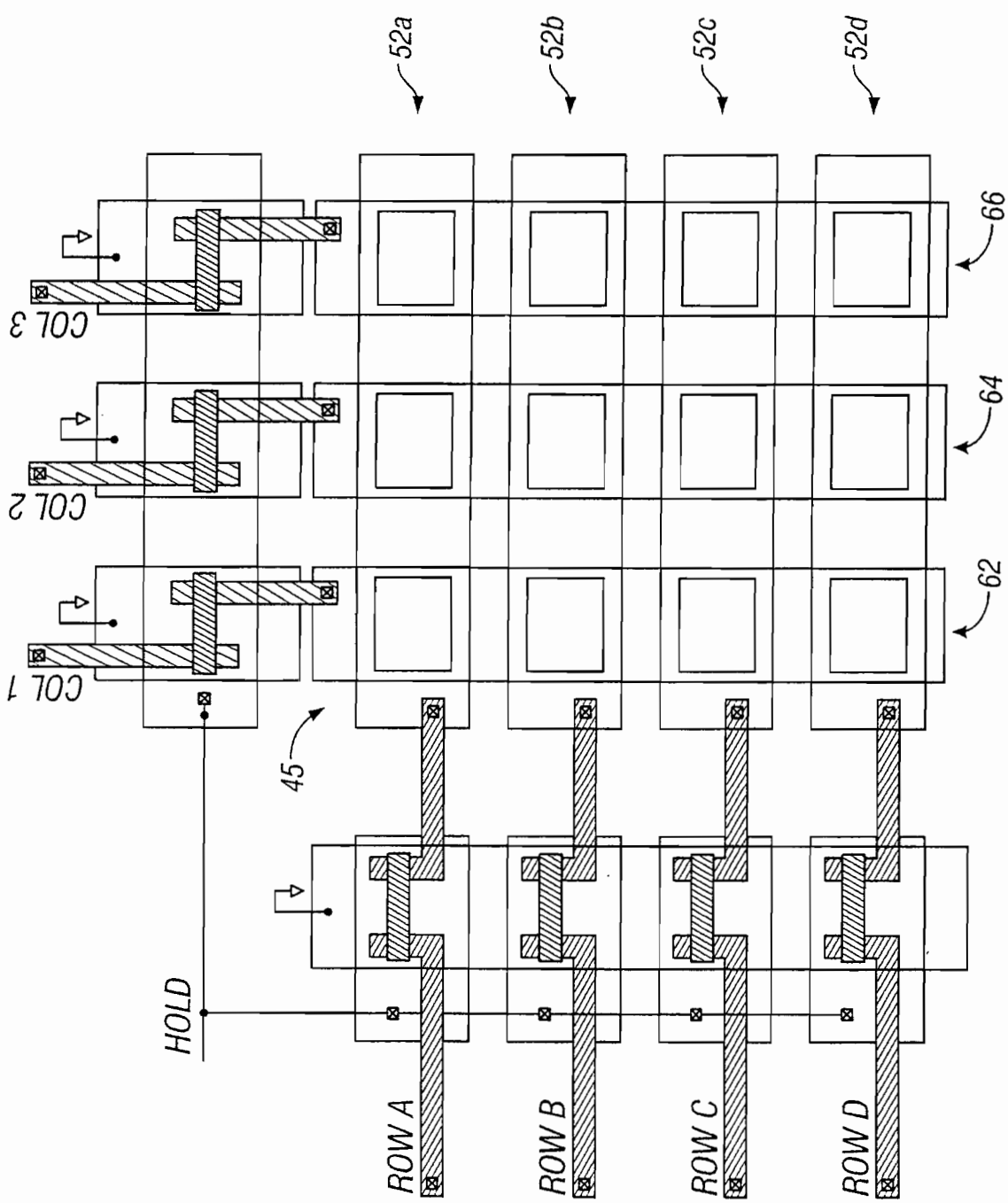

52a
52b
52c
52d
66
64
62
COL 3
COL 2
COL 1
45
HOLD
ROW A
ROW B
ROW C
ROW D

FIG. 11B

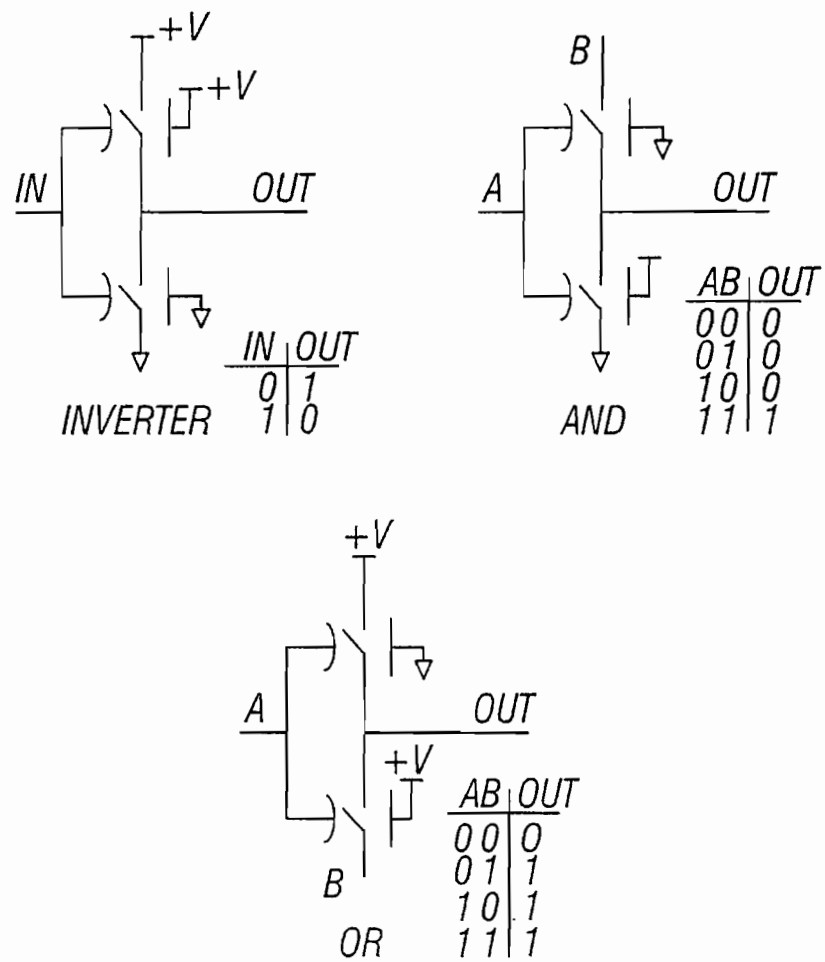

+V
+V
IN
OUT
IN OUT
0 1
1 0
INVERTER
B
A
OUT
AB OUT
0 0 0
0 1 0
1 0 0
1 1 1
AND
+V
A
OUT
+V
B
AB OUT
0 0 0
0 1 1
1 0 1
1 1 1
OR

FIG. 12