

2003022134
16/04/03



162162

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
6 June 2002 (06.06.2002)

PCT

(10) International Publication Number
WO 02/45157 A1

(51) International Patent Classification⁷: **H01L 21/8246**,
27/115

Francisco, CA 94109 (US). **DERHACOBIAN**, Narbeh;
1518 Williams Avenue, Belmont, CA 94002 (US). **WU**,
Yider; 1685 Marco Drive, San Jose, CA 95131 (US).

(21) International Application Number: PCT/US01/24829

(74) Agent: **RODDY, Richard, J.**; Advanced Micro Devices,
Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-
3453 (US).

(22) International Filing Date: 7 August 2001 (07.08.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/723,635 28 November 2000 (28.11.2000) US

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM,
HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK,
LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX,
MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL,
TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(71) Applicants: **ADVANCED MICRO DEVICES, INC.**
[US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA
94088-3453 (US). **FUJITSU LIMITED** [JP/JP]; 1-1,
Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi,
Kanagawa 211 (JP).

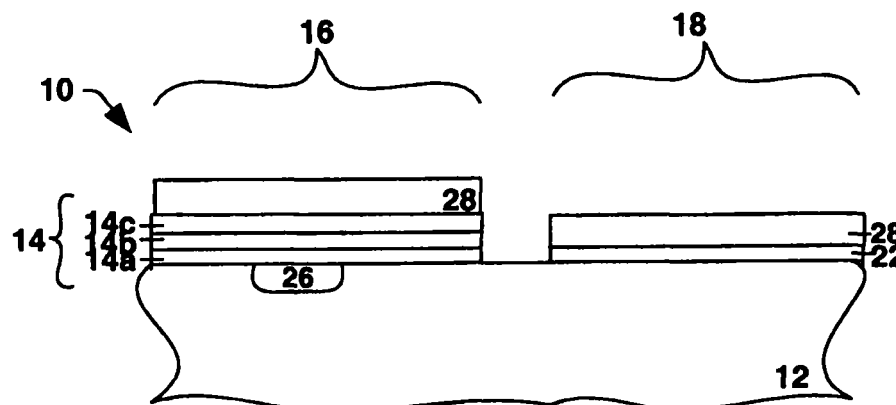
(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian
patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European
patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE,
IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF,
CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD,
TG).

(72) Inventors: **RAMSBEY, Mark, T.**; 402 Cumulus Av-
enue, Sunnyvale, CA 94087 (US). **YANG, Jean, Y.**; 125
Connemara Way, #17, Sunnyvale, CA 94087 (US). **SHI-**
RAIWA, Hidehiko; 1208 Valley Quail Circle, San Jose,
CA 95120 (US). **VAN BUSKIRK, Michael, A.**; 18653
Vessing Road, Saratoga, CA 95070 (US). **ROGERS,**
David, M.; 665 Endicott Drive, Sunnyvale, CA 94087
(US). **SUNKAVALLI, Ravi**; 2264 Edsel Drive, Milpitas,
CA 95035 (US). **WANG, Janet**; 1999 Broadway #42, San

Published:
— with international search report

For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: SIMULTANEOUS FORMATION OF CHARGE STORAGE AND BITLINE TO WORLDLINE ISOLATION



(57) Abstract: One aspect of the present invention relates to a method of forming a non-volatile semiconductor memory device, involving the sequential or non-sequential steps of forming a charge trapping dielectric (14) over a substrate (12), the substrate (12) having a core region (16) and a periphery region (18); removing at least a portion of the charge trapping dielectric (14) in the periphery region (18); forming a gate dielectric (22) in the periphery region (18); forming buried bitlines (26) in the core region (16); and forming gates (28) in the core region (16) and the periphery region (18).

WO 02/45157 A1



ACTION