# A NOVEL DEPOSITION-PLASMA CURE CYCLE PROCESS TO ENHANCE FILM QUALITY OF SILICON DIOXIDE

## CROSS-REFERENCES TO RELATED APPLICATIONS

**[0001]** This application claims the benefit of U.S. Provisional Application No. 60/803,481 filed May 30, 2006. This application is also related to co-assigned U.S. Provisional App. No. 60/803,493, by Ingle *et al*, filed May 30, 2006 and titled "CHEMICAL VAPOR DEPOSITION OF HIGH QUALITY FLOW-LIKE SILICON DIOXIDE USING A SILICON CONTAINING PRECURSOR AND ATOMIC OXYGEN". This application is also related to U.S. Provisional Application No. 60/803,489, by Nemani *et al*, filed May 30, 2006 and titled "A METHOD FOR DEPOSITING AND CURING LOW-K FILMS FOR GAPFILL AND CONFORMAL FILM APPLICATIONS". In addition, this application is related to U.S. Provisional Application No. 60/803,499 by Lubomirsky, filed May 30, 2006 and titled "PROCESS CHAMBER FOR DIELECTRIC GAPFILL". The entire contents of the priority U.S. Provisional patent application and the related applications are herein incorporated by reference for all purposes.

## BACKGROUND OF THE INVENTION

**[0002]** As the device density on integrated circuits continues to increase, the size and distance between device structures continue to decrease. The narrower widths in the gaps of the structures and the trenches between structures increases the ratio of height to width (*i.e.*, the aspect ratio) in these formations. In other words, the continued miniaturization of integrated circuit elements is shrinking the horizontal width within and between these elements faster than their vertical height.

**[0003]** While the ability to make device structures with ever increasing aspect ratios has allowed more of the structures (*e.g.*, transistors, capacitors, diodes, *etc.*) to be packed onto the same surface area of a semiconductor chip substrate, it has also created fabrication problems. Once of these problems is the difficulty of completely filling the gaps and trenches in these structures without creating a void or seam during the filling process. Filling gaps and

trenches with dielectric materials like silicon oxide is necessary to electrically isolate nearby device structures from each other. If the gaps were left empty, there would be too much electrical noise, and current leakage for the devices to operate properly (or at all).

**[0004]** When gap widths were larger (and aspect ratios smaller) the gaps were relatively easy to fill with a rapid deposit of a dielectric material. The deposition material would blanket the sides and bottom of the gap and continue to fill from the bottom up until the crevice or trench was fully filled. As aspect ratios increased however, it became more difficult to fill the deep, narrow trench without having a blockage start a void or seam in the fill volume.

**[0005]** Voids and seams in a dielectric layer cause create problems both during semiconductor device fabrication and in the finished devices. The voids and seams are formed randomly in the dielectric layer and have unpredictable sizes, shapes, locations and population densities. This results in unpredictable and inconsistent post-deposition processing of the layer, such as even etching, polishing, annealing, *etc.* The voids and seams in the finished devices also create variations in the dielectric qualities of gaps and trenches in device structures. This can result in uneven, and inferior device performance due to electrical crosstalk, charge leakage, and even shorting within and between device elements.

**[0006]** Techniques have been developed to minimize the formation of voids and seams during deposition of dielectric materials on high aspect ratio structures. These include slowing the deposition rate of the dielectric material so it stays more conformal to the sidewalls and bottom of the trench. A more conformal deposition can reduce the degree to which the deposited material builds up at the top or middle of the trench and eventually seals off the top of a void. Unfortunately however, slowing the deposition rate means increasing the deposition time, which reduces processing efficiency and production rates.

**[0007]** Another technique to control void formation is to increase the flowability of the deposited dielectric material. A material with more flowability can more quickly fill a void or seam and prevent it from becoming a permanent defect in the fill volume. Increasing the flowability of an silicon oxide dielectric material often involves adding water vapor or peroxide (*e.g.*, $H_2O_2$) to the mix of precursors used to form the oxide layer. The water vapor creates more Si-OH bonds in the deposited film, which impart an increased flowability to the film. Unfortunately however, increasing the moisture level during a silicon oxide deposition

can also adversely effect the properties of the deposited film, including its density (*i.e.*, an increased wet etch rate ratio (WERR)) and dielectric properties (*i.e.*, an increased k-value).

**[0008]** Thus, there remains a need for dielectric deposition systems and processes that can deposit voidless, seamless, dielectric films into gaps, trenches, and other device structures with high aspect ratios. There also remains a need for systems and processes that can deposit a dielectric materials at high deposition rates and flowability characteristics that do not adversely effect the quality of the finished fill. These and other aspects of dielectric film deposition are addressed by the present invention.

## BRIEF SUMMARY OF THE INVENTION

**[0009]** Embodiments of the invention include methods of filling a gap on a substrate with silicon oxide. The methods may include the steps of introducing an organo-silicon precursor and an oxygen precursor to a deposition chamber, reacting the precursors to form a first silicon oxide layer in the gap on the substrate, and etching the first silicon oxide layer to reduce the carbon content in the layer. The methods may also include forming a second silicon oxide layer on the first layer, and etching the second layer to reduce the carbon content in the layer. The silicon oxide layers may be annealed after the gap is filled.

**[0010]** Embodiments of the invention also include methods of forming a multilayer silicon oxide film on a substrate. The methods may include the steps of forming a plurality of silicon oxide layers on the substrate, where each silicon oxide layer has a thickness of about 100Å to about 200Å. The layers may be formed by: (i) introducing an organo-silicon precursor and an atomic oxygen precursor to a reaction chamber, (ii) reacting the precursors to form the layer on the substrate, and (iii) etching the layer to reduce impurities in the layer. The plurality of layers may then be annealed.

**[0011]** Embodiments of the invention still further include systems for performing a multi-cycle, silicon oxide bottom-up gapfills of gaps on wafer substrates. The systems may include a deposition chamber in which the gap containing substrate is held, and a remote plasma generating system coupled to the deposition chamber, where the plasma generating system is used to generate an atomic oxygen precursor. The systems may also include an organo-silicon precursor source used to supply an organo-silicon precursor to the deposition chamber, and a precursor handling system used to direct flows of the atomic oxygen precursor and the silicon precursor into the deposition chamber. The precursor handling

system keeps the atomic oxygen and silicon precursors from mixing before they enter the deposition chamber. The system still further includes an etching system to etch individual silicon oxide layers deposited during each cycle of the multi-cycle gapfill.

**[0012]** Additional embodiments and features are set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the specification or may be learned by the practice of the invention. The features and advantages of the invention may be realized and attained by means of the instrumentalities, combinations, and methods described in the specification.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0013]** A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the drawings wherein like reference numerals are used throughout the several drawings to refer to similar components. In some instances, a sublabel is associated with a reference numeral and follows a hyphen to denote one of multiple similar components. When reference is made to a reference numeral without specification to an existing sublabel, it is intended to refer to all such multiple similar components.

**[0014]** Fig. 1 is a flowchart showing a simplified overview a multi-cycle silicon oxide layer deposition according to embodiments of the invention;

**[0015]** Fig. 2 is a flowchart illustrating methods of making a multilayer silicon oxide film according to embodiments of the invention;

**[0016]** Fig. 3 is a flowchart that highlights a two-stage etching step in methods of making a multilayer silicon oxide film according to embodiments of the invention;

**[0017]** Fig. 4 is another flowchart illustrating methods of making a multilayer silicon oxide film according to embodiments of the invention;

**[0018]** Figs. 5A-F show a substrate having a gap structure that is progressively filled with a multilayer silicon oxide film according to embodiments of the invention;

**[0019]** Fig. 6A shows a vertical cross-sectional view of a substrate processing system that may be used to form silicon oxide layers according to embodiments of the invention; and

[0020] Fig. 6B is a simplified diagram of a system monitor/controller component of a substrate processing system according to embodiments of the invention.

## DETAILED DESCRIPTION OF THE INVENTION

[0021] Systems and methods are described for multilayer, multicycle depositions of silicon oxide in gaps and on surfaces of a wafer substrate. Each oxide layer is thin enough (e.g., about 50Å to about 300 Å) to allow an etch process to dissociate and remove impurities such as organic and hydroxyl groups that can adversely effect the quality and dielectric properties of the film. When a plurality of the oxide layers have been deposited and etched, an anneal may be done to form the layers into a high-quality, low-k silicon oxide film.

[0022] The silicon oxide may be formed from a reaction of highly reactive atomic oxygen and an organo-silicon precursor, such as OMCATS. The atomic oxygen may first be generated outside the chamber were the deposition occurs, and kept isolated from the organo-silicon precursor until they are mixed in the chamber. The resulting silicon oxide is carbon rich and highly flowable, providing a deposition film that easily flows to the bottoms of narrow gaps and trenches. After an etch process removes at least some of the larger carbon groups and hydroxyl groups in the deposited film, a subsequent oxide deposition may flow over the first layer and be etched into the next oxide layer. The cycle may be repeated several more times until, for example, a gap or trench is filled from the bottom up by a plurality of silicon oxide layers. This multicycle process has been referred to as a bottom-up gapfill. Additional details about the methods, products, and systems of the invention will now be discussed.

### Exemplary Oxide Layer Formation Processes

[0023] Fig. 1 shows a flowchart of a simplified overview a multi-cycle silicon oxide layer deposition according to embodiments of the invention. The method 100 shown includes providing a gap containing substrate to a deposition chamber 102. The substrate may have structures formed thereon that include gaps, trenches, *etc.*, with height to width aspect ratios of about 5:1 or more, 7:1 or more, 10:1 or more, 13:1 or more, 15:1 or more, *etc.*

[0024] A plurality of silicon oxide layers are then formed in the gaps (and on other surfaces) of the substrate 104. The silicon oxide may be deposited by reaction an oxygen containing precursor and an organo-silicon precursor in the reaction chamber. The oxygen containing precursor may include atomic oxygen that was remotely generated outside the

deposition chamber. The atomic oxygen may be generated by the dissociation of a precursor such as molecular oxygen ($O_2$), ozone ($O_3$), an nitrogen-oxygen compound (*e.g.*, NO, $NO_2$, $N_2O$, *etc.*), a hydrogen-oxygen compound (*e.g.*, $H_2O$, $H_2O_2$, *etc.*), a carbon-oxygen compound (*e.g.*, CO, $CO_2$, *etc.*), as well as other oxygen containing precursors and combinations of precursors.

**[0025]** The dissociation of the precursor to generate the atomic oxygen may also be done by thermal dissociation, ultraviolet light dissociation, and/or plasma dissociation, among other methods. Plasma dissociation may involve striking a plasma from helium, argon, *etc.*, in a remote plasma generating chamber and introducing the oxygen precursor to the plasma to generate the atomic oxygen precursor.

**[0026]** The atomic oxygen may be first introduced to the organo-silicon precursor in the chamber. The organo-silicon precursor may include compounds with direct Si-C bonding and/or compounds with Si-O-C bonding. Examples of organosilane silicon precursors may include dimethylsilane, trimethylsilane, tetramethylsilane, diethylsilane, tetramethylorthosilicate (TMOS), tetraethylorthosilicate (TEOS), octamethyltrisiloxane (OMTS), octamethylcyclotetrasiloxane (OMCTS), tetramethylcyclotetrasiloxane (TOMCATS), DMDMOS, DEMS, methyl triethoxysilane (MTES), phenyldimethylsilane, and phenylsilane, among others.

**[0027]** The organo-silicon precursor may be mixed with a carrier gas before or during its introduction to the deposition chamber. A carrier gas may be an inactive gas that does not unduly interfere with the formation of the oxide film on the substrate. Examples of carrier gases include helium, neon, argon, and hydrogen ($H_2$), among other gases.

**[0028]** In embodiments of method 100, the atomic oxygen and organo-silicon precursors are not mixed before being introduced to the deposition chamber. The precursors may enter the chamber through separate spatially separated precursor inlets distributed around reaction chamber. For example, the atomic oxygen precursor may enter from an inlet (or inlets) at the top of the chamber and positioned directly above the substrate. The inlet directs the flow of the oxygen precursor in a direction perpendicular to the substrate deposition surface. Meanwhile, the silicon precursor may enter from one or more inlets around the sides of the deposition chamber. The inlets may direct the flow of the silicon precursor in a direction approximately parallel to the deposition surface.

**[0029]** Additional embodiments include sending the atomic oxygen and silicon precursors through separate ports of a multi-port showerhead. For example, a showerhead positioned above the substrate may include a pattern of openings for the precursors to enter the deposition chamber. One subset of openings may be supplied by the atomic oxygen precursor, while a second subset of openings is supplied by the silicon precursor. Precursors traveling through different sets of opening may be fluidly isolated from each other until exiting into the deposition chamber. Additional details about types and designs of precursor handling equipment is described in a co-assigned U.S. Provisional Patent Application having attorney docket number A011162/T72700, by Lubomirsky, and titled PROCESS CHAMBER FOR DIELECTRIC GAPFILL", filed on the same day as the present application, the entire contents of which are hereby incorporated by reference for all purposes.

**[0030]** As the atomic oxygen and silicon precursors react in the deposition chamber, they form the silicon oxide layer on the substrate deposition surface. The initial oxide layer has excellent flowability, and can quickly migrate to the bottoms of the gaps in the structures on the substrate surface.

**[0031]** After each oxide layer is deposited, an etch step may be performed on the layer to remove impurities. This may include dissociating larger organic groups into smaller carbon containing molecules, and dissociating at least some of the Si-OH bonds to form water and silicon oxide.

**[0032]** Following the deposition and etching of the plurality of silicon oxide layers, an anneal may be performed to further drive out moisture and turn the layers into a dense, high-quality oxide film. Embodiments include performing an anneal after all the individual layers of silicon oxide have been deposited and etched. Additional embodiments may include intermediate anneals after one or more of the layers are formed, but before a final anneal of all the layers. For example, intermediate anneals may be done after every, 2, 3, 4, 5, *etc.*, layers are deposited, followed by a final anneal of all the layers.

**[0033]** Referring now to Fig. 2, a flowchart illustrating a method 200 of making a multilayer silicon oxide film according to embodiments of the invention is shown. The method 200 may include introducing precursors to a deposition chamber containing a substrate 202. As noted above, the precursors may include an atomic oxygen precursor and an organo-silicon precursor. The atomic oxygen may be generated in a remote high-density plasma generator supplying 4000 to 6000 Watts (*e.g.*, 5500 Watts) of RF power to a

combined gas stream of argon gas flowing at, for example, about 900 to 1800 sccm with molecular oxygen ($O_2$) flowing at, for example, about 600 to about 1200 sccm.

**[0034]** The organo-silicon precursor may be introduced to the deposition chamber by mixing an organo-silicon compound (gas or liquid) with a carrier gas such as helium or molecular hydrogen ($H_2$). For example, helium may be bubbled at a flow rate of about 600 to about 2400 sccm through a room-temperature liquid organo-silicon precursor such as octamethylcyclotetrasiloxane (OMCTS) to provide a flow of OMCTS to the chamber at a rate of about 800 to about 1600 mgm.

**[0035]** The precursors react with one another in the chamber to form a first oxide layer on the substrate 204. The total pressure in the chamber during the oxide layer deposition may be, for example, about 0.5 Torr to about 6 Torr. Higher total pressures (*e.g.*, 1.3 Torr) may deposit a oxide film with more flow-like qualities, while lower pressures (*e.g.*, 0.5 Torr) may deposit a more conformal oxide layer. Because the atomic oxygen is highly reactive, the deposition temperature in the reaction chamber may be relatively low (*e.g.*, about 100°C or less). Oxide deposition rates may range from about 125 Å/min to about 2 μm/min (*e.g.*, about 500 Å/min to about 3000 Å/min; about 1500Å/min, *etc.*). The thickness of the layer may be about 50Å to about 500Å (*e.g.*, about 100Å to about 200Å).

**[0036]** After the first oxide layer is formed, the flow of the precursors into the chamber may stop, and the first oxide layer may be etched 206. The etching step may be used to dissociate and remove impurities in the layer, and also to planarize the layer. As noted below in the description of Fig. 3, the etching process may include a single etch step, or multiple etch steps.

**[0037]** Following the etching of the first layer, the precursors are reintroduced to the deposition chamber 208, and react to form a second oxide layer on the substrate 210. The second oxide layer may be formed under the same reaction conditions as the first layer, or may be formed under a different conditions (*e.g.*, chamber pressure, temperature, organo-silicon precursor, *etc.*).

**[0038]** After the second layer has been formed it also may be etched 212 to reduced impurity levels and/or planarize the layer. The second layer may be etched using the same process as used to etch the first layer, or may be etched using a different process, (e.g., different number of etching steps, different etch precursors, different power level, *etc.*).

**[0039]** Following the formation and etching of the second silicon oxide layer (and any additional oxide layers) the oxide layers may be annealed 214 to form a uniform, high-quality silicon oxide gapfill. The final gapfill may have a dielectric constant (*i.e.*, k-value) of less than 4.0 (e.g., less than about 3.5; less than about 3.0, etc.), and a wet-etch rate ratio (WERR) of less than 2:1 (*e.g.*, about 1.8:1 to about 1.4:1). The gapfill may be uniform throughout the fill volume, and contain few, if any, voids or seams.

**[0040]** Fig. 3 shows a flowchart that highlights a two-stage etching step in a method 300 of making a multilayer silicon oxide film according to embodiments of the invention. The method 300 includes providing a substrate to a reaction chamber 302, and introducing precursors (*e.g.*, oxygen and silicon precursors) to the reaction chamber 304. The precursors then react to form a silicon oxide layer on the substrate 306, which then undergoes the two-stage etch.

**[0041]** The two-stage etch starts by conducting a first etch on the oxide layer 308. This first etch may include using a lower-density plasma to dissociate larger organic molecules and remove at least a portion of the carbon in the layer. This lower-density plasma etch may include using an RPS system to generate an $Ar/O_2$ plasma that etches the oxide layer. The etch conditions may include, for example, striking a plasma from a flow of 1600 sccm $O_2$ and 400 sccm argon at a power of about 5500 Watts and introducing it to the deposition chamber at a pressure of about 760 mTorr. This plasma etch can dissociate larger carbon groups and remove carbon impurities from the oxide layer.

**[0042]** Following the first etch, a second etch of the oxide layer is conducted 310 at a higher plasma density to remove at least a portion of the hydroxyl groups in the layer. This higher-density plasma etch may include exposing the layer to a plasma formed from the dissociation of a flow of molecular oxygen (*e.g.*, 600 sccm) with a high-power RF field (*e.g.*, 6000 Watts). The oxygen plasma may be introduced to the deposition chamber at a pressure of, for example, 8 mTorr, and react with the -OH groups in the oxide layer to form silicon dioxide and water.

**[0043]** The deposition and etch cycles may be repeated with a next oxide layer 312 formed on top of the previous layer. The deposited and etched oxide layers are then built up until a predetermined number of layers and/or film thickness is reached, and the plurality of layers are annealed 314. The anneal may be done in a single step, or multiple steps. A single step anneal may be done, for example, by heating the plurality of layers to about 300°C to about

1000°C (*e.g.*, about 600°C to about 900°C) in a substantially dry atmosphere (*e.g.*, dry nitrogen, helium, argon, *etc.*). The anneal removes moisture from the deposited layer and further converts Si-OH groups into silicon oxide.

**[0044]** Multi-step anneals may include a two-step anneal where the layers first undergo a wet anneal stage, such as heating the layer to, for example, about 700°C in the presence of steam. This may be followed by a dry anneal stage, where the layers are heated to a higher temperature (*e.g.*, about 900°C) in an atmosphere that is substantially free of moisture (*e.g.*, dry $N_2$). The first, wet anneal, may help hydrolyze additional Si-C bonds with Si-OH bonds, while the dry anneal converts the Si-OH into silicon oxide bonds and drives off moisture from the layers.

**[0045]** In addition to wet and dry thermal annealing, other annealing techniques (alone or in combination) may be used to anneal the plurality of oxide layers. These include a steam anneal, a plasma anneal, an ultraviolet light anneal, an e-beam anneal, and/or a microwave anneal, among others.

**[0046]** Referring now to Fig. 4, another flowchart illustrating a method 400 of making a multilayer silicon oxide film according to embodiments of the invention is shown. The method 400 includes providing a substrate to a deposition chamber 402 and introducing precursors (*e.g.*, atomic oxygen and organo-silicon precursors) to the chamber 404. The precursors react to form a silicon oxide layer on the substrate 406, and then the oxide layer may be etched 408.

**[0047]** At this point, a check may be made to determine if the cumulative thickness of the deposited oxide layers has reached a preset point 410. If the preset thickness level of the total oxide film has been reached, then the deposition and etch cycle may end, and the film may be annealed 412. However, if the thickness level has not been met, then another oxide deposition and etch cycle may occur to add at least one more additional layer to the oxide film.

**[0048]** Determining whether the oxide film has reached a predetermined thickness may be done by a thickness measurement of the deposited and etched layers, or may be done by calculating the number of layers need to reach a desired film thickness. For example, if each deposited and etched layer is 100Å thick, and the desired film thickness 1.2 μm, then 12 deposition and etch cycles should be done to form the film. The thickness of each deposited layer may be set by controlling the parameters that effect the oxide deposition rate, such as

the types and flow rates of the reactive precursors, the total pressure in the deposition chamber, and the temperature, among other parameters. As noted above, typical deposition rates for the oxide layers are about 500Å/min to about 3000Å/min (*e.g.*, about 1500Å/min).

**[0049]** Figs. 5A-F show a substrate having a gap structure that is progressively filled with a multilayer silicon oxide film using embodiments of the multicycle deposition-etch oxide layer formation process. Fig. 5A shows a substrate 502 on which a gap 504 has been formed. It will be appreciated that gap 504 shown in Figs. 5A-F has been drawn with a relatively low aspect ratio to more clearly show the progression of the oxide fill layers. Embodiments of the present gapfill methods may include void and seam free depositions into gaps having aspect ratios of 5:1, 6:1, 7:1, 8:1, 9:1, 10:1, 11:1, 12:1, 13:1, 14:1, and 15:1 or more.

**[0050]** Fig. 5B shows a first oxide layer 506a deposited in gap 504. The silicon oxide that formed the layer has good flowability qualities, allowing the film to quickly migrate to the bottom of gap 504. Thus, the thickness of the deposited oxide at the bottom of the gap 504 may be greater than the oxide thickness along the sidewalls of the gap.

**[0051]** Figs. 5C and D show additional oxide layers 506b, 506c, *etc.*, being deposited on previously deposited and etched layers in the gap 504. These additional layers may be formed from the bottom up in the gap 504, until a desired oxide film thickness level is reached (*e.g.*, the top of gap 504).

**[0052]** Once the last of the plurality of the oxide layers is deposited and etched, an anneal may be conducted to form the layers into a uniform film 508, as shown in Fig. 5E. The film may be planarized by, for example, plasma etching or CMP to remove deposition materials formed over the top of the gap 504. Fig. 5F shows the remaining silicon oxide gapfill 510, having few, if any, voids or seams, and having high film-quality and dielectric characteristics.

Exemplary Substrate Processing System

**[0053]** Deposition systems that may implement embodiments of the present invention may include high-density plasma chemical vapor deposition (HDP-CVD) systems, plasma enhanced chemical vapor deposition (PECVD) systems, sub-atmospheric chemical vapor deposition (SACVD) systems, and thermal chemical vapor deposition systems, among other types of systems. Specific examples of CVD systems that may implement embodiments of the invention include the CENTURA ULTIMA™ HDP-CVD chambers/systems, and

PRODUCER™ PECVD chambers/systems, available from Applied Materials, Inc. of Santa Clara, California.

**[0054]** One suitable substrate processing system in which can be modified to utilize embodiments in accordance with the present invention is shown and described in co-assigned U.S. Pat. Nos. 6,387,207 and 6,830,624, which are incorporated herein by reference for all purposes. FIG. 6A is vertical, cross-sectional views of a CVD system 10, having a vacuum or processing chamber 15 that includes a chamber wall 15a and a chamber lid assembly 15b.

**[0055]** The CVD system 10 contains a gas distribution manifold 11 for dispersing process gases to a substrate (not shown) that rests on a heated pedestal 12 centered within the process chamber 15. Gas distribution manifold 11 may be formed from an electrically conducting material in order to serve as an electrode for forming a capacitive plasma. During processing, the substrate (e.g. a semiconductor wafer) is positioned on a flat (or slightly convex) surface 12a of the pedestal 12. The pedestal 12 can be moved controllably between a lower loading/off-loading position (depicted in FIG. 6A) and an upper processing position (indicated by dashed line 14 in FIG. 6A), which is closely adjacent to the manifold 11. A centerboard (not shown) includes sensors for providing information on the position of the wafers.

**[0056]** Deposition and carrier gases are introduced into the chamber 15 through perforated holes 13b of a conventional flat, circular gas distribution faceplate 13a. More specifically, deposition process gases flow into the chamber through the inlet manifold 11, through a conventional perforated blocker plate 42 and then through holes 13b in gas distribution faceplate 13a.

**[0057]** Before reaching the manifold 11, deposition and carrier gases are input from gas sources 7 through gas supply lines 8 into a mixing system 9 where they are combined and then sent to manifold 11. Generally, the supply line for each process gas includes (i) several safety shut-off valves (not shown) that can be used to automatically or manually shut-off the flow of process gas into the chamber, and (ii) mass flow controllers (also not shown) that measure the flow of gas through the supply line. When toxic gases are used in the process, the several safety shut-off valves are positioned on each gas supply line in conventional configurations.

**[0058]** The deposition process performed in the CVD system 10 can be either a thermal process or a plasma-enhanced process. In a plasma-enhanced process, an RF power supply

44 applies electrical power between the gas distribution faceplate 13a and the pedestal 12 so as to excite the process gas mixture to form a plasma within the cylindrical region between the faceplate 13a and the pedestal 12. (This region will be referred to herein as the "reaction region"). Constituents of the plasma react to deposit a desired film on the surface of the semiconductor wafer supported on pedestal 12. RF power supply 44 is a mixed frequency RF power supply that typically supplies power at a high RF frequency (RF1) of 13.56 MHz and at a low RF frequency (RF2) of 360 KHz to enhance the decomposition of reactive species introduced into the vacuum chamber 15. In a thermal process, the RF power supply 44 would not be utilized, and the process gas mixture thermally reacts to deposit the desired films on the surface of the semiconductor wafer supported on the pedestal 12, which is resistively heated to provide thermal energy for the reaction.

**[0059]** During a plasma-enhanced deposition process, the plasma heats the entire process chamber 10, including the walls of the chamber body 15a surrounding the exhaust passageway 23 and the shut-off valve 24. When the plasma is not turned on or during a thermal deposition process, a hot liquid is circulated through the walls 15a of the process chamber 15 to maintain the chamber at an elevated temperature. The passages in the remainder of the chamber walls 15a are not shown. Fluids used to heat the chamber walls 15a include the typical fluid types, *i.e.*, water-based ethylene glycol or oil-based thermal transfer fluids. This heating (referred to as heating by the "heat exchanger") beneficially reduces or eliminates condensation of undesirable reactant products and improves the elimination of volatile products of the process gases and other contaminants that might contaminate the process if they were to condense on the walls of cool vacuum passages and migrate back into the processing chamber during periods of no gas flow.

**[0060]** The remainder of the gas mixture that is not deposited in a layer, including reaction byproducts, is evacuated from the chamber 15 by a vacuum pump (not shown). Specifically, the gases are exhausted through an annular, slot-shaped orifice 16 surrounding the reaction region and into an annular exhaust plenum 17. The annular slot 16 and the plenum 17 are defined by the gap between the top of the chamber's cylindrical side wall 15a (including the upper dielectric lining 19 on the wall) and the bottom of the circular chamber lid 20. The 360.degree. circular symmetry and uniformity of the slot orifice 16 and the plenum 17 are important to achieving a uniform flow of process gases over the wafer so as to deposit a uniform film on the wafer.

**[0061]** From the exhaust plenum 17, the gases flow underneath a lateral extension portion 21 of the exhaust plenum 17, past a viewing port (not shown), through a downward-extending gas passage 23, past a vacuum shut-off valve 24 (whose body is integrated with the lower chamber wall 15a), and into the exhaust outlet 25 that connects to the external vacuum pump (not shown) through a foreline (also not shown).

**[0062]** The wafer support platter of the pedestal 12 (preferably aluminum, ceramic, or a combination thereof) is resistively heated using an embedded single-loop embedded heater element configured to make two full turns in the form of parallel concentric circles. An outer portion of the heater element runs adjacent to a perimeter of the support platter, while an inner portion runs on the path of a concentric circle having a smaller radius. The wiring to the heater element passes through the stem of the pedestal 12.

**[0063]** Typically, any or all of the chamber lining, gas inlet manifold faceplate, and various other reactor hardware are made out of material such as aluminum, anodized aluminum, or ceramic. An example of such a CVD apparatus is described in co-assigned U.S. Pat. No. 5,558,717 entitled "CVD Processing Chamber," issued to Zhao *et al*, and hereby incorporated by reference in its entirety.

**[0064]** A lift mechanism and motor 32 (FIG. 6A) raises and lowers the heater pedestal assembly 12 and its wafer lift pins 12b as wafers are transferred into and out of the body of the chamber 15 by a robot blade (not shown) through an insertion/removal opening 26 in the side of the chamber 10. The motor 32 raises and lowers pedestal 12 between a processing position 14 and a lower, wafer-loading position. The motor, valves or flow controllers connected to the supply lines 8, gas delivery system, throttle valve, RF power supply 44, and chamber and substrate heating systems are all controlled by a system controller over control lines 36, of which only some are shown. Controller 34 relies on feedback from optical sensors to determine the position of movable mechanical assemblies such as the throttle valve and susceptor which are moved by appropriate motors under the control of controller 34.

**[0065]** In the exemplary embodiment, the system controller includes a hard disk drive (memory 38), a floppy disk drive and a processor 37. The processor contains a single-board computer (SBC), analog and digital input/output boards, interface boards and stepper motor controller boards. Various parts of CVD system 10 conform to the Versa Modular European (VME) standard which defines board, card cage, and connector dimensions and types. The

VME standard also defines the bus structure as having a 16-bit data bus and a 24-bit address bus.

**[0066]** System controller 34 controls all of the activities of the CVD machine. The system controller executes system control software, which is a computer program stored in a computer-readable medium such as a memory 38. Preferably, the memory 38 is a hard disk drive, but the memory 38 may also be other kinds of memory. The computer program includes sets of instructions that dictate the timing, mixture of gases, chamber pressure, chamber temperature, RF power levels, susceptor position, and other parameters of a particular process. Other computer programs stored on other memory devices including, for example, a floppy disk or other another appropriate drive, may also be used to operate controller 34.

**[0067]** A process for depositing a film on a substrate or a process for cleaning the chamber 15 can be implemented using a computer program product that is executed by the controller 34. The computer program code can be written in any conventional computer readable programming language: for example, 68000 assembly language, C, C++, Pascal, Fortran or others. Suitable program code is entered into a single file, or multiple files, using a conventional text editor, and stored or embodied in a computer usable medium, such as a memory system of the computer. If the entered code text is in a high level language, the code is compiled, and the resultant compiler code is then linked with an object code of precompiled Microsoft Windows® library routines. To execute the linked, compiled object code the system user invokes the object code, causing the computer system to load the code in memory. The CPU then reads and executes the code to perform the tasks identified in the program.

**[0068]** The interface between a user and the controller 34 is via a CRT monitor 50a and light pen 50b, shown in FIG. 6B, which is a simplified diagram of the system monitor and CVD system 10 in a substrate processing system, which may include one or more chambers. In the preferred embodiment two monitors 50a are used, one mounted in the clean room wall for the operators and the other behind the wall for the service technicians. The monitors 50a simultaneously display the same information, but only one light pen 50b is enabled. A light sensor in the tip of light pen 50b detects light emitted by CRT display. To select a particular screen or function, the operator touches a designated area of the display screen and pushes the button on the pen 50b. The touched area changes its highlighted color, or a new menu or

screen is displayed, confirming communication between the light pen and the display screen. Other devices, such as a keyboard, mouse, or other pointing or communication device, may be used instead of or in addition to light pen 50b to allow the user to communicate with controller 34.

**[0069]** FIG. 6A shows a remote plasma generator 60 mounted on the lid assembly 15b of the process chamber 15 including the gas distribution faceplate 13a and the gas distribution manifold 11. A mounting adaptor 64 mounts the remote plasma generator 60 on the lid assembly 15b, as best seen in FIG. 6A. The adaptor 64 is typically made of metal. A mixing device 70 is coupled to the upstream side of the gas distribution manifold 11 (FIG. 6A). The mixing device 70 includes a mixing insert 72 disposed inside a slot 74 of a mixing block for mixing process gases. A ceramic isolator 66 is placed between the mounting adaptor 64 and the mixing device 70 (FIGS. 6A). The ceramic isolator 66 may be made of a ceramic material such as $Al_2O_3$ (99% purity), Teflon®, or the like. When installed, the mixing device 70 and ceramic isolator 66 may form part of the lid assembly 15b. The isolator 66 isolates the metal adaptor 64 from the mixing device 70 and gas distribution manifold 11 to minimize the potential for a secondary plasma to form in the lid assembly 15b as discussed in more detail below. A three-way valve 77 controls the flow of the process gases to the process chamber 15 either directly or through the remote plasma generator 60.

**[0070]** The remote plasma generator 60 is desirably a compact, self-contained unit that can be conveniently mounted on the lid assembly 15b and be easily retrofitted onto existing chambers without costly and time-consuming modifications. One suitable unit is the ASTRON® generator available from Applied Science and Technology, Inc. of Woburn, Mass. The ASTRON® generator utilizes a low-field toroidal plasma to dissociate a process gas. In one example, the plasma dissociates a process gas including a fluorine-containing gas such as $NF_3$ and a carrier gas such as argon to generate free fluorine which is used to clean film deposits in the process chamber 15.

**[0071]** Having described several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the invention. Additionally, a number of well known processes and elements have not been described in order to avoid unnecessarily obscuring the present invention. Accordingly, the above description should not be taken as limiting the scope of the invention.

**[0072]** Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limits of that range is also specifically disclosed. Each smaller range between any stated value or intervening value in a stated range and any other stated or intervening value in that stated range is encompassed. The upper and lower limits of these smaller ranges may independently be included or excluded in the range, and each range where either, neither or both limits are included in the smaller ranges is also encompassed within the invention, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included.

**[0073]** As used herein and in the appended claims, the singular forms "a", "an", and "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a process" includes a plurality of such processes and reference to "the precursor" includes reference to one or more precursors and equivalents thereof known to those skilled in the art, and so forth.

**[0074]** Also, the words "comprise," "comprising," "include," "including," and "includes" when used in this specification and in the following claims are intended to specify the presence of stated features, integers, components, or steps, but they do not preclude the presence or addition of one or more other features, integers, components, steps, acts, or groups.

WHAT IS CLAIMED IS:

1. A method of filling a gap on a substrate with silicon oxide, the method comprising:

introducing an organo-silicon precursor and an oxygen precursor to a deposition chamber;

reacting the precursors to form a first silicon oxide layer in the gap on the substrate;

etching the first silicon oxide layer to reduce the carbon content in the layer;

forming a second silicon oxide layer on the first layer, and etching the second layer to reduce the carbon content in the layer, wherein the etching operation of the first and second silicon oxide layers comprises:

exposing the layer to a first plasma having a first density, wherein the first plasma dissociates larger carbon molecules in the layer, and

exposing the layer to a second plasma having a second density that is higher than the first density, wherein the second plasma dissociates silicon-hydroxide bonds in the layer; and

annealing the silicon oxide layers after the gap is filled.

2. The method of claim 1, wherein the oxygen precursor comprises atomic oxygen that is generated outside the deposition chamber.

3. The method of claim 2, wherein the atomic oxygen is formed by:

forming a plasma from a gas mixture comprising argon; and

introducing an oxygen precursor to the plasma, wherein the oxygen precursor dissociates to form the atomic oxygen.

4. The method of claim 3, wherein the oxygen precursor is selected from the group consisting of molecular oxygen, ozone, and nitrogen dioxide.

5. The method of claim 2, wherein the atomic oxygen is formed by:

introducing an oxygen precursor into a photodissociation chamber; and

exposing the oxygen precursor to ultraviolet light, wherein the ultraviolet light dissociates the oxygen precursor to form atomic oxygen.

6. The method of claim 2, wherein the organo-silicon precursor and the atomic oxygen are not mixed until after being introduced into the deposition chamber.

7. The method of claim 1, wherein the organo-silicon precursor comprises dimethylsilane, trimethylsilane, tetramethylsilane, diethylsilane, tetramethylorthosilicate (TMOS), tetraethylorthosilicate (TEOS), octamethyltrisiloxane (OMTS), octamethylcyclotetrasiloxane (OMCTS), tetramethylcyclotetrasiloxane (TOMCATS), DMDMOS, DEMS, methyl triethoxysilane (MTES), phenyldimethylsilane, or phenylsilane.

8. The method of claim 1, wherein the first and second silicon oxide layers each have a thickness from about 100Å to about 200Å.

9. The method of claim 1, wherein the annealing of the silicon oxide layers comprises an anneal in a dry non-reactive gas at a temperature of about 800°C or more.

10. The method of claim 10, wherein the non-reactive gas is nitrogen ($N_2$) and the temperature is 900°C.

11. The method of claim 1, wherein the method includes forming additional silicon oxide layers on the first and second layers, and wherein each additional silicon oxide layer has a thickness of about 50Å to about 500Å.

12. The method of claim 12, wherein the additional silicon oxide layers are etched in the same manner as the first and second silicon oxide layers.

13. The method of claim 12, wherein a total thickness of the silicon oxide layers is about 500Å to about 10,000Å.

14. The method of claim 1, wherein the annealed silicon oxide layers have a wet etch rate ratio (WERR) of about 2:1 or less.

15. The method of claim 1, wherein the annealed silicon oxide layers have a wet etch rate ratio (WERR) of about 1.8:1 to about 1.4:1.

16. The method of claim 1, wherein the annealed silicon oxide layers have a k-value of about 4.0 or less.

17. The method of claim 1, wherein the method further comprises pretreating the substrate with a high-density plasma before introducing the precursors to the deposition chamber.

18. The method of claim 1, wherein the gap has a height to width aspect ratio of about 5:1 or more.

19. The method of claim 1, wherein the gap has a height to width aspect ratio of about 13:1 or more.

20. A method of forming a multilayer silicon oxide film on a substrate, the method comprising:

forming a plurality of silicon oxide layers on the substrate, wherein each silicon oxide layer has a thickness of about 100Å to about 200Å, and wherein each layer is formed by;

(i) introducing an organo-silicon precursor and an atomic oxygen precursor to a reaction chamber,

(ii) reacting the precursors to form the layer on the substrate, and

(iii) etching the layer to reduce impurities in the layer, wherein the etching of the layer comprises:

exposing the layer to a first plasma having a first density, wherein the first plasma dissociates larger carbon molecules in the layer, and

exposing the layer to a second plasma having a second density that is higher than the first density, wherein the second plasma dissociates silicon-hydroxide bonds in the layer; and

annealing the plurality of layers.

21. The method of claim 21, wherein the atomic oxygen precursor is generated outside the deposition chamber, and wherein the organo-silicon and atomic oxygen precursors are not mixed until after being introduced into the reaction chamber.

22. The method of claim 21, wherein the annealing of the plurality of layers comprises a thermal anneal, a steam anneal, a plasma anneal, an ultraviolet light anneal, an e-beam anneal, or a microwave anneal.

23. The method of claim 21, wherein the annealing of the plurality of layers comprises:

heating the substrate at a first anneal temperature in the presence of steam; and

heating the substrate at a second anneal temperature in dry nitrogen.

24. The method of claim 25, wherein the first anneal temperature is about 650°C and the second anneal temperature is about 900°C.

25. The method of claim 21, wherein each of the plurality of layers is formed at a rate of about 125 Å/min to about 2 μm/min.

26. The method of claim 21, wherein each of the layers is etched in about 3 minutes or less.

27. The method of claim 21, wherein the plurality of layers is annealed in about 30 minutes or less.

28. The method of claim 21, wherein the plurality of layers have a wet etch rate ratio (WERR) of about 1.8:1 to about 1.4:1.

29. The method of claim 21, wherein the plurality of layers have a -value of about 4.0 or less.

30. The method of claim 21, wherein the multilayer silicon oxide film has a thickness of about 1000Å to about 3000Å.