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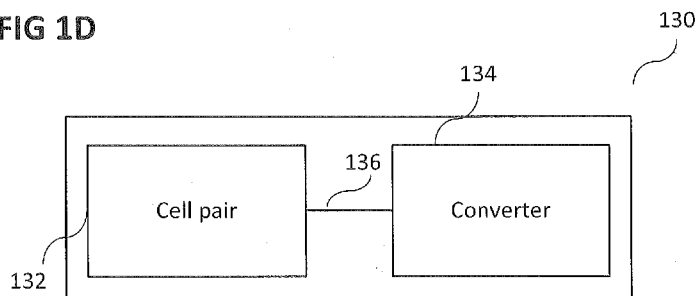
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FIG 1D



(57) Abstract: According to various embodiments, a testing apparatus may be provided. The testing apparatus may include: a cell pair comprising two *l*-bit memory cells configured to represent a stored pattern of *l*-bit; and a converter configured to convert a query pattern of *l*-bit into a pair of voltages defined such that when applied to gates of the cell pair, the voltages make the cell pair into high resistance mode when the query pattern matches the stored pattern and into low resistance mode when the query pattern does not match the stored pattern.