We claim:

1. A capacitive energy storage device (CESD), comprising:

an array of electrodes with spaces between the electrodes, the array of electrodes comprising *n* groups of electrodes in one or more planes, where *n* is an integer greater than or equal to 2, each electrode having a central axis A_C perpendicular to the plane in which the electrode is located, each group of electrodes comprising a plurality of electrodes;

an electrical interconnect for each group of electrodes, each electrical interconnect comprising an electrically conductive filament connecting electrodes of a group in series;

an edge connector for each electrical interconnect, wherein a terminal end of the electrical interconnect is coupled to the edge connector; and

a dielectric material occupying the spaces between the electrodes and contacting the electrodes, wherein regions of the dielectric material located between adjacent electrodes define capacitive elements, and wherein the dielectric material is an electroentropic dielectric material that has a relative permittivity greater than 3.9, the electroentropic dielectric material comprising a plurality of polymeric molecules,

wherein

the array comprises a grid pattern of rows and columns of electrodes, each row comprising electrodes of a row group alternating with electrodes of a plurality of column groups,

each row group further comprises a row electrical interconnect connecting each electrode of the row group in series, and

each column group further comprises a column electrical interconnect connecting each electrode of the column group in series, wherein there is a vertical spatial separation at each intersection where a row electrical interconnect crosses a column electrical interconnect.

2. The CESD of claim 1, wherein:

the column electrical interconnects are offset from the central axes of the column electrodes and have a branched configuration to connect to each column electrode.

3. The CESD of claim 1, further comprising:

an insulative layer disposed between the row electrical interconnects and the column electrical interconnects such that the row electrical interconnects are above the insulative layer and the column electrical interconnects are below the insulative layer; and

a via defined by the insulative layer for each electrode of the row group, the via connecting the electrode to the row electrical interconnect.

4. The CESD of claim 1, wherein a central axis-to-central axis spacing between adjacent electrodes is within a range of 5 nm to 5 mm.

5. A method for making a capacitive energy storage device (CESD) according to claim 1, comprising:

forming an array of electrodes at least partially embedded within or in contact with a dielectric material with spaces between the electrodes, the array of electrodes comprising *n* groups of electrodes arranged in one or more planes, where *n* is an integer greater than or equal to 2, each group of electrodes comprising a plurality of electrodes and each electrode having a central axis perpendicular to the plane, wherein the array comprises a grid pattern of rows and columns of electrodes, each row comprising electrodes of a row group alternating with electrodes of a plurality of column groups;

connecting electrodes of each group in series with an electrical interconnect comprising an electrically conductive filament by (i) connecting electrodes of each column group with a column electrical interconnect and (ii) connecting electrodes of each row group in series with a row electrical interconnect, such that there is a vertical spatial separation at each intersection where a row electrical interconnect crosses a column electrical interconnect; and

connecting a terminal end of each electrical interconnect to an edge connector, thereby forming the CESD.

6. The method of claim 5, wherein forming the array of electrodes at least partially embedded in or in contact with the dielectric material further comprises:

(i) forming the array of electrodes, and disposing the dielectric material in the spaces between the electrodes; or

(ii) forming a layer of the dielectric material, and at least partially embedding the electrodes in the dielectric material or placing the electrodes in contact with the dielectric material to form the array of electrodes.

7. A method for using a capacitive energy storage device (CESD) according to claim 1, comprising:

providing a CESD according to claim 1; and

applying a voltage across a capacitive element disposed between two adjacent electrodes, wherein the capacitive element is a region of the dielectric material located between the adjacent electrodes, thereby charging the capacitive element to a voltage *V1*.

8. The method of claim 7, further comprising supplying energy from the CESD to a load by:

providing a circuit including the CESD and a load connected to the CESD, wherein the capacitive element is charged to the voltage *V1*; and

applying a reversed polarization electric potential across the capacitive element for a discharge period of time, wherein the reversed polarization electric potential is less than the voltage *V1* and less than a voltage that would be generated by the capacitive element in a high impedance state, thereby supplying power from the capacitive element to the load.

9. A method of using a memory device, comprising:

providing a memory device comprising a capacitive energy storage device (CESD) according to claim 1; and

writing to the memory device by applying a voltage across a capacitive element disposed between an electrode of a first group of electrodes and an adjacent electrode of a second group of electrodes, wherein the capacitive element is a region of the dielectric material located between the electrode of the first group and the adjacent electrode of the second group, thereby charging the capacitive element to a voltage *V1*.

10. A method of refreshing a memory device, comprising:

providing a capacitive energy storage device (CESD) according to claim 1;

charging a capacitive element in the CESD to a voltage *V1*, wherein the voltage *V1* discharges, at least in part, due to leakage over time;

subsequently determining a capacitance *C* of the capacitive element;

determining, based on the capacitance *C*, the voltage *V1*; and

recharging the capacitive element to the voltage *V1*.