

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:
 - a base including a first bonding structure; and
 - a first semiconductor chip, including a second bonding structure, the second bonding structure being coupled to the first bonding structure of the base,wherein the first bonding structure includes:
 - a test pad;
 - a first pad being electrically connected to the test pad; and
 - a first insulating layer,wherein the second bonding structure includes:
 - a second pad being electrically connected to the first pad; and
 - a second insulating layer being in contact with the first insulating layer,wherein at least a portion of the test pad is in contact with the second insulating layer,
 - wherein the first bonding structure further includes a pad connection portion electrically connecting the first pad and the test pad to each other, and
 - wherein the second bonding structure further includes a dummy connection portion, the dummy connection portion being in contact with the pad connection portion.
2. The semiconductor package of claim 1, wherein at least a portion of the pad connection portion is in contact with the second insulating layer.
3. The semiconductor package of claim 1 or claim 2, wherein the second bonding structure further includes a dummy pad portion,
 - wherein the test pad of the base includes:
 - a test area; and
 - a dummy area surrounding the test area, andwherein the dummy pad portion of the second bonding structure is in contact with

the dummy area of the test pad.

4. The semiconductor package of claim 3, wherein the test area is in contact with the second insulating layer of the first semiconductor chip.

5. The semiconductor package of any one of claims 1 to 4, wherein the base includes:

a base body;

a through electrode structure penetrating through the base body; and

a base back side structure disposed on the base body,

wherein the first bonding structure of the base is disposed on the base back side structure, and

wherein the base back side structure includes a base wiring structure electrically connected to the test pad.

6. The semiconductor package of claim 5, wherein the base body comprises a silicon substrate.

7. The semiconductor package of any one of claims 1 to 6, wherein the base comprises an interposer.

8. The semiconductor package of any one of claims 1 to 7, wherein the base comprises a semiconductor chip different from the first semiconductor chip.

9. The semiconductor package of any one of claims 1 to 8, wherein the test pad has a width greater than a width of the first pad.

10. The semiconductor package of any one of claims 1 to 9 further comprising:

a lower structure disposed below the base; and
a connection structure disposed between the base and the lower structure.

11. A semiconductor package comprising:

a base including a first bonding structure; and

a plurality of semiconductor chips disposed on the base,

wherein the plurality of semiconductor chips include:

a first semiconductor chip; and

a second semiconductor chip, which are sequentially stacked on and coupled to the base,

wherein the first semiconductor chip comprises:

a first surface including a second bonding structure; and

a second surface opposite to the first surface,

wherein the second semiconductor chip comprises:

a third surface; and

a fourth surface opposite to the third surface,

wherein the first semiconductor chip includes a first semiconductor body and a first internal circuit wiring,

wherein the second semiconductor chip includes a second semiconductor body and a second internal circuit wiring,

wherein the first internal circuit wiring is between the first semiconductor body and the first surface,

wherein the second internal circuit wiring is between the second semiconductor body and the third surface,

wherein the second surface of the first semiconductor chip includes:

a first pad;

a first test pad; and

a first insulating layer, and

wherein the third surface of the second semiconductor chip includes:

a second pad being in contact with and bonded to the first pad; and

a second insulating layer being in contact with and bonded to the first insulating layer,

wherein the first bonding structure of the base includes:

a third pad;

a second test pad; and

a third insulating layer,

wherein the second bonding structure of the first semiconductor chip includes:

a fourth pad being in contact with and bonded to the third pad; and

a fourth insulating layer being in contact with and bonded to the third insulating layer,

wherein the first bonding structure further includes a pad connection portion electrically connecting the third pad and the second test pad to each other, and

wherein the second bonding structure further includes a dummy connection portion, the dummy connection portion being in contact with the pad connection portion.

12. The semiconductor package of claim 11, wherein at least a portion of the test pad is in contact with the second insulating layer.

13. The semiconductor package of claim 11 or claim 12, wherein the base has a first width greater than a second width of each of the plurality of semiconductor chips.

14. A semiconductor package comprising:

a base having a first surface and a second surface opposite to the first surface;

a lower semiconductor chip disposed on the base and having a third surface and a fourth surface opposite to the third surface; and

an upper semiconductor chip disposed on the lower semiconductor chip and having

a fifth surface and a sixth surface opposite to the fifth surface,

wherein:

each of the second surface of the base and the fourth surface of the lower semiconductor chip includes a first bonding structure,

each of the third surface of the lower semiconductor chip and the fifth surface of the upper semiconductor chip includes a second bonding structure,

the first bonding structure includes:

a first pad;

a test pad; and

a first insulating layer,

the second bonding structure includes:

a second pad; and

a second insulating layer,

the first bonding structure of the base and the second bonding structure of the lower semiconductor chip are bonded while being in contact with each other, and

the first bonding structure of the lower semiconductor chip and the second bonding structure of the upper semiconductor chip are bonded while being in contact with each other,

wherein the first bonding structure of the base further includes a pad connection portion electrically connecting the first pad and the test pad to each other, and

wherein the second bonding structure of the lower semiconductor chip further includes a dummy connection portion, the dummy connection portion being in contact with the pad connection portion.

15. The semiconductor package of claim 14, wherein each of the first pad and the second pad comprises a conductive material.

16. The semiconductor package of claim 14 or claim 15, wherein:

the first pad of the first bonding structure of the base and the second pad of the second

bonding structure of the lower semiconductor chip are bonded while being in contact with each other, and

at least a portion of the test pad of the first bonding structure of the base is in contact with the second insulating layer of the second bonding structure of the lower semiconductor chip.

17. The semiconductor package of any one of claims 14 to 16, wherein:

the first pad of the first bonding structure of the lower semiconductor chip and the second pad of the second bonding structure of the upper semiconductor chip are bonded while being in contact with each other, and

at least a portion of the test pad of the first bonding structure of the lower semiconductor chip is in contact with the second insulating layer of the second bonding structure of the upper semiconductor chip.

18. The semiconductor package of any one of claims 14 to 17, wherein the lower semiconductor chip further includes a through electrode structure disposed between the third surface and the fourth surface.