CLAIMS

1. A method of making a semiconductor package, comprising:

placing a single layer dielectric film on a temporary carrier substrate, the single layer dielectric film comprising a first surface and a second surface opposite the first surface;

placing a plurality of semiconductor die directly on the first surface of the single layer dielectric film opposite the second surface of the single layer dielectric film attached to the temporary carrier substrate;

curing the single layer dielectric film after placing the plurality of semiconductor die on the first surface of the single layer dielectric film to lock the plurality of semiconductor die in place on the single layer dielectric film;

encapsulating the plurality of semiconductor die directly on the single layer dielectric film with an encapsulant;

patterning the single layer dielectric film utilizing a mask-less patterning technique to form a via hole that extends from the first surface of the cured single layer dielectric film to the second surface of the cured single layer dielectric film after removing the temporary carrier substrate; and

forming a conductive layer directly on, substantially parallel to, and extending across, the second surface of the patterned single layer dielectric film, within the vial hole, and over the plurality of semiconductor die.

2. The method of claim 1, further comprising placing an active surface of the plurality of semiconductor die on the first surface of the single layer dielectric film.

3. The method of claim 1, further comprising:

laminating the single layer dielectric film to the temporary carrier substrate at a temperature in a range of 100-130 °C., wherein the single layer dielectric film comprises a thickness in a range of 5-50 micrometers, a glass transition temperature (Tg) in a range of 140-190 °C., and further comprises 50-90% of ceramic filler or silica filler by weight; and

after laminating the single layer dielectric film to the temporary carrier, placing the plurality of semiconductor die directly on the first surface of the single layer dielectric film, and curing the single layer dielectric film at a temperature greater than the glass transition temperature (Tg) of the single layer dielectric film.

4. The method of claim 1, further comprising using laser ablation to form the via hole comprising a first depth and redistribution layer (RDL) trace pattern openings comprising a second depth less than the first depth to intersect with the via hole in the single layer dielectric film.

5. The method of claim 1, further comprising:

forming the plurality of semiconductor die with thick RDL traces formed while the plurality of semiconductor die is part of a native wafer; and

placing the plurality of semiconductor die directly on the first surface of the single layer dielectric film with the thick RDLs directly contacting the first surface of the single layer dielectric film.

6. A method of making a semiconductor package, comprising:

placing a single layer dielectric film on a temporary carrier substrate, the single layer dielectric film comprising a first surface and a second surface opposite the first surface;

placing a plurality of semiconductor die directly on the first surface of the single layer dielectric film with the plurality of semiconductor die disposed over the temporary carrier substrate;

curing the single layer dielectric film after placing the plurality of semiconductor die on the surface of the single layer dielectric film;

encapsulating the plurality of semiconductor die on the single layer dielectric film with an encapsulant while the temporary carrier substrate supports the single layer dielectric film and the plurality of semiconductor die;

patterning the single layer dielectric film and leaving a portion of the single layer dielectric film disposed over an active surface of the plurality of semiconductor die; and

forming a conductive layer directly on, and extending across, the second surface of the patterned single layer dielectric film and over the plurality of semiconductor die.

7. The method of claim 6, wherein a composition of the encapsulant is the same as a composition of the single layer dielectric film.

8. The method of claim 6, wherein the single layer dielectric film comprises a thickness in a range of 5-50 micrometers, a glass transition temperature (Tg) in a range of 140-190 °C., and further comprises 50-90% of ceramic filler or silica filler by weight.

9. The method of claim 6, further comprising using laser ablation to form both vias and a redistribution layer trace pattern openings in within the single layer dielectric film, the RDL trace pattern intersecting with the vias in the single layer dielectric film in a stair step fashion.