The invention concerns a method for the expansion of a digital signal according to the preamble of claim 1 as well as a circuit arrangement for the implementation of the method.

From DE-A-37 22 172 there is known a method for the magnification of the spatial dimensions of a picture, in which the magnification of the amplitude of the vertical deflection is combined with a digital magnification of the signal in the horizontal direction. With this method, owing to the magnification of the signal in the horizontal direction. With this method, owing to the magnification of the amplitude in the vertical deflection, the number of lines in the vertical direction is reduced so that the line structure becomes visible. The visibility of the line structure can be drastically reduced if a double scanning deflection is used such as described in DE-A-37 22 170. The solution described therein uses standard RAM modules as memories.

It is the object of the invention to provide a method as well as a circuit arrangement for the modification of the spatial dimensions of a picture.

This task is solved by the features of claim 1. Further developments of the invention are given in the dependent claims.

With the solution according to the invention, a video memory with two periphery interfaces is used such as described in DE-A-37 33 012 (EP-A-0 309 807).

For the modification of the spatial dimensions of a picture using the above mentioned picture memory two methods are possible.

1. The data are written into the memory without prior expansion. The expansion of the picture data is performed during the reading-out of the picture memory.

2. The expansion of the data is performed during the writing of the data into the picture memory. The picture memory is then read out line by line for the reproduction.

The picture memory used in accordance with the invention has the following features:

The two peripheral interfaces of the video memory are fed with clock pulses, the rate of one of which is an integral multiple of the other. For example, the following combination may be used:

input A	13.5 MHz	13.5 MHz	27.0 MHz	27.0 MHz
input B	27.0 MHz	13.5 MHz	13.5 MHz	27.0 MHz

In order to achieve the required reading and writing speed the transmission between the peripheral interfaces and the memory is conducted in parallel manner. The data are transmitted in blocks of, for example, twelve scanning values.

Owing to the high data rate which requires a very high access time of the memory the peripheral interfaces are able to read blocks of, for example, 24 scanning values.

The invention is explained below in more detail with reference to two embodiments which are shown in the drawing.

Fig.1 shows a memory organisation for the double

scanning mode;

Fig.2 shows a time diagram of the input and output data;

Fig.3 shows a buffer;

Fig.4 shows a time diagram of the clock pulse adaptation circuit;

Fig.5 shows a further time diagram of the input and output data;

Fig.6 shows a circuit arrangement for the expansion of the luminance components;

Fig.7 shows a circuit for the expansion of the chrominance components.

Fig.1 shows a memory organisation of a memory 14 with a double scanning mode. The data are written into the memory 14 as follows:

A first horizontal counter 11 controls the writing data of one line, a first vertical counter 12 controls the writing of the luminance components Y of one column and a vertical counter 13 controls the writing of the chrominance components of one column. The data are written block-wise into the memory, whereby a block may contain, for example, twelve scanning values. The data of the blocks contain luminance Y and chrominance signal components C alternately.

The reading of the data is performed in the following way:

The memory 14 has a first horizontal read counter 16 for

the luminance Y. These data are fed to a first peripheral interface B. The vertical write counter 13 is used for the read cycle as a vertical read counter 13 for the chrominance signal components C for the peripheral interface A. For the luminance signal component Y a vertical read counter 15 is used which feeds the data to the peripheral interface B. The horizontal write counter 10 is used for the read cycle as a horizontal read counter and feeds the chrominance signal components C to the peripheral interface A. The peripheral interfaces A and B are used to read out the data in doubled manner, the chrominance C is fed to the interface A and the luminance Y is fed to the interface B.

Fig.2 shows a time diagram of the input data D_{in} and the output data at the peripheral interfaces A and B. The input data D_{in} are alternately fed to the memory 14 as luminance components Y and chrominance components C. When the data are read out of the memory 14 the chrominance components C1, C2,... are fed to the peripheral interface A while the luminance components Y1, Y2, ... are fed to the peripheral interface B. As can be seen from Fig.2, the luminance components Y5, Y6 and the chrominance components C5, C6 are read out repeatedly. For the reading out process two components C2, C2; Y1, Y2 ... are combined in each case into one block.

If, for examples, the write clock pulse rate is 27 MHz and a picture magnification in a ratio of 4/3 is to be achieved, the read pulse rate must be 20.25 MHz. The memory 14 is read at a read frequency of 27 MHz. Through a special read-out method, however, an average frequency of 20.25 MHz is obtained.

In order to achieve the average frequency of 20.25 MHz, one block out of every four blocks with, for example, 24 samples is read out in repeated manner. For example, the third block can be read out in repeated manner so that the horizontal error is prevented from increasing.

In order to attain this read out frequency, a buffer according to Fig.3 is used. The data D_{in} are fed to shift registers 20,21,22 in parallel manner. These shift registers 20,21,22 are each followed by a controllable amplifier 23,24,25 the combined output of which lead to an output D_{out}. The shift registers 20,21,22 have control inputs CK1, CK2 and CK3. The controllable amplifier 23,24,25 have control inputs EN1, EN2, EN3.

Fig.4 shows a time diagram of the buffer according to Fig.3. The input data D_{in} consists of four blocks BO to B3. During a first block period the data of the block W_{BO} are written into the shift register 20. During a second block period B1 the block W_{B1} is written into the shift register 21. In a third block period B2 the data from the block W_{B2} are written into the shift register 22. This block period B2 is repeated without carrying out a writing process in order to obtain the average frequency of 20.25 MHz. In a fourth block period B4 the data of the block W_{B3} are written into the shift register 20. The writing process is performed at a clock pulse frequency of K = 27 MHz. In order to achieve an expansion, the data of the blocks BO to B3 are read at an average frequency of 20.25 MHz. For this, an enable signal EN1, EN2, EN3 is fed to the inputs of the controllable amplifiers 23,24,25. The duration of the enable signal corresponds to 20.25 MHz and is shown in Fig.4 with the duration 31.

Fig.5 shows the writing of the input data into the memory 14 as well as the organisation of the luminance components Y and the chrominance components C after the writing into the memory 14. During the writing of the luminance components Y by means of the counters 12,11 and the chrominance components C, regions ND of the memory are not written into. For the reading-out process the data are read out in order corresponding to the way in which they were written into the memory and are fed to the peripheral interface A,B in a Y/C component manner.

Fig.6 shows a block circuit diagram of an embodiment according to the invention. An incoming signal path 10 for the luminance signal Y with an analog-to-digital converter 70 is split up to a first read-write memory 68 and a second read-write memory 79 and subsequently, via a multiplexer 74, re-combined to an outgoing signal path 13 for the luminance signal Y with a digital-to-analog converter 77. The read-write memories 68 and 79 are provided with data inputs, data outputs, read-write control inputs and address inputs. The address inputs of the read-write memories 68 and 79 are connected to counter outputs of address counters 64 and 81 which in turn have reset inputs as well as clock pulse inputs. The reset inputs are triggered by means of multiplexer 63 and 80 and the clock pulse inputs are triggered by means of multiplexers 65 and 82. For reasons of clarity, the individual control lines are not shown, rather only the signals are indicated at the respective control input or output terminals. The control signals are the switching signals $f_{H/2}$ and $f_{H/2'}$, i.e.. the inverse signal with respect to $f_{h/2}$. These signals are symmetrical switching signals and change their states after each line period of the picture signal that is transmitted or reproduced. The switching signals serve

for the alternating switching-over of the read-write memories 68 and 79 by means of control inputs from the operating mode "writing" to the operating mode "reading" and vice versa. In addition, a demultiplexer 74 is triggered by the switching signal $F_{H/2}$, so that during each line period alternatingly the data output of the read-write memory 68 and the data output of the read-write memory 79 are switched through to the outgoing signal path. Finally, the multiplexers 63, 65 are switched by the switching signal $f_{H/2}$ and the multiplexers 80, 82 are switched by the inverse switching signal $f_{H/2}$.

The control signals $f_{H/2}$ and $2f_H$ are reset signals for the counters 64 and 81 as described in P 37 22 170 in Fig. 1c and d.

The frequency of the reset signal f_4 corresponds in amount with the line frequency of the picture that is transmitted or reproduced, and the frequency of the signal $2f_H$ corresponds in amount to the line frequency of the picture displayed. In this case, the frequency of the signal $2f_H$ is twice as high as the frequency of the signal f_4. Finally, clock pulse signals are generated which are fed to the counters 64 and 81 at the clock pulse inputs via the multiplexers 65 and 82. These are clock pulse signals f for the operating mode "writing" and clock pulse signals 2f for the operating mode "reading". The frequency of the clock pulse signals f, 2f corresponds to the number of picture elements of each line multiplied by the respective line frequency. In the present case the clock pulse frequency of the signal 2f is consequently twice as high as that of the signal f.

The picture signals are fed via the incoming signal path

10 in digital form to the data inputs of the read-write memories 68 and 79. It is assumed that at the time t_o the read-write memory 68 is set to the operating mode "writing" and the read-write memory 79 to the operating mode "reading". Then, the multiplexer 63 is controlled in such a way that it switches reset signals f_H through to the reset input and the multiplexer 80 is controlled in such a way that it switches reset signals 2f through to the input of the counter 81. The multiplexer 65 is also switched in such a way that it switches clock pulse signals f through to the clock pulse input of the counter 64 and the multiplexer 82 switches clock pulse signals 2f through to the clock pulse input of the counter 81. Subsequently, the picture data of the line n are written into the read-write memory 68 all required storage locations being addressed one after the other. The picture data of the preceding line n-1 were already written in the read-write memory 79, and these data are now read out at the time t_1 and fed to the outgoing signal path 13 via the demultiplexer 79. In the available period of time between t_1 and t_o the storage locations in the read-write memory 79 are addressed in two coincident cycles, i.e. the picture signals are read out twice. Subsequently, the read-write memories 68 and 79 are switched over to the respective other operating modes, i.e. from the read-write memory 68 the prior stored picture signals are read out and the picture data of the line that is presently transmitted or reproduced are written into the read-write memory 79. Thus the prior stored picture data are lost. The demultiplexer 74 is switched over in order to switch the output of the read-write memory 68 to the outgoing signal path 13. This described process is repeated after each line period of the picture signal transmitted or reproduced.

The address outputs of the counter 64 lead to a

peripheral interface A, and the address outputs of the counter 81 lead to a peripheral interface B.

Fig.7 shows the signal processing for the chrominance signal components U, V. The control signals are fed to the read-write memories 66, 71 via the interfaces A,B. The signal processing is carried out in a way analogous to Fig.6. The chrominance signal components are fed to a multiplexer 96 via an incoming signal path 54. The signal components U, V are then fed to the multiplexer 96 via filters 90, 91, A/D converters 92, 93 and D flipflops 94, 95. The multiplexer 96 is followed by a serial-to-parallel converter 83 the output data from which are fed to the read-write memories 66,71. The output data of the read-write memories 66,71 are fed, via a multiplexer 84 and a D flipflop 85, to an outgoing signal path 55, which consists of a demultiplexer 86 as well as a D flipflop each 98,99 with a digital-to-analog converter each 50,51 and a filter 52,53.

The A/D converters 92,93 and the multiplexer 96 are clocked at half the clock pulse signal f/2, the D flipflop 85 at twice the clock pulse signal 2f and the serial-to-parallel converter 83, the multiplexer 86, the D flipflops 98,99 and the D/A converters 50,51 are clocked by the clock pulse signal f.

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Claims

1. A method for the expansion of digital signals with an expansion ratio of M:N with M>N, in which picture point values are written in blocks into a memory (14) and thereafter are read out of said memory, characterised in that the memory can be separately addressed for rows and columns of the video signal during reading and during writing, the writing and reading clock rates being the same, and in that in each case M blocks of picture point values are read in or out, in which after the reading out in each case only the picture point values of N blocks are used further and fed to subsequent intermediate stores (20,21,22) which supply expanded, continuous video signals with a clock rate reduced according to the factor N:M.

2. A method according to claim 1, characterised in that the memory (14) can be addressed separately for luminance values (Y) and chrominance values (C).

3. A method according to claim 2, characterised in that for the addressing of rows of chrominance values (C) a similar vertical counter (13) is used during writing and during reading.

4. A method according to one or more of claims 1 to 3, characterised in that M=4 and N=3.

5. A method according to one or more of claims 1 to 4, characterised in that there is used as the memory (14) a video store with two peripheral interfaces (A,B) and during the reading out the luminance values are supplied to the first interface (B) and the chrominance values are supplied to the second interface (A).