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(54) ELECTRONIC COMPUTER

(71) We, SHARP KABUSHIKI KAISHA (formerly known as Hayakawa Denki Kogyo Kabushiki Kaisha), a Japanese Company, of 22-22, Nagaike-cho, Abeno-ku, Osaka 545, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —

This invention relates to an electronic computer, especially to a serial-type electronic computer, and seeks to provide a serial-type computer which is small, which is light in weight, affords high speed operation, exhibits simplified shifting operation and includes means of simply erasing unnecessary "0"s above the most significant digit at the time of visual presentation of the result of the operation.

In the field of electronic computers, minimizing the size and weight is highly desirable, and especially in the case of table type electronic computers. The decisive factors for such small and light computers are to minimize the weight of the parts, to minimize the number of parts, integration of the parts and to minimize the size of the parts. With this in view, a magnetic memory matrix which having high density and reliability is advantageous, and many have been utilized as a memory in large size electronic computers. However, since it requires reading and writing operations at the time of receiving and giving informations it is not very suitable for a register in which the frequency of receiving and giving information is high. For the register of an electronic computer the use of the magnetic memory matrix has therefore been avoided, and in many cases flip flops have been used. But, if the magnetic memory device can be utilized in the register, it greatly aids the computer being made small and light. In applying the magnetic memory device to the register, it can be assumed that various computer operations should be based upon the repetition of read period and write period per each one bit time alternatingly. More specifically, information of one bit is read out, then it is transmitted to each unit of an operation device, and subsequently and immediately it is written into the original address. However, even if said method is employed there are still various difficulties encountered. For example, in the case where numeral value information is to be registered in the form of binary coded decimal code (1 digit = 4 bits) in a core matrix plane and this information is to be addition (subtraction) processed by a pure binary added (subtracter), it is a well known fact that if a decimal carry (borrow) is produced a correction operation by $+6$ (-6) is necessary. According to the above-mentioned read and write alternative repetition system, four times of repetition of alternate read and write periods per one bit are made in one digit time, and based upon said digit time, addition (subtraction) processing is performed. Thus, said system requires one digit time (8 bit time) for each pure binary addition (subtraction) processing and decimal correction respectively. Thus, two digit time (16 bit time) in total is required for addition (subtraction) processing of one digit unit. On the other hand, in the case of a flip flop register, the required time for said one digit unit addition (subtraction) processing is 7 to 8 bit time. Since the addition (subtraction) processing is a basis of multiplication (division) operation, shortening of the processing time is very desirable.

In a decimal correction operation, in practice, the output of a pure binary addition (subtraction) operation is stored in a register, the presence or absence of a decimal carry (borrow) is judged from the contents thereof. If it is judged that decimal carry (borrow) is present a converter disposed between digits of the register is operated according to the judgement in order to apply a conversion operation of $+6$ to the addition (subtraction)

output, and, thereby, a correction to a decimal number is performed, but it is necessary to dispose a converter between each pair of adjacent digits in the register.

In order to achieve not only addition (subtraction) processing but also multiplication (division) processing, it is inevitable for the register to have a shift function in order to transfer numeral values stored therein to the adjacent digits respectively, but the magnetic memory matrix which has been used as a memory is not provided with such a shift function as this. Further, even if it is decided to provide the magnetic memory matrix with a shift function in addition to the read and write function in accordance with the aforementioned alternating repetition system there will be the disadvantage that, although it may seem possible to make a leftward shift by having the read out numeral value temporarily memorized externally, then capturing next write period, and writing it in the adjacent upper digit, in the case of rightward shift it is impossible to capture the write period corresponding to the adjacent lower place digit immediately after a numeral value is once read out. As in the case of flip flop register, the leftward shift operation must be repeated for the number of times corresponding to the whole digit number minus one, and thus, particularly in the case of the rightward shift operation, it takes a considerable time.

Further, in the case of an electronic table type computer, it is necessary externally to indicate the operation result or the registered contents, and as an output apparatus thereof numeral indicating tubes are used. The indicating device, in general, is directly coupled to the register, and since the contents of the register to be indicated involves many "0"s appearing in the upper spaces above the effective numeral value, there is the disadvantage that the effective numeral value, especially the most significant digit, can not be readily recognized. In order to erase such unnecessary "0"s it has been suggested that a judging logic gate and NOT circuit respectively be provided for each of the whole digits of the register so that, whether the contents of the digits above the k-th place digit respectively are "0"s or not is judged, and based upon the result of said judgement, "0" indication above the k-th place digit is suppressed, but this requires a very complicated additional circuit.

This invention seeks to solve these problems together, by employing in a serial-type computer, a magnetic memory matrix for the register so that the occupied area is reduced to a large extent compared to the case of a flip flop register, thereby the size and weight of the computer, especially a table type computer, is minimized, and at the same time the operation processing is speeded up and simplification of the operation device and simplification of the shift operation are now realized.

Additionally, but briefly explaining the above, the computer is so arranged that the conventional read and write operations with respect to the magnetic memory device are improved so that it is not necessary to employ the aforementioned read and write alternating repetition system. When an addition (subtraction) of binary coded decimal numbers is processed, a pure binary addition (subtraction) processing is performed during the read period. At the next write period, a decimal correction operation is performed. By thus reducing the time required for decimal addition (subtraction) processing of one digit unit to about half the time required by said read and write alternating repetition system, the operation processing efficiency is greatly speeded up, almost to that of a flip flop register. After pure binary addition (subtraction) processing is performed during the read period, the addition (subtraction) output together with a correction signal of $+6$ (-6) is returned to the same adder (subtracter) to apply a correction operation thereto without using a separate pure binary adder (subtracter), and thus by fully utilizing just one adder (subtracter) the operation unit is now simplified.

Still further, it is so arranged according to a substantial feature of this invention in connection with the above mentioned read and write operations, especially in the case of rightward shift, that after a numeral value is once read out the write period corresponding to the lower place digit is immediately captured and said read out numeral value is promptly written in said lower place digit. Thus both of rightward shift operation and leftward shift operation can be very easily performed. At the time of the indication of an operation result, on the other hand, the numeral value stored in the magnetic memory device as a result of the operation is read out from the most significant digit. Then, just one flip flop is set by the most significant digit (which is not zero) of the effective numeral value which appears first. An indicating tube driving circuit is operated by this set output, and thereby the indication of any meaningless "0" is eliminated.

In order that the invention may be clearly understood and readily carried into effect, apparatus in accordance therewith will now be described, by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a diagram showing the layout of an electronic computer,

Figures 2(1) to 2(12) show blocks or symbols of circuits, and diagrams of concrete examples of circuits represented by the symbols,

Figures 3(1) to 3(9) are diagrams showing various kinds of timing signals for synchron-

ously controlling the computer of Figure 1 and concrete examples of devices for generating said signals,

Figures 4(1) to 4(3) are diagrams showing the construction of registers used in the computer of Figure 1,

Figures 5(1) to 5(4) are diagrams showing details of an added (subtracter),

Figures 6(1) to 6(3) are diagrams demonstrating shift operations in core registers, and

Figures 7(1) and 7(2) are diagrams showing an output indicating device.

Outline of the Computer

Shown in the drawings is an actual example of a table type electronic computer, and the whole constitution thereof can be classified into two, an operation unit and a control unit. The operation unit comprises main registers 1 and 2, buffer registers 3 and 4, an indicating buffer register 5, a decimal point register 6, an adder (subtracter) 7 and a key board 8. The control unit comprises a programme device 9, an address counter 10, a conditional flip flop 11, a clock pulse generator 12, and a timing signal generator 13. Further, a power source unit 14 is provided. By the way, the numeral value handled by the computer as a whole is of binary coded decimal coded representation (1 digit = 4 bits).

Both of the main registers 1 and 2 are constituted of magnetic memory devices respectively, and these store first operand, second operand or operation result. The storage capacity of each of said registers is in maximum 16 digits (16 × 4 bits) of binary coded decimal number. Only the register 1 is directly coupled to the indicating device so that its storage contents can be immediately indicated externally. Detailed internal structures of these registers will be explained later. The buffer registers 3 and 4 are connected to the main registers 1 and 2, and each comprises four flip flops. Each has a capacity of one digit component. These buffer registers are for temporarily memorizing the contents read out from the main registers 1 and 2. The adder 7 is capable of performing pure binary addition (subtraction) processing, and is a full adder (subtracter) to which addition input signals a_1 and a_2 and a carry (borrow) input signal F_c representative of a carry (borrow) from lower place digit are applied. In addition, a carry (borrow) memory device is provided, but the details thereof will be explained later. The buffer register 5 is required at the time of externally indicating an operation result or registered contents by means of gas sealed glow discharge tubes, that is for temporarily memorizing the contents to be indicated and thereby for obtaining a decimal output according to which the discharge tubes are to be actuated. The decimal point register 6 is composed of four flip flops and has a one digit capacity, and serves a function of storing the position of the decimal point of numerical value as a numerical information. The keyboard 8 has various operation control keys, such as digit keys, operation command keys and clearing keys, and relays incorporated therewith.

The programme device 9 comprises a diode matrix and generates micro-orders required for performing various operations. These micro-orders are supplied to the inputs of logic gates respectively disposed between various units which constitute the device for controlling the flow of numerical information. In the diode matrix, for example several input address lines are prepared for multiplication operation and, when one of the address lines is selected, output lines coupled thereto through diodes are driven to generate several kinds of micro-orders which are used to control transfer of the information between the corresponding units. The address counter 10 designates in order programme address lines as the operation process progresses. The conditional flip flop 11 judges the internal states of various devices as is necessary during the development of the operation processing. According to the output of the conditional flip flop 11, the programme address lines are divided and selected so that micro-orders as required are generated and thereby the efficiency of the operation processing is enhanced.

In addition to the above mentioned, there are provided some judging flip flops within the computer. The clock pulse generator 12 generates clock pulses which are the basis of synchronous control of various devices. The timing signal generator 13 generates a bit time notifying signal, a digit time notifying signal and read and write instruction signals by modifying said clockpulses in various ways. These generators are described below. In the drawings, only the major portion, but not all, of the information transmission lines between devices is shown.

Before explaining in detail each unit of the device a brief explanation will be given, referring to Figure 2, of the logic symbols or blocks representative of basic circuits of the electronic computer and examples of typical circuits.

For a logic product, the logic block shown in Figure 2(1) is used, and an equivalent circuit is shown in Figure 2(2). A plurality of diodes (three diodes are shown in the drawing) 21—23 are connected in parallel to a load resistor 24. The connecting point is made an output terminal, and the other ends of said diodes 21—23 are used as input terminals. For a logic sum, the logic block shown in Figure 2(3) is used, and the circuit shown in Figure 2(4) is employed. The circuit is same as that shown in Figure 2(2) except that the polarity of diodes 25—27 and the polarity of a source of voltage supplied through a load resistor 28 are opposite. For an inverter, the

logic block shown in Figure 2(5) is used, and is shown in Figure 2(6) a transistor 29 is provided, to the base of which input signals are introduced through a resistor 30, and an inverted output of the signal is derived from the collector of the transistor 29. Further, a clamp diode 31 and a load resistor 32 are connected to the collector, and a bias resistor 33 is connected to said base. An emitter follower is represented by the logic block shown in Figure 2(7), and it is only provided with a transistor 34 and a load resistor 35 as is shown in Figure 2(8). The output signal is derived from the emitter of said transistor. For the bistable flip flop, the logic block shown in Figure 2(9) is used. As is shown in Figure 2(10) it is provided with two transistors 36 and 37, and the base of one transistor is d.c. coupled to the collector of the other transistor through resistors 38 and 39 respectively. Each of the collectors thereof is connected to a power source through load resistors 40 and 41 respectively, and the emitters are grounded. A bias voltage is applied through resistors 42 and 43 to the respective bases thereof. Said flip flop further comprises resistors 44 and 45, condensers 46 and 47 and diodes 48 and 49 as trigger gates. For an exclusive logic sum, the logic block shown in Figure 2(11) is used, and it is so arranged, as is shown in Figure 2(12), that two transistors 52 and 53 are provided. The base of one transistor is coupled with the emitter of the other transistor across resistors 54 and 55 respectively, and the input signal is introduced into each of the coupling points. The collectors of these transistors are connected to a common point which, in turn, is connected to a power source voltage through a load resistor 56, and an output signal is derived from said common point.

Timing Signal

The basis of various timing signals for synchronously controlling the serial type operation device as a whole is the clock pulse CP which is obtained from the clock pulse generator 12. The basic frequency thereof is 100 KC, and the time interval thereof is 10μ sec. The clock pulse GP from the clock pulse generator 12 is shown in Figure 3(1). As the pulse generator 12, a multivibrator which oscillates at 100 KC is used, and by supplying the output therefrom to the timing signal generator 13 different timing signals are produced. In practice, as is shown in Figure 3(1), two stage inverters 61 and 62 are connected to the output side of the pulse generator 12, and clock pulse CPB for producing the timing signals is derived from the output end thereof. Said clock pulse CPB is in reverse phase relation with respect to the clock pulse CP shown in Figure 3(2). The clock pulse for driving matrix cores, CPCO, is obtained through two stage inverters 63 and 64 and a pulse width enlarging condenser 65 from the pulse generator 12. The timing signal generator 13 comprises eight bistable flip flops in total 71, 72, 73, 74, 75, 76, 77 and 78 and a decoder, and by simply cascade connecting four flip flops 71, 72, 73 and 74 as is shown in Figure 3(3) the well known octal notation counter 79 which performs frequency division operations is constituted. Operation wave forms of each part thereof are shown in Figure 3(4). The flip flops 71 and 72 as a whole are co-operating to work as a quaternary notation counter, and output signals B1 and B2 therefrom are utilized for producing bit time signals $\phi_1 - \phi_4$ which represent bit times $t_1 - t_4$. The establishing condition of the bit time signals $\phi_1 - \phi_4$ is as below:—

$$\phi_1 \text{ ——— } \overline{B1}.\overline{B2} = \overline{(B1 + B2)}$$
$$\phi_2 \text{ ——— } B1.\overline{B2} = \overline{(\overline{B1} + B2)}$$
$$\phi_3 \text{ ——— } \overline{B1}.B2 = \overline{(B1 + \overline{B2})}$$
$$\phi_4 \text{ ——— } B1.B2 = \overline{(\overline{B1} + \overline{B2})}$$

The decoder for actually obtaining the bit time signals $\phi_1 - \phi_4$ is shown in Figure 3(5). Therein, conversion output signals or the bit time signals $\phi_1 - \phi_4$ are obtained through OR gates 81 — 84 each consisting of two diodes and transistor inverters 85 — 88. The state of the flip flop 73 is inverted per each 4 bit time, and its state $\overline{WF}$ is utilized as a read instruction and its state WF is utilized as a write instruction with respect to the core matrix plane (the registers 1 and 2). The state of the flip flop 74 is inverted per each 8 bit time, and the period of its output D1 corresponds to one digit time T_1. The relation of these timing signals is shown in Figure 3(6). It should be noted especially that the read period and write period continue for four bits respectively. In other words, as was previously explained, this is different from the conventional system in which read and write are repeated per each one bit, the read and write according to this invention being repeated per each one digit unit of numeral value information. This largely facilitates the simplification of the operation device and the speeding up of the operation efficiency. More specifically, this point is the basis of this invention. It is not different from the conventional system in that the information is read out from the magnetic memory matrix per each one bit, but the specific feature of this invention is that the read operation is continued covering one digit unit instead of one bit unit of the numeral value information. The read out contents are temporarily stored in parallel in the buffer register 3 having one digit capacity, and subsequent to said read cycle, write operation is similarly performed for the time or for the

number of times corresponding to one digit unit.

The flip flops 74—78 as a whole, on the other hand, constitute a notation counter, and each of outputs D1—D5 therefrom is utilized for producing signals ϕ_0—ϕ_{19} which represent digit times T_0—T_{19}. In this case, 2^5 states in total can be taken, but since in practice 20 states only are required, the balance, 12 states, are cancelled, and a jumping operation to return back to the first state is performed. Further, as it is necessary at the time of rightward shift to invert the counter, a simple cascade connection will not do. In addition, the logics of the set input side and the reset input side inevitably become complicated, and, therefore, a special arrangement is provided therein in order to overcome these problems as will be explained later.

As is shown in Figure 3(7), the logic constitution of the input side of the flip flops 75—78 is represented by the following equations. In the equations, FF is a flip flop, RS is an inversion instruction signal, and Rg is a jump instruction signal.

$$\begin{aligned}
&\text{FF 75 set input} && = RS \cdot \overline{D2} + \overline{RS} \cdot \overline{D2} \\
&\text{FF 75 reset input} && = RS \cdot D2 + \overline{RS} \cdot D2 \\
&\text{FF 76 set input} && = RS \cdot Rg \cdot \overline{\phi_1} + RS \cdot \overline{D3} + \overline{RS} \cdot \overline{\phi_{19}} \cdot \overline{D3} \\
&\text{FF 76 reset input} && = RS \cdot D3 + \overline{RS} \cdot D3 \\
&\text{FF 77 set input} && = RS \cdot D4 \cdot \overline{\phi_1} + \overline{RS} \cdot \overline{D4} \\
&\text{FF 77 reset input} && = RS \cdot D4 + \overline{RS} \cdot D4 \\
&\text{FF 78 set input} && = RS \cdot \overline{Rg} \cdot \overline{\phi_1} + RS \cdot \overline{D5} + \overline{RS} \cdot \overline{D5} \\
&\text{FF 78 reset input} && = RS \cdot D5 + \overline{RS} \cdot D5 + \overline{RS} \cdot \overline{\phi_{19}}
\end{aligned}$$

The condition of the establishment of the digit time signals is listed below with reference to Figure 3(8) in which operation wave forms of the flip flops 74—78 are shown.

$$\begin{aligned}
\overline{\phi_0} &\text{ ——— } \overline{D1} \cdot \overline{D2} \cdot \overline{D3} \cdot \overline{D4} \cdot \overline{D5} && = \overline{(D1+D2+D3+D4+D5)} \\
\overline{\phi_1} &\text{ ——— } D1 \cdot \overline{D2} \cdot \overline{D3} \cdot \overline{D4} \cdot \overline{D5} && = \overline{(\overline{D1}+D2+D3+D4+D5)} \\
\overline{\phi_2} &\text{ ——— } \overline{D1} \cdot D2 \cdot \overline{D3} \cdot \overline{D4} \cdot \overline{D5} && = \overline{(D1+\overline{D2}+D3+D4+D5)} \\
&\vdots \\
\overline{\phi_{19}} &\text{ ——— } D1 \cdot D2 \cdot D3 \cdot D4 \cdot D5 && = \overline{(\overline{D1}+\overline{D2}+\overline{D3}+\overline{D4}+\overline{D5})}
\end{aligned}$$

The structure of the decoder for actually obtaining the digit time signals $\overline{\phi_0}$—$\overline{\phi_{19}}$ may be similar to that of the case of aforementioned bit time signals, and a part thereof is shown in Figure 3(9). As can be seen from said drawing, said decoder comprises a plurality of diodes 91—95 which form a logic sum 96, and a transistor inverter 97.

Structure of Register

In an actual example of the register, a core matrix plane is used. The core in general is a small annular core made of a ferromagnetic material, and by making positive and negative states of its residual magnetic flux correspond to "0" and "1" it is made to memorize binary value information. In order to derive its memory contents, it is necessary to cause a current $+I_m$ exceeding its coercive force to flow through driving lines as is shown in Figure 4(1), and herein a current coincidence system is employed as the driving method. This means that cores are arranged in a matrix, a current of $I_m/2$ is caused to flow through its column direction driving line and row direction driving line respectively so that a current of $I_m/2 + I_m/2$ flows through a core at the crossover of said two lines, thus the core at the location where the selected column direction driving line and the selected row direction driving line coincide is selected and at the same time the information therein is read out or information is written therein. It is necessary, of course, to make the flow direction of the read current pulse and the write current pulse mutually opposite.

In this arrangement, a transistor switching device is adopted for selecting the row and column drive lines so as to improve the efficiency as compared with that of conventional systems.

The structure of a transistor having two p-n junctions in general is symmetrical, and amplification can be recognized at both junc-

tions between the emitter and collector and between the collector and emitter, but with a little difference in the degree of amplification. In the case of the forward direction (emitter to collector), as is shown in Figure 4(2), when a base current ieb flows, a current ieb × β can be obtained at the collector side. On the other hand, in the case of reverse direction (collector to emitter), when a base current icb flows, a current icb × β' can be obtained at the emitter side. β is a forward direction amplification factor and β' is a reverse direction amplification factor. In applying the above mentioned principle, the transistors are utilized as bidirectional switching devices for the selection of the column and row direction driving lines.

The computer shown in the drawings comprises two core registers 1 and 2 for simultaneously registering a first operand and a second operand consisting of a binary coded decimal number of 16 digits (16 × 4 bits), for example. As is shown in Figure 4(3), (16 × 8) cores, 16 units in the column direction driving lines 101—116, and 8 units in the row direction driving lines 121—128 are provided. These two kinds of the driving lines extend mutually orthogonally, penetrating through the cores to form a matrix. Further, the registers 1 and 2 are respectively provided with independent sense lines (not shown). The driving lines 101—116 and 121—128 are provided respectively with transistors 131—146, and 151—158, which perform the aforementioned bidirectional switching operation. The column direction of the matrix corresponds to the digit position of the register, and the row direction thereof corresponds to bit position of each digit. The left end of the column direction corresponds to the least significant digit, and the upper end of the row direction corresponds to the least significant bit. In practice, the selection transistors of the column direction are driven in synchronization with the respective corresponding digit times (T_2—T_{17} out of T_0—T_{19}). A half value current $I_m/2$ is caused to flow therethrough to select the digit position. The transistors in the row direction, on the other hand, are driven in synchronization with the respective corresponding bit times (t1—t4) to select the bit position, and the core at the intersection is selected and is driven. For example, where a decimal number 3 (binary number 0011) stored in the second place digit of the register 1 is to be read out, the digit time T_3 is selected to drive the switching transistor so that a half value current is caused to flow through the column direction driving line 102, and the row direction driving lines 121—124 are selected in order and in synchronization with the bit times t_1—t_4. Thereby, at the times $\overline{WFt_1}$ (the bit time t_1 being within the read period — this being applicable also to similar operations hereinafter described) and $\overline{WFt_2}$ an output "1" is obtained from said sense line at each time respectively. At the following times $\overline{WFt_3}$ and $\overline{WFt_4}$ an output "0" is obtained each time respectively, and thus the stored contents of one digit unit (0011) is derived. On the other hand, if the decimal number 3 is to be written in the second place digit thereof, the switching transistor 132 of the column direction is driven during the time WFT3 (the digit time T_3 being in the write period) in order to select the column direction driving line 102, and a half value current is caused to flow through the row direction driving lines 121 and 122 only at the bit times t_1 and t_2. It should be noted that the read operation and the write operation respectively are exclusively performed for 4 bit unit (1 digit unit).

The peripheral circuit of the matrix comprises a read drive amplifier 161, a write drive amplifier 162, read exclusive switches 163—165, and write exclusive switches 166—168. The read drive amplifier 161 consists of a PNP transistor. Read instruction signal $\overline{(WF)}$ is introduced to the base of said transistor. Its collector is connected through a resistor 169 to one end of column direction driving line group and is also connected through resistors 170, 171 and 172 to the bases of NPN transistors which constitute read exclusive switches 163, 164 and 165. The switch 163 is to control the row direction driving line group of the core register 1. The switch 164 is to control the row direction driving line group of the core register 2. The switch 165 is to control the column direction driving line group. A proper bias voltage is applied between the base and the collector of each of the transistors which constitute the switches 163—165. The write drive amplifier 162 also consists of a PNP type transistor, and the write instruction signal (WF) is introduced to its base. Write exclusive switches 166—168 belonging to the amplifier 162 are provided. The switch 166 controls the column direction driving line group, the switch 167 controls the row direction driving line group of the core register 1, and the switch 168 controls the row direction driving line group of the core register 2.

When the read drive amplifier 161 operates, the read exclusive switches 163—165 connected thereto all at once are set to the "ON" state. The lower end of the column direction and the right end of the row direction thereby are set at ground potential, and the potential arrangement becomes such that the half value current of the column direction flows downwardly and the half value current of the row direction flows rightwardly. When the write drive amplifier 162 operates, on the other hand, the write exclusive switches 166—168 are set to the "ON" state, and the upper end

of the column direction and the left end of the row direction are set at ground potential. Thus, by the combination of said read and write drivers and the bidirectional selection transistors, the peripheral circuit of the core matrix registers 1 and 2 is simplified.

Adder (subtracter)

The pure binary adder itself is a full adder having three inputs and consisting of two stage stack circuit of exclusive logic sums 175 and 176 as is shown in Figure 5(1). Its logic constitution is given by the following equation wherein a_1 and a_2 are addition input signals, and F_c is a signal of carry from a lower order.

$$\begin{aligned}\Sigma(a_1, a_2, F_c) &= a_1\,a_2\,F_c + a_1\,\bar{a}_2\,\bar{F}_c + \bar{a}_1\,a_2\,\bar{F}_c + \bar{a}_1\,\bar{a}_2\,F_c \\ &= (a_1\,a_2 + \bar{a}_1\,\bar{a}_2)\,\bar{F}_c + (a_1\,\bar{a}_2 + \bar{a}_1\,a_2)\,F_c \\ &= AF_c + \bar{A}F_c \quad \text{wherein } A = a_1\,a_2 + \bar{a}_1\,\bar{a}_2 \\ &= A \oplus F_c \\ &= (a_1 \oplus a_2) \oplus F_c\end{aligned}$$

The condition of production of carry (borrow) between bits accompanying said addition output is given by the following equation as is well known.

$$\begin{aligned}C^{n+1} &= \overline{Sb}\,(a_1\,a_2 + a_1\,F_c + a_2\,F_c)^n + Sb\,(\bar{a}_1\,a_2 + \bar{a}_1\,F_c + a_2\,F_c)^n \\ &= (a_2\,F_c)^n + (a_1\,\overline{Sb} + \bar{a}_1\,Sb)\,(a_2 + F_c)\end{aligned}$$

wherein Sb is a subtraction instruction signal, and n and n+1 are bit times.

The above two equations are handled in pure binary manner, and the adder (subtracter) herein described requires consideration in regard to decimal correction. Therefore, as is shown in Figure 5(2) a bistable flip flop 177 for memorizing a carry (borrow) between bits (including a carry (borrow) between the uppermost order bit and the lowermost order bit of the next place digit) and a bistable flip flop 178 for memorizing a carry (borrow) between digits are provided. As was aforementioned, the condition of occurrence of said carry (borrow) is pure binary, and if one digit comprises four bits, a carry (borrow) to an upper place digit occurs for the first time at and above 2^4, but in the case of adder (subtracter) herein described for the necessity of converting a pure binary addition (subtraction) result to a binary coded decimal number, a carry (borrow) signal must be produced for all of the numeral values exceeding 9. At the time of production of this decimal carry (borrow) signal Nc, it is necessary not only to judge the presence or absence of binary carry (borrow) signal C which is produced after an addition (subtraction) of four bits but also to judge whether or not the bit values of the second, third and fourth places of the result of addition (subtraction) coincide with the following judgement equation. The carry (borrow) between digits is memorized in the flip flop 178.

$$N_c = d_4 \cdot d_3 + d_4 \cdot d_2 + c = d_4\,(d_3 + d_2) + c$$

Said judgement will be easily understood from the following truth table.

Decimal Number	Carry	Binary Code d_4 d_3 d_2 d_1	Binary Coded Decimal Code	
0		0 0 0 0	0 0 0 0	
1		0 0 0 1	0 0 0 1	
2		0 0 1 0	0 0 1 0	
3		0 0 1 1	0 0 1 1	
4		0 1 0 0	0 1 0 0	
5		0 1 0 1	0 1 0 1	
6		0 1 1 0	0 1 1 0	
7		0 1 1 1	0 1 1 1	
8		1 0 0 0	1 0 0 0	
9		1 0 0 1	1 0 0 1	
10		1 0 1 0	0 0 0 0	$d_4.d_2$
11		1 0 1 1	0 0 0 1	
12		1 1 0 0	0 0 1 0	$d_4.d_3$
13		1 1 0 1	0 0 1 1	
14		1 1 1 0	0 1 0 0	
15		1 1 1 1	0 1 0 1	
16	1	0 0 0 0	0 1 1 0	C
17	1	0 0 0 1	0 1 1 1	
18	1	0 0 1 0	1 0 0 0	
19	1	0 0 1 1	1 0 0 1	

In practice, the output of the adder (subtracter) is once stored in the buffer register 3, and, therefore, at the time $\overline{WFt_4}$ at which addition (subtraction) is over the presence or absence of a decimal carry (borrow) is judged by noting the adder (subtracter) output signal FA and the bit values X_3 and X_4 of the third and fourth places of the buffer register 3. The practical logic constitution of carry (borrow) memory devices 177 and 178 is described below.

In Figure 5(2), in order to judge binary carry (borrow) between bits, a gate network is constituted of an exclusive logic sum 179, two AND gates 180 and 181 and two OR gates 182 and 183. The output signal therefrom is introduced to an AND gate 184 which includes an input terminal to which the signal $\overline{\phi_4}$ is introduced, and further said output signal is introduced also to a carry (borrow) flip flop 177 through an OR gate 185. On the other hand, for the judgement of decimal carry (borrow), in addition to the above mentioned gate network output there are provided OR-AND gates 186 and 187 to which the adder (subtracter) output signal FA and the contents X_3 and X_4 of the buffer register are applied. The output of the OR-AND gates 186 and 187 is applied as an input to an OR gate 188, and it is further introduced

to the other flip flop 178 through an AND gate 189 which includes input terminals to which $\overline{WF}$, the signal ϕ_4 and micro-orders (16) and (17) are introduced. Incidentally when shifting the result of addition (subtraction) processing to the next place digit, it is necessary to make the decimal carry (borrow) signal as a third input signal for the adder (subtracter), and, therefore, an AND gate 190 is provided, and it is transmitted to the flip flop 177 at the time WFt_4. (16), (17), (18), etc., are micro-orders from the programme device 9. (WF) and $\overline{WF}$ respectively are the signals which indicate the write period WF and the read period $\overline{WF}$.

It is necessary in order to convert the result of pure binary addition (subtraction) to a binary coded decimal number to perform a correction operation based upon the result of judgement of said presence or absence of decimal carry (borrow). The aforementioned driving system, in which the read period and the write period respectively are continued for four bit or one digit unit time, is employed in the computer. In the read period $\overline{WF}$ of four bit time a pure binary addition (subtraction) processing of four bits is performed and at the same time the addition (subtraction) result thereof is deposited in the buffer register 3 having a four bit capacity. Then, in the write period WF of four bit time, a correction signal is generated based upon the decimal judgement, and by said correction signal a correction operation is applied to the addition (subtraction) result.

More specifically, the following is performed wherein A and B are two numbers.

(1) In the case of addition

$A + B \geq 10$	The flip flop 178 is set. (A correction by +6 is performed).
$A + B < 10$	(No correction is made).

(2) In the case of subtraction

$A - B \geq 0$	(No correction is made).
$A - B < 0$	The flip flop 178 is set. (A correction by −6 is performed).

In the case of addition, at the time $\overline{WFt_4}$ under the condition of $A+B \geq 10$ the flip flop 178 is set, and during the next write period WF a correction by +6 is applied to the bit time signals ϕ_2 and ϕ_3. In the case of subtraction, if $A-B<0$ a borrow is produced, the flip flop 178 is set without fail, and a correction by −6 is performed.

Figure 5(3) shows the logic constitution of an addition (subtraction) device which actually involves the decimal correction function. In order to perform a pure binary addition (subtraction) during the read period $\overline{WF}$, outputs COX and COY of the registers 1 and 2 respectively are introduced into the adder (subtracter) 7 through AND-OR gates 191, 192, 193 and 194. Then, in order to perform a decimal correction operation during the write period WF, a decimal number 6 is introduced into the adder (subtracter) 7 through AND-OR gates 195 and 194 during the period WFt_2—WFt_3 in response to the decimal carry (borrow) signal obtained at the time $\overline{WFt_4}$, and, on the other hand, output X_1 of pure binary addition (subtraction) passed through the buffer register 3 is introduced thereto through AND-OR gates 196 and 192.

With the information path shown in Figure 5(4) formed of the above mentioned various devices, as the operation progresses, the addition (subtraction) processing of binary coded decimal numbers is completed. In the drawing, 201 and 202 are driving gate networks for the registers 1 and 2, 203 and 204 are gate networks respectively provided at the entrances of the buffer registers 3 and 4, and 205 and 206 are gate networks related to the addition (subtraction) input signals a_1 and a_2.

First, during the read period $\overline{WF}$ consisting of four bit time, the gate networks 201 and 202 are opened in order to drive the core registers 1 and 2, and the numeral value is read out by bit from the least significant digit of each of the registers. These read out numeral values are introduced into the adder (subtracter) 7, and thereby pure binary addition (subtraction) processing of four bits is performed serially. The addition (subtraction) output therefrom is provisionally stored in the buffer register. 3. If a carry (borrow) is present, the carry (borrow) flip flop 178 is set at the time WFt_4, and based upon the result of the carry presence judgement, a correction operation is performed during the next write period WF of four bit time.

During this period WF, the result of addition (subtraction) and the correction signal of +6 (−6) are fed into the same adder (subtractor) 7 and the corrected result of addition (subtraction) is immediately written in a predetermined digit position of the register 1 or 2. Accordingly, there should be no wasted time. Though the summand (minuend) A is previously fed into the register 1, and the addend (subtrahend) B is previously fed into the register 2, the summand (minuend) A is derived from the register 2, since the contents of the both registers are exchanged when the addition (subtraction) operation starts, and written in the register 2 again through the buffer register 4 during the write-in period WF following this operation.

In the case of A+B≥10, the actual operating states of the core registers 1 and 2, the buffer register 3, and the carry flip flops 177 and 178 are set forth in the following table.

EXAMPLE: 5 + 7 = 12

TIME			REGISTER 1				INPUT AT a_1	REGISTER 2				INPUT AT a_2	BUFFER 3				CARRY FLIP-FLOP 177		CARRY FLIP-FLOP 178	
			COX1-4	COX1-3	COX1-2	COX1-1		COY1-4	COY1-3	COY1-2	COY1-1		X4	X3	X2	X1	INPUT Fcin	OUTPUT Fc	INPUT Ncin	OUTPUT Nc
T2	$\overline{WF}$	t_1	0	1	0	1	1	0	1	1	1	1					1			
		t_2		0	1	0	0		0	1	1	1	0				1	1		
		t_3			0	1	1			0	1	1	0	0			1	1		
		t_4				0	0				0	0	1	0	0		0	1	1	
	WF	t_1	1	1	0	0	0	0	1	1	0	0	1	1	0	0	1	1	1	1
		t_2		1	1	0	0		0	1	1	1	0				0	0		1
		t_3			1	1	1			0	1	1	1	0			1	0		1
		t_4				1	1				0	0	0	1	0		0	1		1
T3	$\overline{WF}$	t_1											0	0	1	0	1	1		0

In the above table, COX1−1, COX1−2, COX1−3 and COX1−4 represent first, second, third and fourth bits of the first digit of the register 1, respectively. Similarly, COY1−1 through COY1−4 represent first through fourth bits of the first digit of the register 2, respectively. As shown in the table, the content of COX1−1 appears at the terminal a_1 (Figure 5—4) at time $T2\overline{WF}t_1$, the content of COX1-2 appears at the next time interval $T2\overline{WF}t_2$ and, thus, the information of four bits time are read out after four bit times. At the same time, the contents of COY1—1 through COY1—4 are successively read out from the terminal a_2. They are applied to the adder (subtractor) 7 and its sum (difference) output is stored in the buffer register 3. This sum (difference) output stored in the buffer register 3 is thereafter fed back successively to the terminal a_1 during the time of $T2\overline{WF}t_1$ through $T2\overline{WF}t_4$. On the other hand, a correction signal of +6 (0110) is applied to the terminal a_2 and a correction operation is carried out.

At the time of the various operation processes, it is evident that a function capable of shifting the registered contents of the registers is provided. Though the above mentioned core matrix plane itself has no such shifting function, the device of this invention affords a shifting operation by utilizing the buffer registers 3 and 4 and employing the aforementioned driving system in which the read period and the write period are continued for four bit times, without adding any new device.

More specifically, in such a matrix core register information of one digit unit can be the digit time signals ϕ_2—ϕ_{17}, and, therefore, read out and written in synchronization with together with the utilization of the buffer registers 3 and 4, the digit time signal and the read and write instruction signals are used, and thereby a shift function is provided in the register. An example of leftward shift will be explained below.

Figure 6(1) shows the flow of information of the case where the stored contents of the least significant digits COX_1 of the register 1 is to be shifted to the second place digit COX_2. The shift operation starts from the digit time T_2. During the four bit time T_2 $\overline{WF}$, the reading of the numeral value of the least significant digit is performed, and the read out contents are immediately introduced into the buffer register 3. As the buffer register 3 consists of flip flops, four bits of the numeral value of the least significant digit are registered at the time T_2 $\overline{WF}t_1$, with a time delay.

During the next write period T_2 $\overline{WF}$ of four bit time, the contents of the buffer register 3 are circulated. Further, at the time of the next read period T_3 $\overline{WF}$, four bits of the contents of the buffer register 3 are introduced into the buffer register 4. At this time, however, reading of the information of the second place digit is being performed separately. Then, during the write period T_3 $\overline{WF}$, the contents of the buffer register 4 are written into the second place digit COX_2 of the register 1. In other words, the second place digit of the register 1 is selected in synchronization with the digit time signal $\overline{\phi_3}$ at this time, and, therefore said contents of the least significant digit can be readily written in. At the same time, the numeral value read out from the second place digit separately circulates in the buffer register 3. By repeating said operation at each timing, leftward shift is performed digit by digit.

The operations of COX_1 and COX_2 of the register 1 and the operations of the buffer registers 3 and 4 are shown below.

			COX_1	3	4	COX_2
T_2	$\overline{WF}$	t_1	0 1 1 1			0 0 0 1
		t_2	0 1 1 0	1 0 0 0		0 0 0 1
		t_3	0 1 0 0	1 1 0 0		0 0 0 1
		t_4	0 0 0 0	1 1 1 0		0 0 0 1
	WF	t_1	0 0 0 0	0 1 1 1		0 0 0 1
		t_2	0 0 0 0	1 0 1 1		0 0 0 1
		t_3	0 0 0 0	1 1 0 1		0 0 0 1
		t_4	0 0 0 0	1 1 1 0		0 0 0 1
T_3	$\overline{WF}$	t_1	0 0 0 0	0 1 1 1	0 0 0 0	0 0 0 1
		t_2	0 0 0 0	1 0 1 1	1 0 0 0	0 0 0 0
		t_3	0 0 0 0	0 1 0 1	1 1 0 0	0 0 0 0
		t_4	0 0 0 0	0 0 1 0	1 1 1 0	0 0 0 0
	WF	t_1	0 0 0 0	0 0 0 1	0 1 1 1	0 0 0 1
		t_2	0 0 0 0	1 0 0 0	1 0 1 1	0 0 1 1
		t_3	0 0 0 0	0 1 0 0	0 1 0 1	0 1 1 1
		t_4	0 0 0 0	0 0 1 0	0 0 1 0	0 1 1 1

The logic blocks for the parts of the device used in a shift operation are shown in Figure 6(2). Five AND gates 211—215 are included. Although the adder (subtracter) 7 is present, only one input is introduced into the adder (subtracter) 7 during the shift operation, and no addition (subtraction) operation is performed and said input simply passes through the adder (subtracter).

In the case of rightward shift operation, on the other hand, this is a considerable difference from the well known method. The rightward shift instruction signal RS is generated, and the counting operation of the eicosal notation counter consisting of five bistable flip flops 74—78 is invented by said signal (see Figure 3). More specifically, the counter operation is inverted so that the digit time signals $\overline{\phi}_0$—$\overline{\phi}_{19}$ are generated in the following order:

$$\overline{\phi}_0 \mapsto \overline{\phi}_1 \mapsto \overline{\phi}_{19} \mapsto \overline{\phi}_{18} \mapsto \text{———} \overline{\phi}_2 \to \overline{\phi}_2 \to \overline{\phi}_1 \mapsto \overline{\phi}_0$$

By utilizing the above mentioned digit time signals $\overline{\phi}_{19}$—$\overline{\phi}_0$ of reversed order, the rightward shift operation can be performed within a very short time with an information circulation path which is exactly the same as that of the case of leftward shift. In Figure 6(1), the rightward shift is possible by just substituting COX_2 and COX_1 one with the other and changing T_2 to T_{17} and T_3 to T_{16}. More specifically, since the digit order of read and write of the core register is reversed the incorporation of the write period corresponding to the adjacent lower place digit soon after a numeral value is once read out, can be done very easily in the case of the rightward shift. It is no longer necessary, as is in the conventional well known system, at

the time of the rightward shift by one digit to repeat the leftward shift operation for the number of times equal to the whole digit number of the register minus one. The operation wave forms of the flip flops 74—78 under counter reversed condition are shown in Figure 6(3).

Indicating System

As in the indicating systems of electronic table type computers in general, glow discharge type numeral indicating tubes are used. For driving the tubes, a d.c. static driving system has mostly been used. At the present time, however, a so-called dinamic driving technique wherein indicating tubes are periodically driven by a train of pulses utilizing the persistence of human eyesight has become practical. Now, although the stored contents of the core matrix plane can be derived bit serially, it is impossible to read the contents of all the digits in parallel. From this view point, the dynamic time division indicating system for synchronization with the digit time is convenient, and it is optimum for the output indication of the core matrix plane. Especially, when this system is employed, the advantage is that the number of driver transistors can be reduced. A circuit arrangement for indicating the output is shown in Figure 7(1). An amplifier 216 amplifies the read signal from the sense line of the register 1.

Suppose that a decimal number 7 is memorized in the least significant digit COX_1 of the register 1, the indicating time is in the non-operation cycle, and referring to the circuit arrangement shown in the drawing the operations of COX_1 of the register and the buffer registers 3 and 5 become as shown in the following table:

	COX_1	3
$T_2\ \overline{WFt_1}$	0 1 1 1	0 0 0 0
$T_2\ \overline{WFt_2}$	0 1 1 0	1 0 0 0
$T_2\ \overline{WFt_3}$	0 1 0 0	1 1 0 0
$T_2\ \overline{WFt_4}$	0 0 0 0	1 1 1 0
$T_2\ WFt_1$	0 0 0 0	0 1 1 1
$T_2\ WFt_2$	0 0 0 1	1 0 1 1
$T_2\ WFt_3$	0 0 1 1	1 1 0 1
$T_2\ WFt_4$	0 1 1 1	1 1 1 0
$T_2\ \overline{WFt_4}$	0 1 1 1	0 1 1 1 → 5

If the digit time signals are generated in the order of normal forward direction, the contents of the core register COX_1 are not changed and the numeral value 7 is memorized from the digit time T_3 to the digit time T_1 of the next cycle, and when the digit time T_2 arrives the read and write operations are performed again, and thereby the indicating tube of the first digit is driven and illuminated. In practice, the time that 7 is indicated at the first digit is at the digit time T_8. By repetition of this, the numeral value 7 is externally indicated visually. In the indicating system herein described, however, the inversion operation of the digit counter at the time of rightward shift is utilized, thereby the read and write operations are performed from the most significant digit of the core register, and by using only one flip flop, said flip flop is set by the most significant digit of the effective numeral value which is not zero and which appears first, and an indicating tube driving circuit is operated for the first time by the set output therefrom.

Incidentally, even when "0" is present within an effective numeral value, inversion does not occur when the reset input of said flip flop is used as a digit time signal for indicating the contents of the least significant digit. Only those unnecessary "0"s at the digit higher than the effective numeral value are prevented from being indicated.

Figure 7(2) shows the details of the indicating tube driving circuit. Therein, 13 is a timing signal generator, and 15 is a decoder

for obtaining digit time signals. Switches 220—229 are switched by cathode side driving pulses for selecting the numeral value obtainable from conversion of the registered contents of the buffer register 5. These switches control the paths from the cathodes of indicating tubes 251—266 to ground. Switches 231—246 are switched by digit designating driving pulses or the digit time signals T_{16} —T_1, and control the supply of applied voltage to the anode side of the corresponding numeral indicating tubes 251—266. A set output E ignition controlling bistable flip flop 217 is introduced into the decimal decoder of the cathode side as an another gate input, and controls the operation of the indicating tube driving circuit. By said control, unnecessary "0"s in the indicating device are erased.

WHAT WE CLAIM IS:—

1. An electronic serial-type computer comprising at least one register having a plurality of magnetic memory elements for storing numerical digital information wherein each digit comprises a plurality of binary bits, said register being in the form of a matrix with the rows corresponding to bit positions and the columns corresponding to digit positions, said matrix further including column drive lines, row drive lines, and a signal output, a signal generator for generating a train of bit time control signals indicative of the bit positions, a train of digit time control signals indicative of the digit positions, and a write instruction signal and a read instruction signal co-ordinated with said control signals, first selection means interconnected with the column drive lines and said generator to feed said digit time control signals thereto to select the digits to be written in and read out, second selection means interconnected with the row drive lines and said generator to feed said bit time control signals thereto to select the bits to be written in and read out, and means interconnected with the drive lines and said signal generator to serially write and read numerical information in the order in which said instruction signals are generated.

2. The computer according to claim 1, in which said signal generator generates said write instruction signal during the first half of the digit time control signal and said read instruction signal during the second half of said digit time control signal, and in which connections are provided between said generator and said selection means to feed said control signals thereto to select the digits and bits to be written in and read out.

3. The computer according to claim 1, further comprising at least two registers each having magnetic memory elements, an operation unit including a binary add and subtract device connected to said registers for performing addition and subtraction operations of the numerical information read out of said registers, and correction means interconnected with said operation unit and said registers for applying a numerical correction of $+6$ or -6 to an output of said add and subtract device during the write period immediately following a read period.

4. The computer according to claim 3, in which said correction means includes judge means interconnected with said addition and subtraction device, said judge means determining the need for a correction during the final bit time signal of a read period, and an instruction signal generator for producing an instruction signal in accordance with the determination of the judge means.

5. The computer according to claim 3, further comprising buffer registers interconnected with said add and subtract device for serially storing output signals of said device and judge means connected to said buffer registers and said device for determining the presence or absence of a carry signal from three bits stored in said buffer registers and the output of said device during the final bit time signal of a read period.

6. The computer according to claim 3, in which an addition or subtraction of one digit component is performed during a read period and in the subsequent write period and a signal corresponding to the addition or subtraction result and the correction signal is fed back to said device during the second and third bit time signals during the write period.

7. An electronic serial-type computer substantially as herein described with reference to the accompanying drawings.

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WHAT WE CLAIM IS:—

1. An electronic serial-type computer comprising at least one register having a plurality of magnetic memory elements for storing numerical digital information wherein each digit comprises a plurality of binary bits, said register being in the form of a matrix with the rows corresponding to bit positions and the columns corresponding to digit positions, said matrix further including column drive lines, row drive lines, and a signal output, a signal generator for generating a train of bit time control signals indicative of the bit positions, a train of digit time control signals indicative of the digit positions, and a write instruction signal and a read instruction signal co-ordinated with said control signals, first selection means interconnected with the column drive lines and said generator to feed said digit time control signals thereto to select the digits to be written in and read out, second selection means interconnected with the row drive lines and said generator to feed said bit time control signals thereto to select the bits to be written in and read out, and means interconnected with the drive lines and said signal generator to serially write and read numerical information in the order in which said instruction signals are generated.

2. The computer according to claim 1, in which said signal generator generates said write instruction signal during the first half of the digit time control signal and said read instruction signal during the second half of said digit time control signal, and in which connections are provided between said generator and said selection means to feed said control signals thereto to select the digits and bits to be written in and read out.

3. The computer according to claim 1, further comprising at least two registers each having magnetic memory elements, an operation unit including a binary add and subtract device connected to said registers for performing addition and subtraction operations of the numerical information read out of said registers, and correction means interconnected with said operation unit and said registers for applying a numerical correction of $+6$ or -6 to an output of said add and subtract device during the write period immediately following a read period.

4. The computer according to claim 3, in which said correction means includes judge means interconnected with said addition and subtraction device, said judge means determining the need for a correction during the final bit time signal of a read period, and an instruction signal generator for producing an instruction signal in accordance with the determination of the judge means.

5. The computer according to claim 3, further comprising buffer registers interconnected with said add and subtract device for serially storing output signals of said device and judge means connected to said buffer registers and said device for determining the presence or absence of a carry signal from three bits stored in said buffer registers and the output of said device during the final bit time signal of a read period.

6. The computer according to claim 3, in which an addition or subtraction of one digit component is performed during a read period and in the subsequent write period and a signal corresponding to the addition or subtraction result and the correction signal is fed back to said device during the second and third bit time signals during the write period.

7. An electronic serial-type computer substantially as herein described with reference to the accompanying drawings.

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