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ABSTRACT

METHOD FOR FORMING PLDD STRUCTURE WITH MINIMIZED LATERAL DOPANT DIFFUSION

A new method is provided for the creation of PLDD regions that is aimed at reducing lateral p-type impurity diffusion. The process starts with a silicon substrate on the surface of which gate electrodes have been created. An NLDD implantation is performed self-aligned with the NMOS gate electrode, a layer of oxide (oxide liner) is deposited over the structure over which a layer of nitride is deposited over which a first layer of top oxide is deposited. First gate spacers are formed by etching the first layer of top oxide, stopping on the nitride layer. NS/D and PS/D implantations are performed self-aligned with respectively the NMOS and the PMOS devices, the S/D implantations are annealed. The first gate oxide spacers are removed, a PLDD implantation is performed self-aligned with the PMOS gate electrode. A second layer of top oxide is deposited over the structure and etched to form the second gate spacers on the sidewalls of the NMOS and PMOS gate electrodes. After this sequence of processing steps has been completed, the gate electrodes can be completed following conventional methods of gate electrode processing.

FIGURE 2