This Sheet Has Been Replaced

ABSTRACT OF THE DISCLOSURE

In a semiconductor device having a three-layered buffer layer comprising core layer 1 having interconnected foams such as a three-dimensional reticular structure and adhesive layers 2 provided on both sides of the core layer as a stress buffer layer between semiconductor chip 5 and wiring 4 to lessen a thermal stress generated between the semiconductor device and the package substrate, where a thickness ratio of core layer 1 to total buffer layer is at least 0.2, the production process can be simplified by using such a buffer layer, thereby improving the mass production capacity and enhancing the package reliability.