CLAIMS

1. A semiconductor package, comprising:

a first redistribution substrate;

a semiconductor chip on a top surface of the first redistribution substrate;

a conductive structure provided on the top surface of the first redistribution substrate and laterally spaced apart from the semiconductor chip; and

a molding layer on the first redistribution substrate, the molding layer covering a sidewall of the semiconductor chip and a sidewall of the conductive structure,

wherein the conductive structure includes:

a first conductive structure having a first sidewall; and

a second conductive structure on a top surface of the first conductive structure, the second conductive structure having a second sidewall,

wherein the first conductive structure has an undercut at a lower portion of the first sidewall, and

wherein the second conductive structure has a protrusion at a lower portion of the second sidewall; and

wherein the semiconductor package further comprises a conductive pattern disposed between the first redistribution substrate and the first conductive structure, wherein a width of the conductive pattern is less than a width of the top surface of the first conductive structure and is equal to a width of a bottom surface of the first conductive structure.

2. The semiconductor package of claim 1,

wherein a first height of the first conductive structure is less than a second height of the second conductive structure.

3. The semiconductor package of claim 1 or claim 2,

wherein a width at a top surface of the second conductive structure is less than a width at the top surface of the first conductive structure.

4. The semiconductor package of claim 3,

wherein a width at a bottom surface of the second conductive structure is greater than the width at the top surface of the second conductive structure, and

wherein the width at the bottom surface of the second conductive structure is less than the width at the top surface of the first conductive structure.

5. The semiconductor package of claim 3 or claim 4,

wherein a difference between the width at the top surface of the first conductive structure and the width at the top surface of the second conductive structure is a value between 20 μm and 30 μm.

6. The semiconductor package of any one of claims 1 to 5,

wherein the molding layer covers the protrusion and fills a region defined by

the undercut.

7. The semiconductor package of any one of claims 1 to 6,

wherein the second conductive structure exposes an edge region at the top surface of the first conductive structure, and

wherein the molding layer covers the edge region at the top surface of the first conductive structure.

8. The semiconductor package of any one of claims 1 to 7,

wherein the second conductive structure contacts the first conductive structure, and

wherein the second conductive structure includes a material that is the same as a material of the first conductive structure and has a grain different from a grain of the first conductive structure.

9. The semiconductor package of any one of claims 1 to 3,

wherein the undercut is recessed from the first sidewall of the first conductive structure along the bottom surface of the first conductive structure, and

wherein the protrusion protrudes from the second sidewall of the second conductive structure and extends from a bottom surface of the second conductive structure along the top surface of the first conductive structure.

10. The semiconductor package of any one of claims 1 to 9, further comprising:

a second redistribution substrate on the molding layer and the second conductive structure,

wherein the second redistribution substrate is coupled to the second conductive structure.

11. A semiconductor package, comprising:

a first redistribution substrate;

a semiconductor chip on a top surface of the first redistribution substrate;

a conductive structure provided on the top surface of the first redistribution substrate and laterally spaced apart from the semiconductor chip; and

a second redistribution substrate provided on the semiconductor chip and the conductive structure and coupled to the conductive structure,

wherein the conductive structure includes:

a first conductive structure having a first sidewall and an undercut at a lower portion of the first sidewall; and

a second conductive structure on the first conductive structure,

wherein a first height of the first conductive structure is less than a second height of the second conductive structure; and

wherein the semiconductor package further comprises a conductive pattern disposed between the first redistribution substrate and the first conductive structure,

wherein a width of the conductive pattern is less than a width of a top surface of the first conductive structure and is equal to a width of a bottom surface of the first conductive structure.

12. The semiconductor package of claim 11,

wherein the second conductive structure has a second sidewall and a protrusion at a lower portion of the second sidewall.

13. The semiconductor package of claim 11 or claim 12,

wherein the first height is between 5% and 45% of a sum of the first height and the second height.

14. The semiconductor package of claim 11 or claim 12,

wherein the first height is between 30 μm and 50 μm, and

wherein a sum of the first height and the second height is between 150 μm and 250 μm.

15. The semiconductor package of any one of claims 11 to 14, further comprising:

a molding layer between the first redistribution substrate and the second redistribution substrate,

wherein the molding layer fills a region defined the undercut and covers the

semiconductor chip and the first sidewall of the first conductive structure.

16. The semiconductor package of any one of claims 11 to 15, further comprising:

an upper semiconductor chip on a top surface of the second redistribution substrate.

17. A semiconductor package, comprising:

a first redistribution substrate that includes a first dielectric layer, a first conductive pattern, and a first redistribution pattern on the first conductive pattern;

a solder ball on a bottom surface of the first redistribution substrate;

a semiconductor chip on a top surface of the first redistribution substrate;

a conductive structure provided on the first redistribution substrate and laterally spaced apart from the semiconductor chip;

a second conductive pattern between the first redistribution substrate and the conductive structure;

a molding layer provided on the first redistribution substrate and covering the semiconductor chip, the molding layer covering a sidewall of the conductive structure and exposing a top surface of the conductive structure; and

a second redistribution substrate provided on the molding layer and electrically connected to the conductive structure,

wherein the second redistribution substrate includes a second dielectric layer,

a third conductive pattern, and a second redistribution pattern on the third conductive pattern,

wherein the first dielectric layer includes a photo-imageable polymer,

wherein the second dielectric layer includes a photo-imageable polymer,

wherein the conductive structure includes a signal conductive structure and a ground/power structure that are electrically separated from each other,

wherein each of the signal conductive structure and the ground/power structure includes:

a first conductive structure that has a first sidewall and an undercut at a lower portion of the first sidewall; and

a second conductive structure on a top surface of the first conductive structure,

wherein the second conductive structure has a second sidewall and a protrusion at a lower portion of the second sidewall, and

wherein a width of the second conductive pattern is less than a width of the top surface of the first conductive structure and is equal to a width of a bottom surface of the first conductive structure.

18. The semiconductor package of claim 17,

wherein the first conductive structure has a first height,

wherein the second conductive structure has a second height, and

wherein the first height is between 5% and 45% of a sum of the first height

and the second height.

19. The semiconductor package of claim 17 or claim 18,

wherein a width at a bottom surface of the second conductive structure is greater than a width at a top surface of the second conductive structure, and

wherein the width at the bottom surface of the second conductive structure is less than the width at the top surface of the first conductive structure.