

Doping of Semiconductor Fin Devices

TECHNICAL FIELD

[0001] The present invention relates to semiconductor devices and more particularly to semiconductor devices with fin structures and methods for doping semiconductor fin devices.

BACKGROUND

[0002] The dominant semiconductor technology used for the manufacture of ultra-large scale integrated (ULSI) circuits is the metal-oxide-semiconductor field effect transistor (MOSFET) technology. Reduction in the size of MOSFETs has provided continued improvement in speed performance, circuit density, and cost per unit function over the past few decades. As the gate length of the conventional bulk MOSFET is reduced, the source and drain increasingly interact with the channel and gain influence on the channel potential. Consequently, a transistor with a short gate length suffers from problems related to the inability of the gate to substantially control the on and off states of the channel.

[0003] Phenomena such as reduced gate control associated with transistors with short channel lengths are termed short-channel effects. Increased body doping concentration, reduced gate oxide thickness, and ultra-shallow source/drain junctions are ways to suppress short-channel effects. However, for device scaling well into the sub-50 nm regime, the requirements for body-doping concentration, gate oxide thickness, and source/drain (S/D) doping profiles become increasingly difficult to meet when conventional device structures based on bulk silicon (Si) substrates are employed. Innovations in front-end process technologies or the introduction of alternative device structures may be needed to sustain the historical pace of device scaling.

[0004] For device scaling well into the sub-30-nm regime, a promising approach to controlling short-channel effects is to use an alternative transistor structure with more than one gate, i.e., multiple-gates. An example of the alternative transistor structure is the multiple-gate transistor. Examples of the multiple-gate transistor include the double-gate transistor, triple-gate transistor, omega field-effect transistor (FET), and the surround-gate or wrap-around gate transistor. A multiple-gate transistor structure is expected to extend the scalability of CMOS technology beyond the limitations of the conventional bulk MOSFET and realize the ultimate limit of silicon MOSFETs. The introduction of additional gates improves the capacitance coupling between the gates and the channel, increases the control of the channel potential by the gate, helps suppress short channel effects, and prolongs the scalability of the MOS transistor.

[0005] The simplest example of a multiple-gate transistor is the double-gate transistor, as described in U.S. Patent No. 6,413,802 ('802) issued to Hu, *et al.* and incorporated herein by reference. In the '802 patent, the transistor channel comprises a thin silicon fin defined using an etchant mask and formed on an insulator layer, e.g., silicon oxide. Gate oxidation is performed, followed by gate deposition and gate patterning to form a double-gate structure overlying the sides of the fin. Both the source-to-drain direction and the gate-to-gate direction are in the plane of the substrate surface.

SUMMARY OF THE INVENTION

[0006] The preferred embodiment of the present invention provides several methods for doping the semiconductor fin in a multiple-gate transistor to provide improved performance. In embodiments of the invention, the channel length is more uniformly doped than in certain prior art implementation thereby improving performance.

[0007] A first embodiment provides a method of doping semiconductor fins of multiple-gate transistors. A semiconductor structure includes of a plurality of semiconductor fins overlying an insulator layer, a gate dielectric overlying a portion of said semiconductor fin, and a gate electrode overlying the gate dielectric. Each of the semiconductor fins has a top surface, a first sidewall surface, and a second sidewall surface. Dopant ions are implanted at a first angle (greater than 7°) with respect to the normal of the top surface of the semiconductor fin to dope the first sidewall surface and the top surface. Further dopant ions are implanted with respect to the normal of the top surface of the semiconductor fin to dope the second sidewall surface and the top surface.

[0008] A second embodiment provides a method to dope semiconductor fins with a different orientation. In this embodiment, a first mask covers the second semiconductor fin while the first semiconductor fin is doped by implanting dopant ions with a large implant angle. Similarly, a second mask covers the first semiconductor fin while the second semiconductor fin is doped by implanting the dopant ions with a large implant angle.

[0009] The present invention also includes structure embodiments. For example, semiconductor-on-insulator chip includes a plurality of multiple-gate transistors formed on an insulator layer. Each multiple-gate transistor includes a semiconductor fin having an orientation

and a gate electrode having a gate length of less than 30 nm. The orientation of each transistor of the plurality of multiple-gate transistors is the same. Other methods and structures are also taught.

[0010] A semiconductor-on-insulator chip comprising of a plurality of multiple-gate transistors formed on an insulator layer, each multiple-gate transistor comprising of a semiconductor fin having an orientation and a gate electrode having a gate length equal to the minimum feature size, said orientations of the plurality of multiple-gate transistors being the same.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0011] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:
- [0012] Figure 1a illustrates a double gate device structure;
- [0013] Figure 1b illustrates a triple-gate device structure;
- [0014] Figure 1c illustrates an omega field-effect transistor;
- [0015] Figure 2 is a plan view of a multiple gate transistor;
- [0016] Figure 3a illustrates a three-dimensional perspective of a triple-gate transistor;
- [0017] Figure 3b illustrates a three-dimensional perspective of the omega FET;
- [0018] Figure 4a is a cross-sectional view taken along B-B' of Figure 2;
- [0019] Figure 4b is a cross-sectional view taken along C-C' of Figure 2;
- [0020] Figures 5a, 5b and 5c are cross-sectional views showing doping of a semiconductor fin using a large angle implant;
- [0021] Figure 6a illustrates the doses received in the top and sidewall surface regions of the semiconductor fin as a function of the implant angle;
- [0022] Figure 6b illustrates the ratio of the dose in the top region to the dose in a sidewall surface region as a function of the implant angle;
- [0023] Figure 7a is a plan view of the semiconductor fin device of the present invention;

[0024] Figure 7b is a cross-sectional view of the semiconductor fin device of the present invention;

[0025] Figure 8a illustrates the second transistor masked during the doping of the source and drain regions of the first transistor;

[0026] Figure 8b illustrates the first transistor masked during the doping of the source and drain regions of the second transistor; and

[0027] Figure 9 illustrates an n-type transistor of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0028] The preferred embodiment of the present invention relates to the field of semiconductor devices and more particularly to semiconductor devices with a fin structure. The present invention provides several methods for doping the semiconductor fin in a multiple-gate transistor.

[0029] Another example of the multiple-gate transistor is the triple-gate transistor 102. The cross-section of the triple-gate transistor structure 102 is illustrated in Figure 1b. The plan view of the triple-gate structure is the same as the double-gate structure and is shown in Figure 2. The triple-gate transistor structure has a gate electrode 110 that forms three gates: one gate on the top surface 124 of the silicon body/fin 112, and two gates on the sidewalls 114 of the silicon body/fin 112. The triple-gate transistor achieves better gate control than the double-gate transistor because it has one more gate on the top of the silicon fin. A three-dimensional view of the triple-gate transistor 102 is shown in Figure 3a. Figure 3a illustrates source region 126 and drain region 128, which are formed in silicon body 112 on opposite sides of the channel region. An example of a triple-gate transistor is provided by R. Chau, *et al.*, "Advanced depleted-substrate transistors: single-gate, double-gate, and tri-gate," 2002 International Conference on Solid State Devices and Materials, Nagoya, Japan, pp. 68-69, Sep. 2002, which is incorporated herein by reference.

[0030] The triple-gate transistor structure may be modified for improved gate control, as illustrated in Figure 1c. Such a structure 104 is also known as the Omega (Ω) field-effect transistor (FET), or simply omega-FET, since the gate electrode 110 has an omega-shape in its cross-sectional view. The encroachment of the gate electrode 110 under the semiconductor fin

or body 112 forms an omega-shaped gate structure. It closely resembles the Gate-All-Around (GAA) transistor for excellent scalability, and uses a very manufacturable process similar to that of the double-gate or triple-gate transistor. The omega-FET has a top gate adjacent surface 124, two sidewall gates adjacent surfaces 114, and special gate extensions or encroachments 130 under the fin-like semiconductor body.

[0031] The omega-FET is therefore a field effect transistor with a gate 110 that almost wraps around the body 112. In fact, the longer the gate extension 130, i.e., the greater the extent of the encroachment E, the more the structure approaches or resembles the gate-all-around structure. A three-dimensional perspective of the triple-gate transistor with recessed insulator, or omega-FET, is schematically illustrated in Figure 3b. The encroachment of the gate electrode 110 under the silicon body 112 helps to shield the channel from electric field lines from the drain 128 and improves gate-to-channel controllability, thus alleviating the drain-induced barrier lowering effect and improving short-channel performance. An example of an omega field-effect transistor is provided by F.L. Yang, *et al.*, "25 nm CMOS Omega-FET's," International Electron Device Meeting, Dig., Technical Papers, December 2002, which is incorporated herein by reference.

[0032] Another multiple-gate device that can utilize aspects of the present invention is the surround-gate or wrap-around gate transistor mentioned above. Examples of these devices are taught in the following references, each of which is incorporated herein by reference: J.P. Colinge, *et al.*, "silicon-on-insulator gate-all-around device," International Electron Device Meeting, Dig. Technical Papers, pp. 595-598, December 1990; U.S. Patent No. 6,391,782, B. Yu, Advanced Micro Devices, Inc., May 21, 2002, "Process for forming multiple active lines and gate-all-around MOSFET; E. Leobandung, *et al.*, "Wire-Channel and wrap-around-gate metal-

oxide-semiconductor field-effect transistors with a significant reduction of short channel effects," J. Vacuum Science and Technology B, vol. 15, no. 6, pp. 2791-2794, 1997; and U.S. Patent No. 6,451,656, B. Yu, *et al.*, Advanced Micro Devices, Inc., Sep. 17, 2002, "CMOS inveter configured from double gate MOSFET and method of fabricating same."

[0033] The multiple-gate transistor structures described, i.e., the double-gate transistor 100, the triple-gate transistor 102, and the omega-FET 104, have a common feature: the fin-like semiconductor active region 112. In doping the source and drain regions 126 and 128 of the semiconductor fin, prior art uses a conventional source and drain ion implantation process where ions are implanted at a small angle with respect to the normal of the wafer or the substrate. In conventional source and drain implantation, a small angle of 7 degrees or less is frequently used, as shown in Figure 4a, which is taken along the B-B' line of Figure 2.

[0034] Using such an ion implantation condition results in most of the implanted dopants reaching the top surface 124 of the fin 112, giving a high-doped top surface region 132. Few dopants are effectively implanted into the sidewall surface 114, resulting in a lightly doped sidewall surface region 134. A long implantation time may be needed to introduce a significant amount of doping in the sidewall source/drain regions 126/128. In addition, since less dopants reach the bottom portion of the fin, the source and drain doping at the bottom portion of the fin will be lower, and may result in a larger channel length at the bottom portion of the fin than at the top portion of the fin.

[0035] Figure 4b shows a cross-section of Figure 2 taken along the C-C' line. A variation of the channel length of channel 136 within the fin 112, i.e., a larger channel length at the bottom portion of the fin, results in a non-uniform source-to-drain current distribution with reduced

current at the bottom portion of the fin. Therefore, the performance of the semiconductor fin device is not optimized when the conventional source and drain doping process is used.

[0036] Embodiments of the present invention can be implemented using any of a number of multiple gate transistors. Three examples of these transistors are described with respect to Figures 1-4. Any of these structures, as well as other structures, can utilize concepts of the present invention. As illustrated in a cross-sectional view in Figure 1a, a double-gate transistor 100 has a gate electrode 110 that straddles across the channel or the fin-like silicon body 112, thus forming a double-gate structure. There are two gates, one on each sidewall 114 of the silicon fin 112, as shown in Figure 1a. The plan view of the double-gate structure is shown in Figure 2, where Figure 1a (and 1b and 1c) are taken along the A-A' line of Figure 2. The silicon fin 112 is formed on an insulator 116 which is formed on silicon substrate 118. The silicon body 112 is separated from the gate electrode 110 by a gate dielectric 120 along the sidewalls 114 and by a mask 122 along a top surface of the fin 114.

[0037] Examples of double-gate transistors are provided in the following references, each of which is incorporated herein by reference. As will become clear from the teachings below, the structures disclosed in these references can be modified and/or utilize the methods of the present invention.

- X. Huang, *et al.*, "Sub-50 nm p-channel finFET," IEEE Trans. Electron Devices, vol. 48, no. 5, pp. 880-886, May 2001.

- C. Hu *et al.*, U.S. Patent No. 6,413,802, "FinFET transistor structures having a double gate channel extending vertically from a substrate and methods of manufacture," July 2, 2002.

- F.L. Yang, *et al.*, "35 nm CMOS FinFETs," Symposium on VLSI Technology,

Digest of Technical Papers, pp. 109-110, June 2002.

- H.S.P. Wong, "Beyond the conventional transistor," IBM J. Research and Development, vol. 46, no. 2/3, pp. 133-168, March/May 2002.
- F.L. Yang et al., U.S. Patent No. 6,252,284, "Planarized Si fin device," June 26, 2001.
- B. Yu, U.S. Patent No. 6,391,695, "Double-gate transistor formed in a thermal process," May 21, 2002.

[0038] Multiple-gate transistors such as the double-gate transistor, the triple-gate transistor, the omega-FET, have a common feature: the semiconductor fin-like active region. Therefore, such devices are also known as semiconductor fin devices. The semiconductor fin has a predetermined fin height h and a predetermined fin width w . Another common feature of multiple-gate transistors is that the sidewall surfaces of the semiconductor fins are used for current conduction, i.e., a significant amount of source-to-drain current in the multiple-gate transistor is carried along the sidewall surfaces.

[0039] Essentially, the effective device width of the multiple-gate transistor is a function of the fin height h (see Figure 1a). In the double-gate transistor, the device width is twice the fin height, i.e., $2h$. In the triple-gate transistor, the device width is given by $(2h + w)$ (see Figure 1a and 1b). As shown in Figures 3a and 3b, portions of the sidewalls of the semiconductor fin 112 are doped for forming the source region 126 and the drain region 128. Therefore, in the fabrication of semiconductor fin devices or multiple-gate transistors, processes involving the doping of the semiconductor fin, and particularly the sidewall surfaces of the semiconductor fin, are used. Effective and efficient doping of the sidewall surfaces of the semiconductor fin can be

used to optimize the transistor characteristics. In one aspect, this invention provides improved methods of doping the semiconductor fin sidewalls in a manufacturing process.

[0040] According to this aspect of the invention, the implant angle α for the source and drain doping of the semiconductor fin device is large to optimize the device performance.

Referring now to Figures 5a – 5c, an ion implantation scheme is shown where the ion implantation is performed in at least two implant steps. As shown in Figure 5a, a semiconductor fin 112 is provided on an insulator layer 116. The insulator layer 116 may have a recess as in the case of an omega-FET as shown in Figure 1c. The thickness of the insulator layer may range from about 100 angstroms to about 2000 angstroms. For illustration purposes, we consider the semiconductor fin 112 for a triple-gate transistor 102.

[0041] In the preferred embodiment, the semiconductor fin 112 is formed from silicon, and the implanted ions are p-type dopant ions such as boron and/or indium or n-type dopant ions such as phosphorus, arsenic, and/or antimony. In the first implant step, as shown in Figure 5b, an angled implant (denoted by arrows 140) with an angle α with respect to the normal of the wafer top surface 124 in the z - x plane is performed. The implanted dose is about half the total dose I (in units of dopants per unit wafer surface area) of dopants for the source 126 and drain 128 ion implantation. The total dose I for the source and drain ion implant is typically in the range of about 1×10^{13} to about 1×10^{16} dopants per square centimeter. The first implantation step 140 creates doped top region 144 and doped sidewall region 146.

[0042] At the point of incidence at the top fin surface 124, the ions approach the top surface 124 at an angle α with respect to the normal of the top fin surface. The normal of the top fin surface is typically parallel to the normal of the wafer. At the point of incidence to the fin sidewall surface 114, the ions approach the sidewall surface 114 at an angle of $(90 - \alpha)$ degrees

with respect to the normal of the fin sidewall surface. The angles of α and $(90 - \alpha)$ are measured in the plane perpendicular to the plane of the sidewall surface 114.

[0043] In the first implant step, the fin's first sidewall surface 114 received a dose of about $(I/2) \cdot \sin(\alpha)$, the fin's top surface 124 received a dose of about $(I/2) \cdot \cos(\alpha)$, and the fin's second sidewall surface 115 received essentially no dopants.

[0044] In the second implant step, the device 102 is rotated 180 degrees about its normal and the second half dose is implanted at an angle α with respect to the normal of the wafer in the z - x plane, as shown in Figure 5c. In the second implant step (denoted by arrows 142), the fin's second sidewall surface 115 received a dose of about $(I/2) \cdot \sin(\alpha)$, the fin's top surface 124 received another dose of about $(I/2) \cdot \cos(\alpha)$, and fin's first sidewall surface 114 received essentially no dopants. As a result, after the first and the second implant steps, the total dose received by the top surface of the fin is $I \cdot \cos(\alpha)$, and the total dose received by each sidewall surface is $(I/2) \cdot \sin(\alpha)$. Figure 5c illustrates the formation of doped sidewall region 148.

[0045] In the embodiment illustrated in Figures 5b and 5c, both ion implantation steps 140 and 142 were performed at an angle α . It is noted that the angle of the first implantation step need not be equal to the angle of the second implantation step. It is desirable, (but not necessary) that these angles be close in value so as to maintain consistent operating characteristics in sidewall doped regions 146 and 148.

[0046] In Figure 6a, the dose of dopants per unit surface area received in a top surface region 144 and in a sidewall surface region 146 (or 148) of the fin 112 are plotted as a function of the implant angle α . If the angle α is zero, $(I/2) \cdot \sin(\alpha)$ becomes zero, i.e., no dopants will reach the fin sidewall surface, while $I \cdot \cos(\alpha)$ becomes I , i.e., the top surface of the fin will be doped with a dose I . Consequently, if a zero implant angle is used, the source and drain regions

126 and 128 on the fin sidewalls 114 and 115 of the multiple-gate transistor cannot be effectively formed. It is seen that in conventional source and drain ion implant conditions using small angles such as 7 degrees, the dose per unit surface area received by each sidewall surface is less than a tenth of the dose per unit surface area received by the top surface. In this case, a very high implant dose and long implantation time are required for the fin sidewall surface to receive a substantial amount of doping.

[0047] The preferred embodiment of this invention teaches that the implant angle should be large for the sidewall surfaces 114 and 115 to receive a substantial amount of doping. In fact, the implant angle is as large as 60 degrees for the top and sidewall surfaces of the fin 112 to have comparable doses, resulting in comparable doping concentrations.

[0048] Referring now to Figure 6b, the ratio of the dose received on the top fin surface 124 to the dose received on a fin sidewall surface 114 (or 115) is plotted as a function of the implant angle α . This ratio can also be interpreted as the ratio of the doping concentration in the top fin surface region 144 to the doping concentration in a fin sidewall surface region 146 (or 148). In one embodiment of the present invention, the ratio is preferably less than about 8, and the corresponding implant angle therefore is more than about 15 degrees. In the preferred embodiment, the ratio is in the range of about 1 to about 4, and the corresponding implant angle has to be in the range of about 26 degrees to about 63 degrees. The doping concentrations in the top surface region 144 and the sidewall surface regions 146 and 148 are preferably more than about 1×10^{20} dopants per cubic centimeter.

[0049] According to the teaching of this invention, a large implant angle α has a number of advantages. First, a large angle implant can introduce more dopants more efficiently in the source and drain regions 126 and 128 on the sidewall surfaces of the transistor. As a result, the

use of a small angle implant with long implantation time can be avoided. Second, a large angle implant will dope the top surfaces 124 and the sidewall surfaces 114 and 115 of the source and drain regions in the fin more equally. As a result, the channel length of the multiple-gate transistor is maintained the same whether at the top portion of the fin or at the bottom portion of the fin.

[0050] However, potential problems arise in the use of large angle implants, and solutions to these problems will be provided according to aspects of the present invention. Referring now to Figure 7a, a plan view of two multiple-gate transistors 102a and 102b are shown, where the two transistors 102a and 102b have source-to-drain directions that are perpendicular to each other, i.e., the semiconductor fins 112 are oriented in directions that are perpendicular to each other. In other words, the orientations of the semiconductor fins are orthogonal to each other. In Figure 7a, the source-to-drain direction of the first transistor 102a is in the y-direction, and the source-to-drain direction of the second transistor 102b is in the x-direction. The x-y axes are shown in the bottom right corner of Figure 7a.

[0051] The orientations of the gate electrodes 110a and 110b of the two transistors are also perpendicular to each other. It is understood that the two transistors may be in close proximity to each other, as illustrated in Figure 7a, or may be far apart from each other, such as being located at extreme ends of an integrated circuit die. The multiple-gate transistors shown in Figure 7a may be double-gate transistors, triple-gate transistors, or omega-FETs. For illustration purposes, the multiple-gate transistors are triple-gate transistors.

[0052] Figure 7b shows the cross-sectional view of the triple-gate transistors 102a and 102b along line A-A' of Figure 7a. Line A-A' of Figure 7a cuts through the source region 126a of the first transistor 102a and the source region 126b, channel region 136b, and drain region 128b of

the second transistor 102b. In general, in the fabrication process of multiple-gate transistors, semiconductor fins 112 are provided on an insulator layer 116, a gate dielectric layer 120 is deposited, followed by the formation of gate electrodes 110.

[0053] The gate dielectric layer may be comprised of silicon oxide or silicon oxynitride. The gate dielectric layer may also comprise high permittivity dielectrics such as lanthalam oxide (La_2O_3), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), hafnium oxynitride (HfON), zirconium oxide (ZrO_2), or combinations thereof. High permittivity dielectrics typically have a relative permittivity of greater than 5. The gate electrode may be comprised of a conductive material. Examples of conductive materials are doped poly-crystalline silicon, doped poly-crystalline silicon-germanium, a metal, or a metal silicide. At this point, before the formation of the source and drain regions 126 and 128, the channel region 136 in the semiconductor fin 112 may be undoped or doped.

[0054] The subsequent fabrication process step may involve the formation of the source region 126 and drain region 128 by doping appropriate portions of the semiconductor fin 112. If a large angle implant with an angle α in the z-x plane is used to dope the first sidewall 114a of the semiconductor fin of the first transistor 102a, the channel region 136b of the second transistor 102b will also receive the source and drain dopants, causing degradation to the performance of the second transistor 102b. The same problem occurs when using a large angle implant to dope the second sidewall 115a of the first transistor 112a.

[0055] In general, the large angle implant steps, while providing efficient doping of the source and drain regions of transistors with a first source-to-drain orientation, e.g., source-to-drain direction in y-direction, will also dope the channel region of the transistors with a second perpendicular source-to-drain orientation, e.g., source-to-drain direction in x-direction, with the

same source/drain dopants. This is because a source and drain implant 140 with a large implant angle α such as 30 degrees has an implant angle similar to that of a halo implant and can therefore dope the channel region 136b of the second transistor. Standard conventional halo implants, however, dope the channel region 136 with dopants of the opposite type to the source 126 and drain 128 dopants in order to control short channel effects. When the channel region 136b of the second transistor 102b is doped with the dopants intended for the source and drain regions 126a and 128a, the second transistor 102b will have degraded short-channel behavior and may even fail due to an electrical short between the source and drain 126b and 128b.

[0056] According to aspects of this invention, a method is provided in which a large angle implant may be used to dope the source and drain regions 126a and 128a of the first transistor 102a with a first source-to-drain orientation without doping the channel region 136b of the second transistor 102b with a second perpendicular source-to-drain orientation. Prior to the source and drain implant, a mask material 150 is deposited on the wafer to cover both the first and second transistors 102a and 102b. The mask material is patterned, e.g., by optical lithography, and the portion of the mask material 150 that covers the first transistor 102a is removed to form a first mask 150, as shown in Figure 8a. The first mask 150 covers the second transistor 102b, shielding the channel region 136b, during the doping of the source and drain regions 126a and 128a of the first transistor 102a.

[0057] The doping of the source and drain regions 126a and 128a may be performed in two implant steps, as described above, in which a half-dose angled implant is performed to dope the first sidewall 114a and top surface 124a of the fin 112a of the first transistor 102a followed by another half-dose angled implant to dope the second sidewall 115a and top surfaces 124a.

Following the doping of the source and drain regions 126a and 128a, the first mask 150 may be removed.

[0058] Next, a second mask 152 is formed to expose the second transistor 102b while covering the first transistor 102a. An ion implantation including at least two steps is performed to dope the source and drain regions 126a and 128a of the second transistor 102b. The channel region 136a of the first transistor 102a is shielded from this ion implantation process by the second mask 152. The implant angle of the ion implantation process to dope the source and drain regions 126b and 128b of the second transistor 102b is oriented at an angle β in the z-y plane. The angle β is in the z-y plane which is perpendicular to the plane of the sidewall 114b of the semiconductor fin 112b of the second transistor. In Figure 8b, the positive y-axis is into the plane of the paper while the negative y-axis is out of the plane of the paper (and, as a result, the angle β cannot be explicitly drawn).

[0059] The second mask 152 may then be removed. A high temperature annealing step may be performed to activate the implanted dopants in the semiconductor fins 112a and 112b. The annealing step may be a spike anneal process in which the wafer temperature is rapidly increased to a peak temperature of 1050 degrees Celsius followed by a rapid cooling of the wafer temperature, or any other annealing techniques such as a rapid thermal anneal (RTA) commonly known and used in the art.

[0060] In the above-mentioned method embodiment, it is seen that the doping of source and drain regions 126 and 128 in transistors of the same type, e.g., n-type or n-channel, involves an additional mask patterning step. The introduction of an additional mask is sometimes costly and could be commercially prohibitive. Therefore, a further improvement over the above-mentioned embodiment is to align all multiple-gate transistors of the same type with a predetermined range

of gate lengths in the same direction to permit the use of a large angle implant without the introduction of an additional mask. This is described in another embodiment of the present invention.

[0061] According to this embodiment, all multiple-gate transistors of the same conductivity type and with gate lengths less than or equal to a predetermined gate length are oriented in the same direction. In this context, all of transistors refers to all of the functional or operational transistors that are designed to operate with optimum characteristics. For example, this does not include dummy transistors or other transistors that do not operate in the circuits of the chip. The predetermined gate length is determined based on susceptibility to short-channel effects. Transistors with shorter gate lengths are more susceptible to short-channel effects. The predetermined gate length may be 30 nm, for example. In another example, the predetermined gate length may be the minimum gate length.

[0062] Since the large angle implant for doping the source and drain regions 126 and 128 of transistors of a first source-to-drain orientation degrade short-channel effects of transistors with other source-to-drain orientations, transistors susceptible to degradation of short-channel effects should all have the same source-to-drain direction. This means, for example, that all n-type multiple-gate transistors with gate lengths less than 30 nm have the source-to-drain direction oriented in the x -direction. This is illustrated in Figure 9 where gate lengths $L_{g,a}$ and $L_{g,b}$ are less than the predetermined gate length, e.g., 30 nm, while $L_{g,c}$ and $L_{g,d}$ are larger than the predetermined gate length. Transistor 102a and transistor 102b of Figure 9, having gate lengths of $L_{g,a}$ and $L_{g,b}$ respectively, therefore have substantially the same source-to-drain orientations (i.e., the source-to-drain current paths are substantially parallel). Transistor 102c and transistor

102d have gate lengths of $L_{g,c}$ and $L_{g,d}$, respectively, and they may have any source-to-drain orientations.

[0063] It is understood, however, that transistor 102c and transistor 102d may have different electrical characteristics or vulnerability to short-channel effects depending on the ion implantation conditions used to dope their source and drain regions 126 and 128. The x -direction can be, for example, a crystallographic direction such as the [100] direction. In this case, the sidewall surfaces of the n-channel multiple-gate transistor are (100) surfaces. N-channel multiple-gate transistors with (100) sidewall surfaces are expected to have the best electron mobility. In another example, all p-type multiple-gate transistors with gate lengths less than 30 nm may have the source-to-drain direction oriented in the [110] crystallographic direction. In this case, the sidewall surfaces of the p-channel multiple-gate transistor are (110) surfaces. P-channel multiple-gate transistors with (110) sidewall surfaces is expected to have the best hole mobility.

[0064] In another method embodiment, the semiconductor fins 112 may be doped by solid-source diffusion instead of ion implantation as described in the other method embodiments. In the solid-source diffusion technique, a dopant-containing material (the solid source) is deposited on the semiconductor fin to be doped. An elevated temperature treatment is then performed to allow the dopants in the dopant-containing material or solid-source to diffuse into the semiconductor fins. Examples of dopant-containing materials include boro-silicate glass (BSG), phospho-silicate glass (PSG), doped germanium, etc. The discussion related to Figure 9 also applies to this embodiment.

[0065] While several embodiments of the invention, together with modifications thereof, have been described in detail herein and illustrated in the accompanying drawings, it will be

evident that various modifications are possible without departing from the scope of the present invention. The examples given are intended to be illustrative rather than exclusive. The drawings may not necessarily be to scale and features may be shown in a schematic form.

WHAT IS CLAIMED IS:

- 1 1. A method of doping semiconductor fins of multiple-gate transistors, the method
2 comprising:
3 providing a semiconductor structure comprising of a plurality of semiconductor fins
4 overlying an insulator layer, a gate dielectric overlying a portion of said semiconductor fin, and a
5 gate electrode overlying said gate dielectric, each of the semiconductor fins having a top surface,
6 a first sidewall surface, and a second sidewall surface;
7 implanting dopant ions at an angle α with respect to the normal of the top surface of the
8 semiconductor fin to dope the first sidewall surface and the top surface, the angle α being larger
9 than about 7 degrees; and
10 implanting dopant ions at an angle β with respect to the normal of the top surface of the
11 semiconductor fin to dope the second sidewall surface and the top surface, the angle β being
12 larger than about 7 degrees.
- 1 2. The method of claim 1 wherein the angle α has a magnitude that is about equal to the
2 magnitude of angle β .
- 1 3. The method of claim 1 further comprising an annealing process to activate the implanted
2 dopant ions.
- 1 4. The method of claim 1 wherein the semiconductor fins are oriented in the same direction.
- 1 5. The method of claim 1 wherein the gate electrodes have gate lengths smaller than 30 nm
2 and the semiconductor fins are oriented in the same direction.

- 1 6. The method of claim 1 wherein the semiconductor fins comprise silicon fins.
- 1 7. The method of claim 6 wherein the dopant ions are p-type dopant ions selected from the
2 group consisting of boron and indium and combinations thereof.
- 1 8. The method of claim 7 wherein the first and second sidewall surfaces are (110)
2 crystallographic surfaces.
- 1 9. The method of claim 6 wherein the dopant ions are n-type dopant ions selected from the
2 group consisting of phosphorus, arsenic, and antimony and combinations thereof.
- 1 10. The method of claim 9 wherein the first and second sidewall surfaces are (100)
2 crystallographic surfaces.
- 1 11. The method of claim 1 wherein the semiconductor structure further comprises an etchant
2 mask overlying the semiconductor fin.
- 1 12. The method of claim 1 wherein the insulator layer is recessed, resulting in a notch at the
2 base of the semiconductor fin.
- 1 13. The method of claim 1 wherein the ratio of the doping concentration in a top surface
2 region of the semiconductor fin to the doping concentration in the first sidewall region of the
3 semiconductor fin is between about 1 and about 4.
- 1 14. The method of claim 1 wherein the angle α is greater than about 15 degrees.

- 1 15. The method of claim 1 wherein the angle α is between about 26 degrees and about 63
2 degrees.
- 1 16. The method of claim 1 wherein the first and second sidewall regions are doped to a
2 doping concentration of more than $1 \times 10^{20} \text{ cm}^{-3}$.
- 1 17. The method of claim 1 wherein the insulator layer comprises silicon oxide.
- 1 18. The method of claim 1 wherein the insulator layer has a thickness of between about 100
2 angstroms and about 2000 angstroms.
- 1 19. The method of claim 1 wherein the gate dielectric layer comprises silicon oxide.
- 1 20. The method of claim 1 wherein the gate dielectric layer comprises silicon oxynitride.
- 1 21. The method of claim 1 wherein the gate dielectric layer comprises high permittivity
2 material.
- 1 22. The method of claim 21 wherein the high permittivity material is selected from the group
2 consisting of lanthalam oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, zirconium
3 oxide, and combinations thereof.
- 1 23. The method of claim 21 wherein the gate dielectric layer comprises of high permittivity
2 materials with relative permittivity greater than 5.
- 1 24. The method of claim 1 wherein the gate dielectric has a thickness of between about 3 and
2 about 100 angstroms.

- 1 25. The method of claim 1 wherein the gate electrode comprises poly-crystalline silicon.
- 1 26. The method of claim 1 wherein the gate electrode comprises a metal.

1 27. A method of doping semiconductor fins of multiple-gate transistors, the method
2 comprising:

3 providing a first semiconductor fin with a first orientation and a second semiconductor
4 fin with a second orientation overlying an insulator layer, each of the first and second
5 semiconductor fins having a top surface and two sidewall surfaces;

6 masking the second semiconductor fin;

7 doping the first semiconductor fin by implanting dopant ions with a large implant
8 angle α ;

9 masking the first semiconductor fin;

10 doping the second semiconductor fin by implanting the dopant ions with a large implant
11 angle β .

1 28. The method of claim 27 wherein the first orientation and second orientation are
2 perpendicular to each other.

1 29. The method of claim 27 wherein the angle α is in a plane perpendicular to the plane of
2 the sidewall surfaces of the first semiconductor fin and the angle β is in a plane perpendicular to
3 the plane of the sidewall surfaces of the second semiconductor fin.

1 30. The method of claim 27 further comprising annealing the semiconductor fins to activate
2 the implanted dopant ions.

1 31. The method of claim 27 wherein the dopant ions are p-type dopant ions selected from the
2 group consisting of boron, indium and combinations thereof.

- 1 32. The method of claim 31 wherein the sidewall surfaces are (110) crystallographic
2 surfaces.
- 1 33. The method of claim 26 wherein the ions are n-type dopant ions selected from the group
2 consisting of phosphorus, arsenic, antimony and combinations thereof.
- 1 34. The method of claim 33 wherein the sidewall surfaces are (100) crystallographic
2 surfaces.
- 1 35. The method of claim 27 wherein each semiconductor fin further comprises an etchant
2 mask overlying that semiconductor fin.
- 1 36. The method of claim 27 wherein the insulator layer is recessed, resulting in a notch at the
2 base of each semiconductor fin.
- 1 37. The method of claim 27 wherein the ratio of the doping concentration in the top surface
2 region of the semiconductor fin to the doping concentration in the sidewall region of the
3 semiconductor fin is between about 1 and about 4.
- 1 38. The method of claim 27 wherein the angle α and the angle β are each greater than about
2 15 degrees.
- 1 39. The method of claim 27 wherein the angle α and the angle β are each between about 26
2 degrees and about 63 degrees.

- 1 40. The method of claim 27 wherein the first and second sidewall regions are doped to a
2 doping concentration of more than about $1 \times 10^{20} \text{ cm}^{-3}$.
- 1 41. The method of claim 27 wherein the insulator layer comprises silicon oxide.
- 1 42. The method of claim 27 wherein the insulator layer has a thickness of between about 100
2 angstroms and about 2000 angstroms.
- 1 43. The method of claim 27 wherein the gate dielectric layer comprises silicon oxide.
- 1 44. The method of claim 27 wherein the gate dielectric layer comprises silicon oxynitride.
- 1 45. The method of claim 27 wherein the gate dielectric layer comprises of high permittivity
2 materials.
- 1 46. The method of claim 45 wherein the gate dielectric layer is selected from the group
2 consisting of lanthalam oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, zirconium
3 oxide, and combinations thereof.
- 1 47. The method of claim 45 wherein the gate dielectric layer comprises of high permittivity
2 materials with relative permittivity greater than 5.
- 1 48. The method of claim 27 wherein the gate dielectric has a thickness of between about 3
2 and about 100 angstroms.
- 1 49. The method of claim 27 wherein the gate electrode comprises poly-crystalline silicon.

- 1 50. The method of claim 27 wherein the gate electrode comprises a metal.

1 51. A semiconductor-on-insulator chip comprising:
2 a plurality of multiple-gate transistors formed on an insulator layer;
3 at least some of the multiple-gate transistors comprising:
4 a semiconductor fin having an orientation in a first direction;
5 a gate electrode formed adjacent a channel region portion of the semiconductor
6 fin, the gate electrode having a gate length of less than about 30 nm;
7 a source region and a drain region disposed within the semiconductor fin such that
8 the channel region is disposed between the source region and the drain region, wherein the
9 channel region is doped to a first conductivity type and the source and drain regions are doped to
10 a second conductivity type that is different than the first conductivity type;
11 wherein the at least some of the multiple gate transistors include substantially all of the
12 multiple-gate transistors on the semiconductor-on-insulator chip that have a gate length less than
13 about 30 nm and a channel region of the first conductivity type.

1 52. The chip of claim 51 wherein the semiconductor fin is comprised of silicon.

1 53. The chip of claim 52 wherein the multiple-gate transistors are p-type transistors.

1 54. The chip of claim 53 wherein the orientation of the semiconductor fin is in the [110]
2 direction.

1 55. The chip of claim 54, the fin having sidewall surfaces that are (110) crystallographic
2 surfaces.

1 56. The chip of claim 52 wherein the multiple-gate transistors are n-type transistors.

- 1 57. The method of claim 56 wherein the orientation of the semiconductor fin is in the [100].
- 1 58. The chip of claim 57, the fin having sidewall surfaces that are (100) crystallographic
2 surfaces.
- 1 59. The chip of claim 52 wherein each semiconductor fin further comprises an etchant mask
2 overlying the semiconductor fin.
- 1 60. The chip of claim 52 wherein the insulator layer is recessed, resulting in a notch at the
2 base of each semiconductor fin.
- 1 61. The chip of claim 52 wherein the ratio of the doping concentration in a top surface region
2 of the semiconductor fin to the doping concentration in a sidewall region of the semiconductor
3 fin is between about 1 and about 4.
- 1 62. The chip of claim 52 wherein first and second sidewall regions are doped to a doping
2 concentration greater than about $1 \times 10^{20} \text{ cm}^{-3}$.
- 1 63. The chip of claim 52 wherein the insulator layer comprises silicon oxide.
- 1 64. The chip of claim 52 wherein the insulator layer has a thickness of between about 100
2 angstroms and about 2000 angstroms.
- 1 65. The chip of claim 52, further comprising of a gate dielectric layer overlying a portion of
2 the semiconductor fin and underlying the gate electrode.
- 1 66. The chip of claim 65 wherein the gate dielectric layer comprises silicon oxide.

- 1 67. The chip of claim 65 wherein the gate dielectric layer comprises silicon oxynitride.
- 1 68. The chip of claim 65 wherein the gate dielectric layer comprises a high permittivity
2 material.
- 1 69. The method of claim 68 wherein the gate dielectric layer is selected from the group
2 consisting of lanthalam oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, zirconium
3 oxide, and combinations thereof.
- 1 70. The chip of claim 68 wherein the gate dielectric layer comprises of high permittivity
2 materials with relative permittivity greater than 5.
- 1 71. The chip of claim 51 wherein the gate dielectric has a thickness of between about 3 and
2 about 100 angstroms.
- 1 72. The chip of claim 51 wherein the gate electrode comprises poly-crystalline silicon.
- 1 73. The chip of claim 51 wherein the gate electrode comprises a metal

- 1 74. A semiconductor-on-insulator chip comprising:
2 a plurality of multiple-gate transistors formed on an insulator layer, each multiple-gate
3 transistor including a semiconductor fin having an orientation and a gate electrode having a gate
4 length equal to the minimum feature size; and
5 wherein said orientation each of the plurality of multiple-gate transistors is the same, the
6 plurality of multiple-gate transistors comprising substantially all functional multiple-gate
7 transistors on the semiconductor-on-insulator chip.
- 1 75. The chip of claim 74 wherein the semiconductor fin is comprised of silicon.
- 1 76. The chip of claim 75 wherein the multiple-gate transistors are p-type transistors.
- 1 77. The chip of claim 76 wherein the orientation of the semiconductor fin is in the [110]
2 direction.
- 1 78. The chip of claim 77, the fin having sidewall surfaces that are (110) crystallographic
2 surfaces.
- 1 79. The chip of claim 75 wherein the multiple-gate transistors are n-type transistors.
- 1 80. The method of claim 79 wherein the orientation of the semiconductor fin is in the [100].
- 1 81. The chip of claim 80, the fin having sidewall surfaces that are (100) crystallographic
2 surfaces.

1 82. The chip of claim 75 wherein each semiconductor fin further comprises an etchant mask
2 overlying the semiconductor fin.

1 83. The chip of claim 75 wherein the insulator layer is recessed, resulting in a notch at the
2 base of each semiconductor fin.

1 84. The chip of claim 75 wherein the ratio of the doping concentration in a top surface region
2 of the semiconductor fin to the doping concentration in a sidewall region of the semiconductor
3 fin is between about 1 and about 4.

1 85. The chip of claim 75 wherein first and second sidewall regions are doped to a doping
2 concentration greater than about $1 \times 10^{20} \text{ cm}^{-3}$.

1 86. The chip of claim 75 wherein the insulator layer comprises silicon oxide.

1 87. The chip of claim 75 wherein the insulator layer has a thickness of between about 100
2 angstroms and about 2000 angstroms.

1 88. The chip of claim 75, further comprising of a gate dielectric layer overlying a portion of
2 the semiconductor fin and underlying the gate electrode.

1 89. The chip of claim 88 wherein the gate dielectric layer comprises silicon oxide.

1 90. The chip of claim 88 wherein the gate dielectric layer comprises silicon oxynitride.

1 91. The chip of claim 88 wherein the gate dielectric layer comprises a high permittivity
2 material.

- 1 92. The method of claim 91 wherein the gate dielectric layer is selected from the group
2 consisting of La_2O_3 , Al_2O_3 , HfO_2 , HfON , ZrO_2 .
- 1 93. The chip of claim 91 wherein the gate dielectric layer comprises of high permittivity
2 materials with relative permittivity greater than 5.
- 1 94. The chip of claim 74 wherein the gate dielectric has a thickness of between about 3 and
2 about 100 angstroms.
- 1 95. The chip of claim 74 wherein the gate electrode comprises poly-crystalline silicon.
- 1 96. The chip of claim 74 wherein the gate electrode comprises a metal.