

ABSTRACT OF THE DISCLOSURE
SPACER FLASH CELL PROCESS

A flash EPROM cell has a reduced cell size by providing vertical coupling between the floating gate and the bit line during programming. The erase operation is done by tunneling of electrons from the sharp tip of the Poly spacer to the control gate. The cell is adapted so that the source for each cell within the array is the source of an adjacent cell and the drain is the drain to another adjacent cell. The cell is formed by forming the drain regions into the substrate through openings in a first insulator that is preferably the field oxide. A second insulator is deposited over the first insulator, over the substrate and along the side walls of the openings and is preferably a thin layer so that the opening is covered with a thin insulating layer. The insulated opening is filled with a first doped polysilicon layer. The field oxide is selectively removed. A gate oxide is grown and a second polysilicon layer is formed and then etched to form spacers along the edges of the first polysilicon/second insulator structure. The second polysilicon is selectively etched and a tunneling insulator layer is formed thereover. A third polysilicon layer is formed over the tunneling insulator.

(Figure 1)