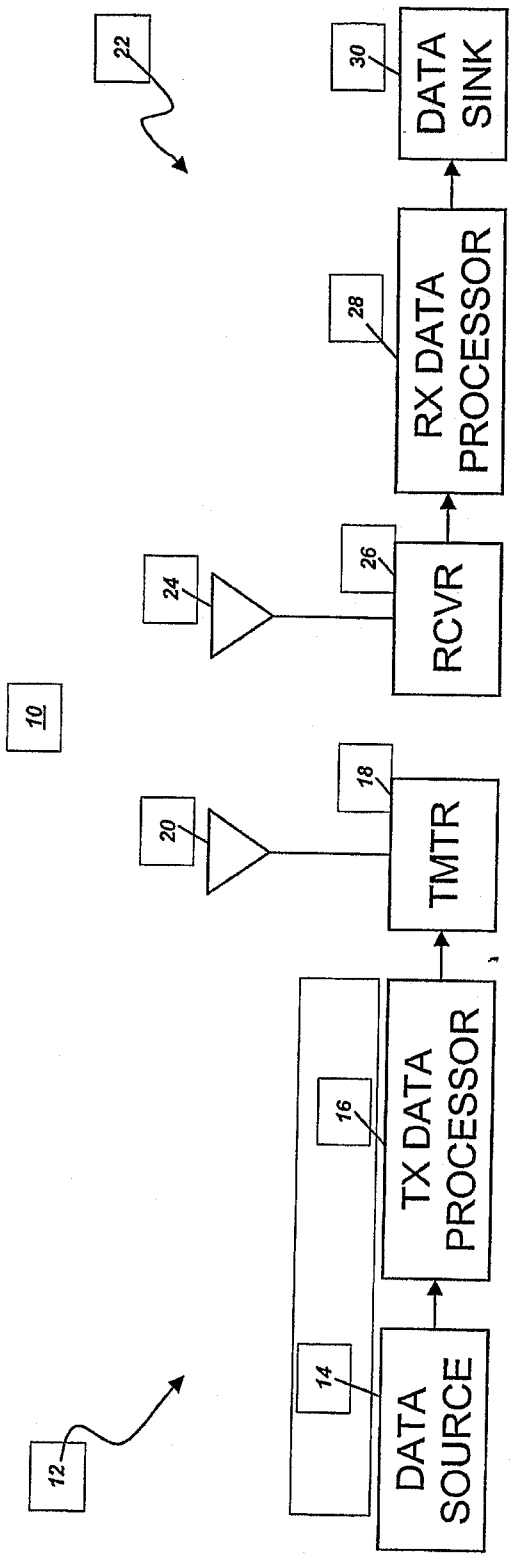

22
30
DATA SINK
28
RX DATA PROCESSOR
24
26
RCVR
10
18
TMTR
20
16
TX DATA PROCESSOR
14
DATA SOURCE
12

FIG. 1

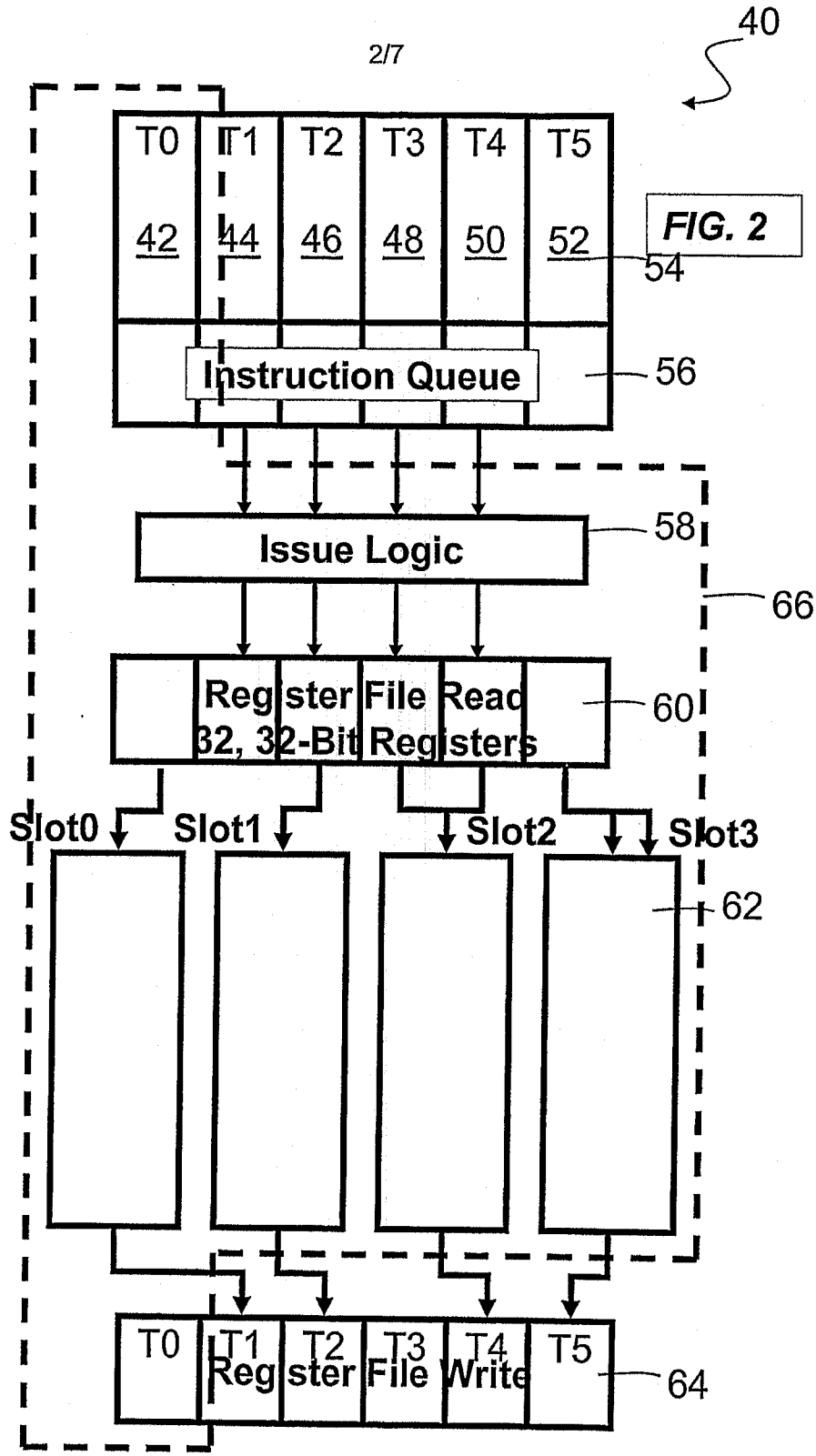

40
T0
T1
T2
T3
T4
T5
42
44
46
48
50
52
54
Instruction Queue
56
Issue Logic
58
66
Register File Read
32, 32-Bit Registers
60
Slot0
Slot1
Slot2
Slot3
62
T0
T1
T2
T3
T4
T5
Register File Write
64

FIG. 2

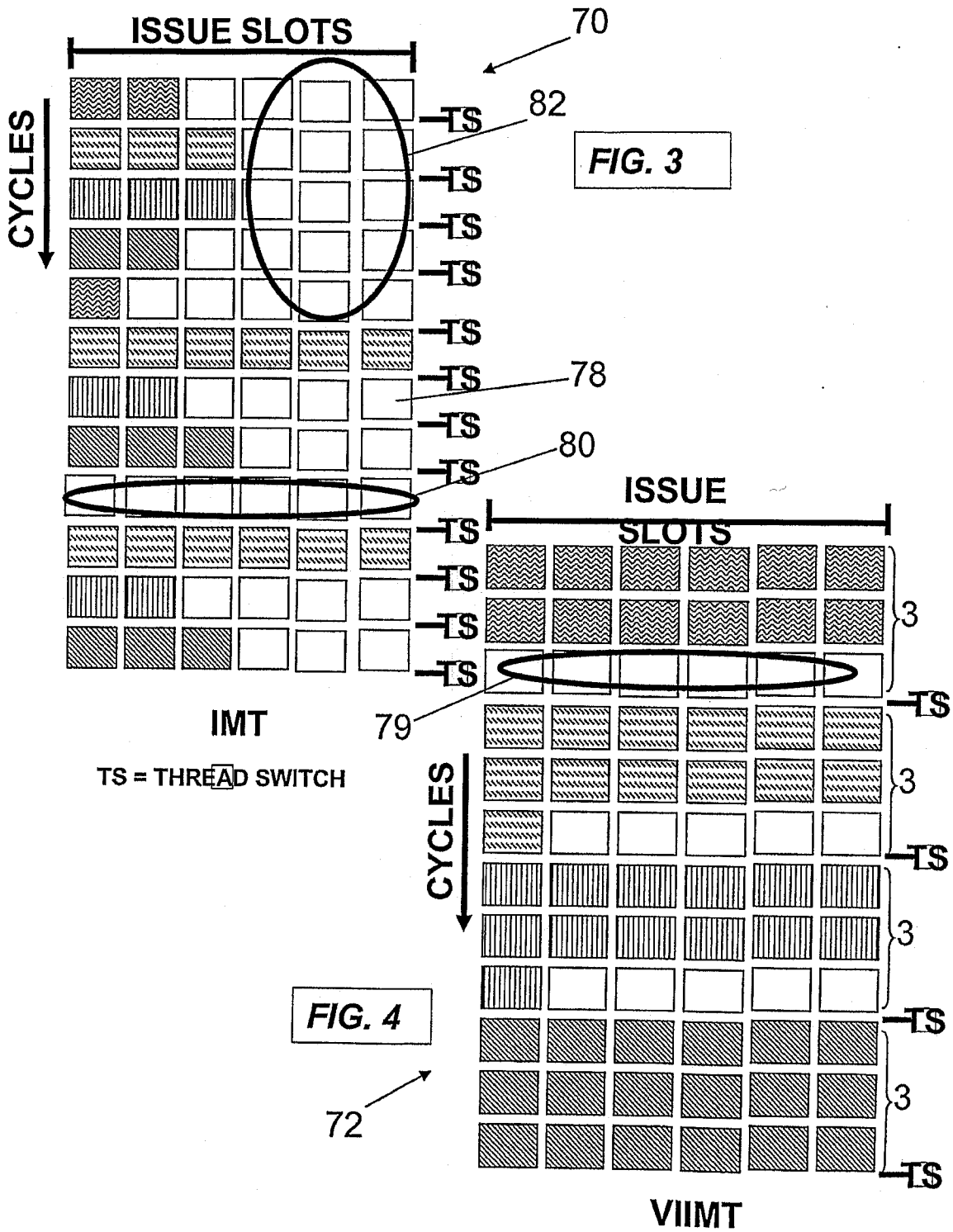

ISSUE SLOTS
70
82
CYCLES
TS
78
80
ISSUE SLOTS
3
IMT
79
TS = THREAD SWITCH
CYCLES
72
VIIMT

FIG. 3

FIG. 4

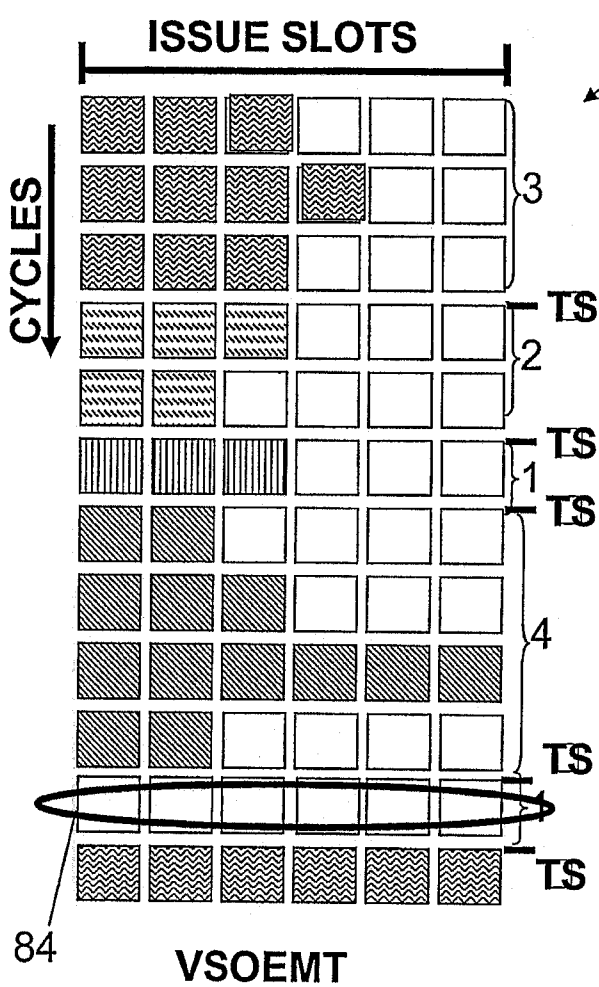

ISSUE SLOTS
74
CYCLES
3
TS
2
TS
TS
1
TS
4
TS
TS
84
VSOEMT

FIG. 5

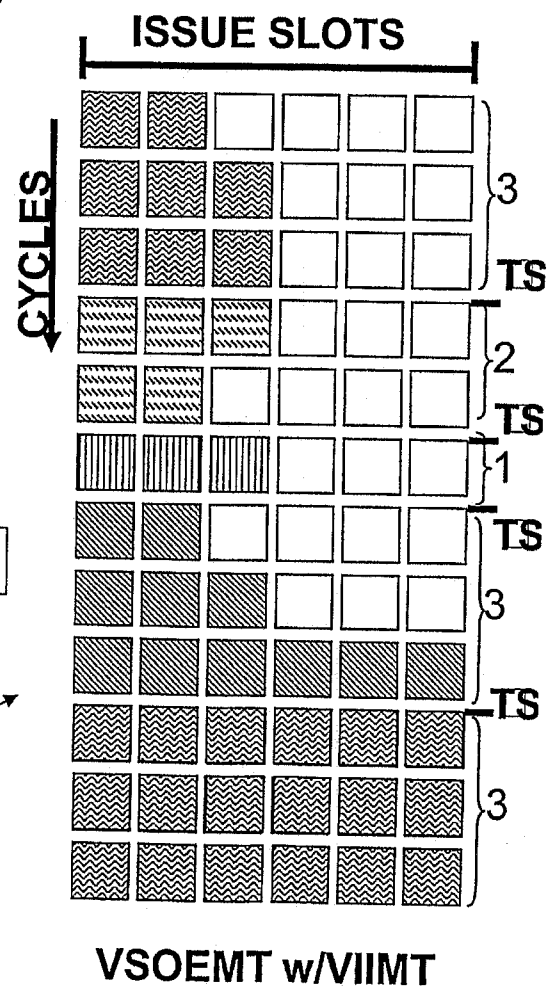

ISSUE SLOTS
CYCLES
3
TS
2
TS
1
TS
3
TS
3
76
VSOEMT w/VIIMT

FIG. 6

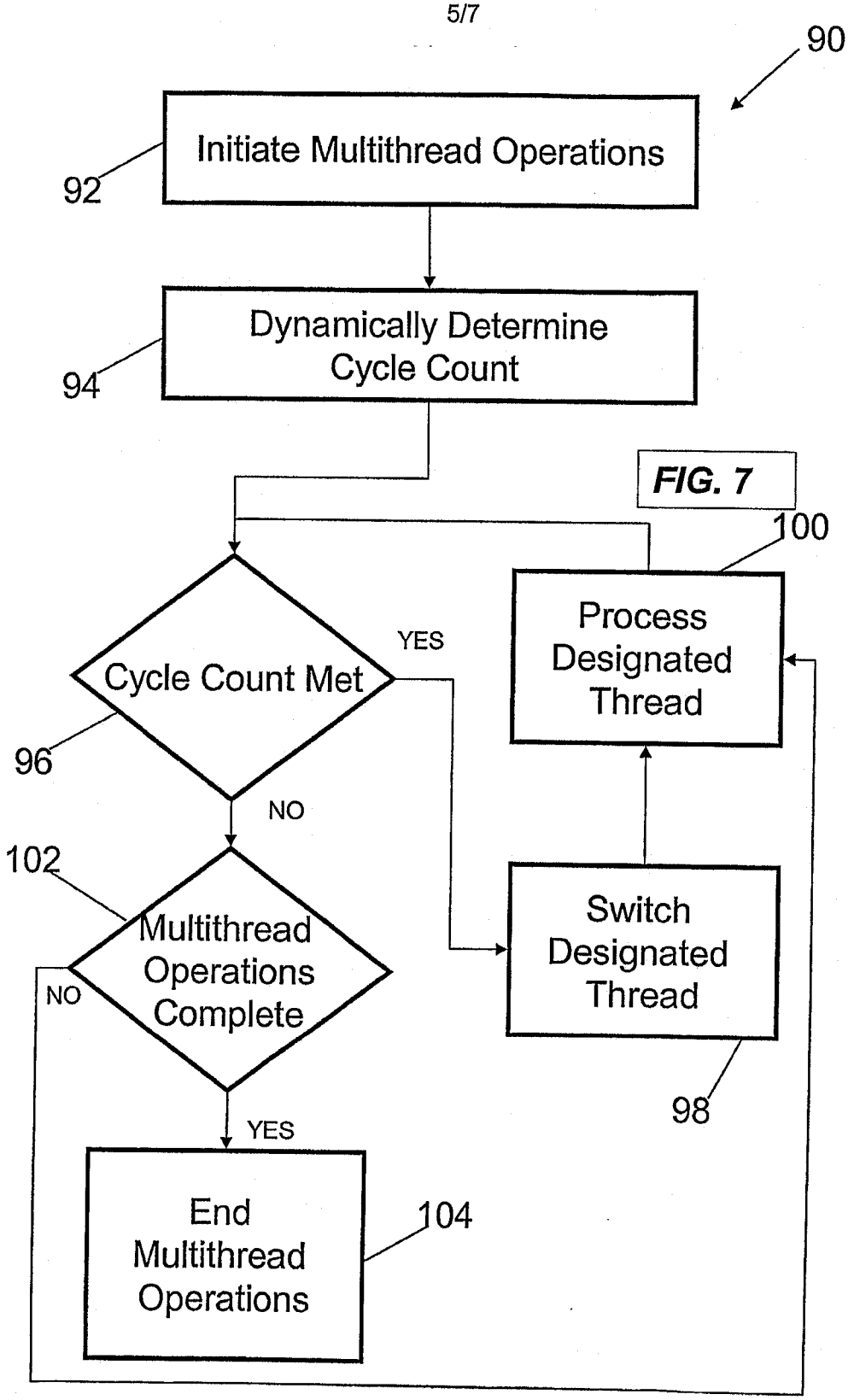

90
Initiate Multithread Operations
92
Dynamically Determine Cycle Count
94
Cycle Count Met
96
YES
NO
Process Designated Thread
100
Switch Designated Thread
98
Multithread Operations Complete
102
NO
YES
End Multithread Operations
104

FIG. 7

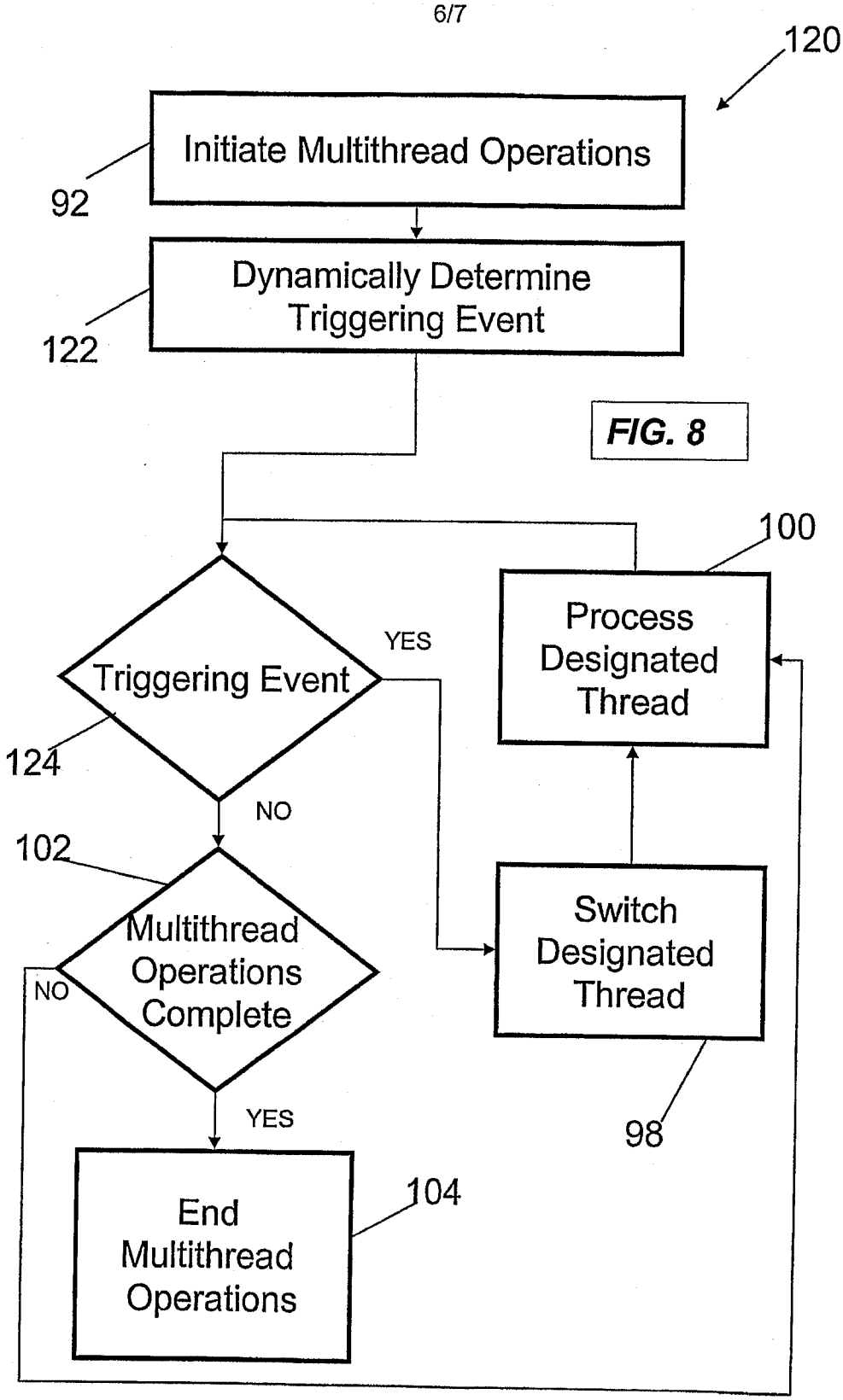

120
Initiate Multithread Operations
92
Dynamically Determine Triggering Event
122
Triggering Event
124
YES
NO
Process Designated Thread
100
Switch Designated Thread
98
Multithread Operations Complete
102
NO
YES
End Multithread Operations
104

FIG. 8

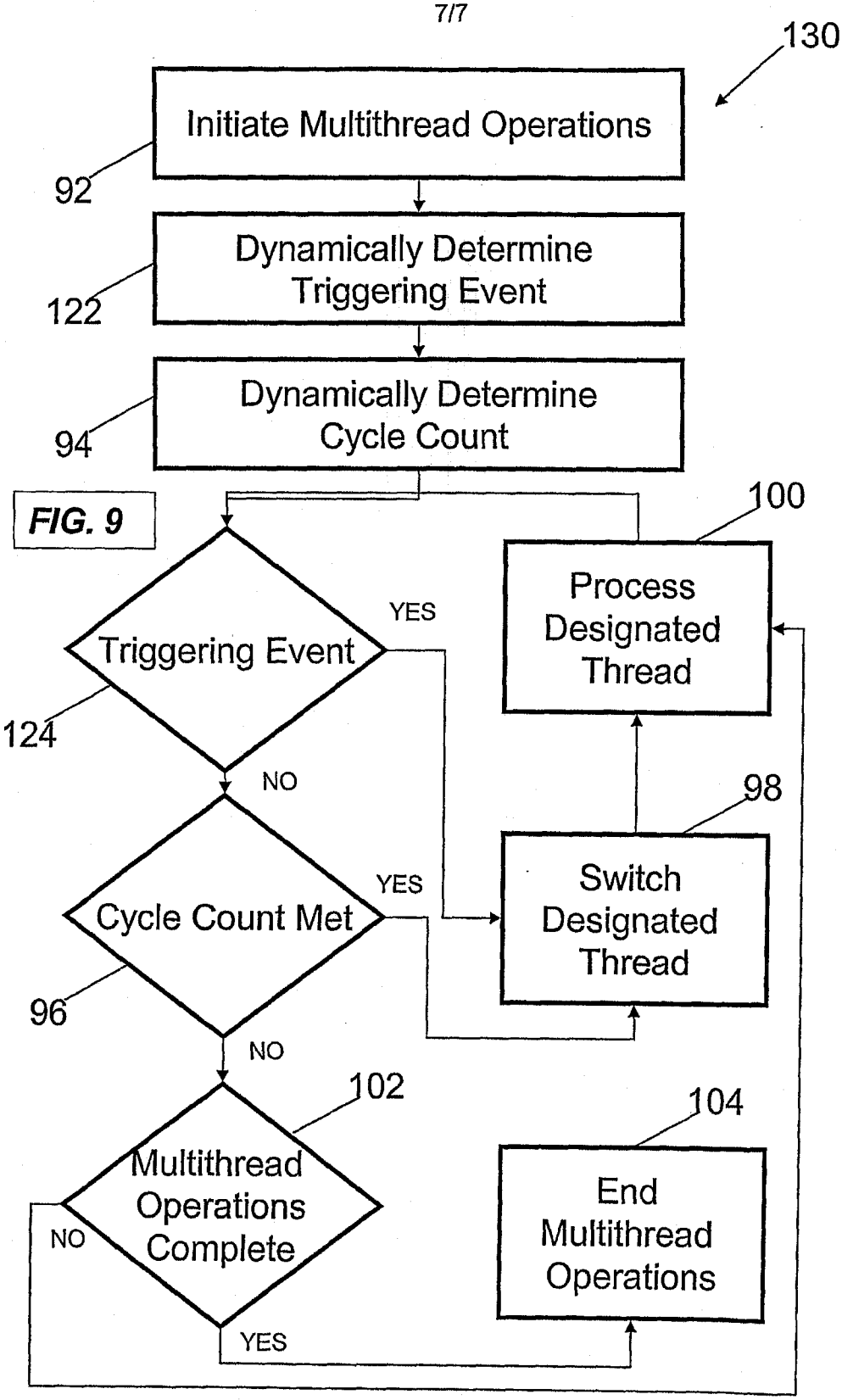

130
Initiate Multithread Operations
92
Dynamically Determine Triggering Event
122
Dynamically Determine Cycle Count
94
100
Process Designated Thread
Triggering Event
YES
124
NO
98
Switch Designated Thread
Cycle Count Met
YES
96
NO
102
104
Multithread Operations Complete
End Multithread Operations
NO
YES

FIG. 9