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COMPLETE SPECIFICATION.

Insulated Isolation Techniques in Integrated Circuits.

We, TEXAS INSTRUMENTS, INCORPORATED, a Corporation organized according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to manufacture of circuit components and of integrated circuits, especially of miniature electronic circuits of the type having all of the necessary circuit components joined together by a common substrate but electrically isolated through the substrate.

There has been a substantial growth of interest in microminiaturization especially in that area of electronics commonly referred to as "microelectronics". Within the semiconductor field in particular, this interest has been reflected by the rapid development of integrated circuitry. Generally speaking, the area of integrated circuits may be resolved into two broad classes. The first is referred to as the "chip approach" wherein individual components such as transistors, resistors, and diodes, are formed on separate pieces of semiconductor material, the separate components thereafter being mounted on an insulating substrate and interconnected in a single package to produce a circuit function. The second class, by far having the greatest potential in microelectronics due to the greater reliability in performance and substantial savings in cost and space, involves having all of the individual active and/or passive components formed on a single piece of semiconductor material, preferably a single crystal, the

components being interconnected to perform the desired circuit function.

The formation of all components in one single crystal semiconductor substrate, however, presents the problem of electrically isolating the circuit components from one another. In particular, when a number of transistors are formed within one portion of the substrate, with the substrate forming the collector region, it is necessary for many circuit applications to isolate the transistors to avoid having the collectors commoned. In the "chip approach", isolation is achieved by separating the devices mechanically, but where all the components of a particular circuit are upon one semiconductor substrate, achieving adequate isolation is one of the principal problems.

Many techniques have been developed to solve this problem, all of them possessing certain disadvantages. One such process involves producing a series of islands of one conductivity type semiconductor material within a substrate of opposite conductivity type material, and biasing the substrate with respect to the rest of the circuit so that the junctions separating the islands from the substrate are never forward biased. The islands form the collectors of transistors, and subsequent diffusions are made into the islands to form the base and emitter regions. Chief among the problems associated with this technique, however, is the fact that the inherent capacitance of the isolation junctions produces undesirable coupling at high frequencies. Also, the circuits and biasing levels must be designed so as to insure that the isolation junctions are not forward biased at any time under normal operating conditions. Even if the junctions are maintained in a reverse biased condition,

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undesirable effects can result from the collection of carriers by the isolation junction.

Another technique for isolation involves having the isolation islands in which the components are subsequently constructed consist of the original wafer doping. Isolation is then achieved by selective diffusion of material of opposite conductivity type from each side of the wafer and completely through the wafer so that the diffusion fronts intersect. A disadvantage of this process is that the diffusions through the wafer require thin wafers and long diffusion times with high surface concentrations, resulting in high isolation capacitance.

There is also known in the art a method of isolation referred to as "insulated isolation" which partially solves the above-mentioned problems. In accordance with this method, a series of mesas are etched upon one face of a monocrystalline semiconductor wafer. These mesas are then coated with an insulating medium, such as silicon oxide, and a thick layer of semiconductor material is subsequently grown over the top of the wafer so as to completely cover the oxide. The semiconductor wafer which forms the substrate, is then removed by lapping, leaving only the mesa regions supported by the grown semiconductor layer but isolated therefrom by the insulating material. Circuit elements such as transistors, resistors, or other appropriate devices are then formed in the unremoved monocrystalline portion of the mesa by the usual techniques, and will be electrically isolated from each other by the silicon oxide insulating medium. Although the process, as a whole, has proven to possess substantial advantages over other methods of isolation, problems are involved when the circuit elements to be formed are active devices. In particular, since the collector region of a transistor, being the unremoved portion of the monocrystalline substrate, is directly adjacent the insulating medium, subsequent electrical contact to be made to this region may conveniently be made only at the surface of the wafer. This restriction means that all the collector current must flow laterally through the lightly doped collector region to the collector contact made in the surface, and a very large collector spreading resistance is consequently added.

To overcome this difficulty, it has been found that if a layer of low resistivity semiconductor material is located intermediate the collector region and the insulating medium, the collector current flow, particularly in the lateral direction, will encounter less opposition, the collector spreading resistance thereby being lowered. In accordance with this objective, therefore, it has been the practice to incorporate an extra step in the "insulated isolation" technique

previously described, the slice of original monocrystalline material being initially subjected to a diffusion operation to produce a shallow low resistivity semiconductor region. The mesas are then etched, and an insulating medium and thick layer of semiconductor material formed as before. The difficulty with this approach, however, is encountered during the lapping step used to remove a portion of the substrate material. Since the operating characteristics of a transistor are largely dependent upon the width of the collector region, close control needs to be maintained over the amount of substrate material removed. However, due to the limitation of the tolerances that may be achieved by lapping, it is very difficult, if not impossible, to produce a collector region adjacent the low resistive semiconductor region having precise dimensions. This difficulty is complicated even more by the bowing of the semiconductor wafer during lapping.

Another disadvantage associated with the process described above is the fact that the low resistivity semiconductor region will be buried within the wafer below the base and emitter regions, and a separate diffusion step will be required in order to make contact at the surface.

The present invention proposes a method for use during fabrication of semiconductor devices, comprising forming individual surface exposed regions of low resistivity semiconductor material in a substrate, the said regions being isolated from each other by insulating material, forming an insulating mask on a surface on the substrate adjacent the said individual regions to leave uncovered selected portions of at least some of those regions, removing uncovered portions of those regions to a depth insufficient to penetrate those regions, and depositing high resistivity semiconductor material of the same conductivity type as the low resistivity material within the respective spaces previously occupied by the material removed from those regions.

In a preferred embodiment of this invention, a series of mesas are initially etched on the face of a wafer of low resistivity semiconductor material. These mesas are then coated with an insulating medium, such as silicon oxide, for example, and a thick layer of semiconductor material is subsequently grown over the surface of the wafer so as to completely cover the oxide. A substantial portion of the substrate is then removed by lapping. An insulating oxide layer is placed over the unremoved portion of the low resistivity material. Using conventional photographic masking and etching techniques, the oxide is selectively removed so as to expose portions of the low resistivity materials within the mesa regions. The

entire wafer is then subjected to a vapor etching process which selectively removes a portion of the low resistivity material. Thereafter, using epitaxial techniques, a layer of high resistivity monocrystalline semiconductor material is redeposited within the space left vacant by the selective vapor etch step. Into this layer subsequent depositions carried out to form diode or transistor structures, for example. Since the high resistivity layer which constitutes the collector region in a transistor, is formed by selective vapor etch and epitaxial deposition rather than by lapping, close control may be maintained over its dimensions. In addition, using the process of this invention, contact may be made directly to the low resistivity layer at the surface of the wafer without the requirement of an extra diffusion step.

By way of example, reference will now be made to the following detailed description of illustrative embodiments, read in conjunction with the accompanying drawings, wherein:

Figure 1 is an isometric pictorial view in section of a semiconductor wafer in an early stage of the production of an integrated circuit in accordance with the process of this invention;

Figures 2-4 are elevational views in section of the semiconductor body of Figure 1, taken along the line 2-2, in successive stages of production;

Figure 5 is an isometric pictorial view of the lower side of the semiconductor body of Figure 4;

Figures 6 and 7 are sectional views of a portion of the wafer of Figure 5 taken along the line 6-6, showing subsequent steps of the process of this invention;

Figure 8 is a front elevation, partly in section, of one form of apparatus used in the process of this invention;

Figure 9 is the same sectional view as Figure 6 and 7 after diffusion operations have been completed and interconnections have been applied;

Figure 10 is an isometric pictorial view of the completed device described with reference to Figures 1-9;

Figure 11 is a schematic diagram of the integrated circuit contained within the device of Figure 10; and

Figures 12-16 are sectional views of a semiconductor wafer showing subsequent steps in the manufacture of an integrated circuit having several circuit components joined by a common substrate but electrically isolated through the substrate.

Referring now to Figure 1, there is now described the first step in practicing a method embodying this invention. A slice of single-crystal low resistivity N+ semiconductor material, such as silicon, having a resistivity of perhaps 0.010 to 0.025 Ω/cm

is used as the starting material. This slice may be about one inch in diameter and ten mils thick. A small segment of the slice may be represented as a chip or wafer 10, which represents the segment occupied by one integrated circuit. Actually, the slice would contain dozens or even hundreds of the segments such as the wafer 10. The top surface of the slice is first masked and etched to form a pattern of raised mesas 11-15. The masking may be by a material such as wax, or preferably by the photoresist techniques which permit excellent geometry control. The height of the mesas 11-15, or in other words the depth of the etching, may be about two mils. At this point the top surface of the slice is covered with an insulating coating 16, silicon oxide for example, which may be formed by any conventional technique to a thickness of perhaps 10,000Å. For instance, the coating 16 may be thermally grown by exposing the slice to steam at about 1200°C. The mesas are now masked with photoresist and the oxide coating selectively removed in the surrounding areas by etching, leaving oxide layers 17 on each mesa, as seen in Figure 2. Alternatively, the oxide coating 16 may be left on at this stage, the layers 17 being produced by a subsequent lapping operation. The top surface of the slice is then cleaned to remove all traces of oxide, organics from the photoresist, and other contaminants from the uncoated areas 18, and the slice is placed in an epitaxial reactor to produce the top layer which eventually becomes the substrate.

Within the reactor a layer 20 of semiconductor material is grown over the top surface of the slice 10 as seen in Figure 3. The most common method of vapor deposition is by the hydrogen reduction of silicon tetrachloride, a technique well known in the art and requiring no elaboration here. This epitaxial growth begins in the areas 18 since the semiconductor material may not adhere to the silicon oxide layers 17. After the thickness of the grown layer reaches the tops of the mesas, however, subsequent growth will spread out and over the entire surface on the layered assembly. The conductivity-type of the layer 20 is not critical as it may be N-type, P-type or intrinsic, and the thickness of the layer should be perhaps seven or eight mils or more to facilitate handling the unit without breakage.

Although one method of depositing the layer 20 has been described, this is by no means restrictive, as other methods well known in the art for depositing semiconductor material may be used in the process of this invention. Also, even though the term epitaxial has been used, implying a continuation of crystalline orientation from the slice to the grown layer, this need not be the case since the grown layer may also be either

polycrystalline or amorphous, thereby increasing the isolation between elements even more.

As the next step in the process being described the structure of Figure 3 is subjected to a lapping and polishing treatment on its lower face to remove all of the original N+ material except that portion remaining within the mesas 11—15, as illustrated in Figure 4. It is to be noted, as a particular feature of this invention, that the degree of lapping is not critical, and although Figure 4 depicts the surface or face 21 as being perfectly flat and the regions of unremoved N+ material within the mesas thereby being of identical depth, in practice it would be impractical, if not impossible, to achieve such close tolerances. Moreover, since the dimensions of the N+ layers within the mesas 11, 13 and 15 do not seriously affect the operating parameters of the devices subsequently to be formed within these areas, there is no requirement for precise lapping.

Inverting the device and looking at what was the bottom surface or face 21 of Figure 4, but will now be considered the top face of the unit, the structure will appear as in Figure 5. Each of the low resistivity N+ monocrystalline portions 11—15 is insulated from the others and from the substrate or layer 20 by the silicon oxide coating 17. This oxide coating 17 is not shown to scale in the drawings, and would actually be perhaps an order of magnitude thinner in proportion than is shown in the sectional views of the drawings.

An oxide layer 22 is then formed upon the upper surface or face 21 of the wafer 25, as depicted in Figure 6. The oxide layer, which might be silicon oxide for example, should preferably be of a thickness in excess of 10,000 Å, and may be formed by any conventional technique. For example, it may be thermally grown by heating the entire structure to a temperature of approximately 1300°C in the presence of oxygen.

An alternative method of forming the oxide layer 22, however, would be the "oxidative" technique, by which oxygen and tetraethoxysilane are reacted in vapor form at 250—500°C. The reaction mixture is obtained by bubbling oxygen through liquid tetraethoxysilane at room temperature, then combining the gaseous mixture with excess oxygen and passing it into a furnace tube containing the wafer 25 where the oxidation takes place. The silicon oxide thereby produced is deposited upon the upper surface or face 21. A typical reaction condition for the oxidative method involves, by way of example, a flow rate of one cubic foot of oxygen per hour into the liquid tetraethoxysilane. The reaction mixture is then mixed with excess oxygen, also at a rate of one cubic foot per hour, and passed into the

tube. At 500°C in a two-inch diameter quartz furnace tube, excellent deposits of silicon oxide are formed at rates from 1300—1400 Å per hour. The advantages of this process is the relatively low temperatures at which uniform oxide coatings can be formed.

Through the use of photographic masking and etching techniques, for example, a select portion of the oxide layer 22 is removed so as to expose a corresponding portion of the low resistivity semiconductor substrates 12 and 14 within the apertures or windows 26 and 27, respectively. This removal may be accomplished by covering the oxide layer 22 with photoresist, exposing and developing the photoresist, and etching away the unmasked areas of the oxide. By this method, the oxide mask shown in section in Figure 6 is produced directly on the substrate surface 21. The mask thus produced will limit the area of the substrate that is to be affected by the subsequent vapor etch and epitaxial redeposition steps.

As the next step in the process the wafer 25 is subjected to a selective vapor etch which removes a select portion of the low resistivity substrate 12 and 14 below the dotted line 21a, as observed in Figure 6. The wafer 25 is thereafter subjected to an epitaxial deposition step whereby, as shown in Figure 7, regions 30 and 31 of high resistivity N-type semiconducting material will be redeposited within the vacant space produced by the vapor etch step previously described. The N-type regions 30 and 31 are formed adjacent the low resistivity N+ regions 12 and 14, also depicted in Figure 7.

In practicing the invention, various desired arrangements may be utilized as well as various techniques applied in order to accomplish the steps of vapor etching and epitaxially redepositing within the unmasked regions. In particular, however, it is desirable to use a process which brings the transformation from an etching condition to a depositing condition as smoothly as possible and with a minimum of cost. In line with this objective, therefore, there is presently described a process whereby the wafer 25 is placed within a reactor whose reactor constituents, during etching, are substantially the same as those during the epitaxial deposition. The basic formula for this operation is $\text{SiCl}_4 + 2\text{H}_2 = 4\text{HCl} + \text{Si}$. This reaction is forced to the left by an addition of an excess of HCl, thus creating an etching condition. To change from an etching condition to one of deposition, (i.e., when the reaction proceeds to the right) merely calls for the termination of the HCl flow which, in turn, brings about a gradual change from an etching condition to one of deposition.

Referring to Figure 8, apparatus for etching and redepositing in accordance with this

process comprises a reactor in the form of a tube 34 having heating coils 31. The furnace may be of a horizontal or vertical type, and may be suited for single or multiple slices, and may be either resistively or inductively heated. The silicon wafers including the wafer 25 are disposed within the furnace in such a position as to expose the slices to gases directed into the tube through a conduit 135. The hydrogen chloride and the silicon tetrachloride vapor are respectively introduced into the conduit 135 from a cylinder 32 containing anhydrous hydrogen chloride and from flask 33 containing liquid silicon tetrachloride, through which hydrogen gas is bubbled. The vapor pressure of the silicon tetrachloride is controlled by submerging the flask 33 in an ice bath. Purified dried hydrogen enters end 136 of the conduit. The flow of the gasses into the tube furnace 34 is regulated by conventional valves.

With the valves adjusted so that an excess of hydrogen chloride vapor is introduced into the reactor, the wafer 25 will be subjected to a selective vapor etch. While the oxide mask 22 will be substantially unaffected, select portions of the low resistivity N+ substrate regions 12 and 14 are removed as shown in Figure 6. The etchant itself will comprise a mixture of silicon tetrachloride, hydrogen chloride, and hydrogen. Alternatively, the valve controlling the flow of silicon tetrachloride may be closed, and an etchant comprising hydrogen chloride and hydrogen may successfully be used to remove the silicon substrate. The rate of etching as well as the dimensions of the etched regions will be determined largely by the configuration and size of the oxide masking 22, as will be observed by a comparison of the area of substrate removed below the aperture 26 with the substrate removed below the aperture 27. Other factors that will affect the rate of etching are the temperature at which the reactor is maintained, the flow rate through the conduit 135, and the percentage composition of the etchant. For example, for one particular configuration of the oxide mask 22, when the flow rate was kept at 15 litres minute, the temperature at approximately 1200°C, and the etchant consisted of 95% H₂ and 5% HCl, the silicon substrates 12 and 14 etched at a rate of approximately 3 microns/minute.

After the desired amount of the low-resistivity silicon has been removed from the wafer by the above-described process, the valves are closed to terminate the flow of the hydrogen chloride, the gas flow through the conduit 135 then consisting of hydrogen and silicon tetrachloride. Doping impurities may be introduced into the gas stream by placing an appropriate impurity-containing

compound, such as a halide of phosphorous, into the flask 33, or in a similar flask if a different temperature is required. With this arrangement, and due to the hydrogen reduction of the silicon tetrachloride, lightly doped N-type silicon is deposited upon the slice 25 within the apertures 26 and 27 and grows epitaxially upon the N+ silicon substrates 12 and 14. The deposition will continue until the regions 30 and 31 of the lightly doped N-type silicon are formed within the vacant areas previously produced by the vapor etch step and adjacent the N+ regions 12 and 14 respectively, as shown in Figure 7.

Although a particular method and particular materials have been described in selectively removing the N+ low resistivity substrate material and epitaxially redepositing the N-type material, any variations of the materials or the techniques may be utilized as long as the broad concept of selective vapor etch and epitaxial redeposition is employed. Using this concept, close control may be maintained over the dimensions and the configuration of the N-type regions. In addition, it is to be observed from Figure 7 that contact may be made to the N+ regions 12 and 14 at the surface of the wafer 25 by cutting through the oxide layer 22 without the necessity of a subsequent diffusion step to reach these regions. As mentioned previously, the N+ layer 12 or 14 allows better low resistance contact to be made to the underside of the N-type region 30 or 31 which serves as one of the active regions of a component in an integrated circuit, for instance the collector region of a transistor.

The selective vapor etch step furnishes two complementary results. In addition to removing the low resistivity N+ substrate as described, it thoroughly cleans the silicon oxide mask 22, thus avoiding undesirable silicon overgrowth on the oxide during the subsequent deposition step, and it also removes contaminants from the surface of the N+ regions upon which the N-type silicon is epitaxially deposited.

In order to more closely control the geometry of the vacant spaces shown below the dotted lines 21a in Figure 6 produced by the vapor etch step, the starting material 10 illustrated in Figure 1 should have a crystal orientation other than the 111 plane. Each of the low resistivity N+ monocrystalline portions 11-15 of Figure 5 have a crystal orientation other than the 111 plane and the vapor etch step as before described may be carried out to produce the vacant spaces illustrated below the dotted lines 21a in Figure 6 and the redeposit step carried out as before described to produce regions 30 and 31 as illustrated in Figure 7. However, it is significant to point out that by using a

starting material with a crystal orientation other than 111 plane, the geometry of the vacant spaces can be more closely controlled so that when regions 30 and 31 are redeposited into the vacant spaces they have a very flat or plane surface thereby allowing more accurate alignment of the masks used in the fabrication of the circuit elements, allowing more uniform diffusion of the regions of these circuit elements and allowing the placement of continuous leads or contacts across the surface of the wafer.

Referring back to Figure 7, it will be observed that the layers 30 and 31 may now serve as active regions into which subsequent diffusions, or upon which epitaxial depositions, may be made in order to fabricate various components of an integrated circuit. Referring now to Figure 9, a sectional view of a completed integrated circuit is seen, with a NPN transistor T_1 and a resistor R_1 having been formed in the N-type redeposition regions 30 and 31 by diffusion. A P-type diffused region provides the base of the transistor, while an elongated P-type region formed simultaneously with the base provides the resistor R_1 . N-type diffused regions provide the transistor emitters. The diffusion operations utilize silicon oxide masking so that the oxide layer 22 acquires a stepped configuration in the final device. Openings are made in the oxide where contact is necessary, then metal film is deposited over the oxide and selectively removed to provide the desired contacts and interconnections. The completed unit is seen in Figure 10, with the transistors T_1 and T_2 and the resistors R_1 , R_2 and R_3 along with the metal film interconnecting providing a logic circuit as seen in schematic form in Figure 11.

The versatility and utility of the process according to this invention, as described above, and in particular the selective vapor etch and epitaxial redeposition steps, allow the fabrication of these discrete circuit components within a single wafer and yet electrically isolated from each other. This may be further illustrated by the following description, in which an NPN transistor, a PNP transistor, a diode, and a resistor, are formed within one segment of a wafer.

Referring to Figure 12, the first step in this fabrication is the formation of a thin oxide layer 37 over the low-resistivity N+ silicon substrate 36 of wafer 35. Using photographic masking and etching techniques, for example, an aperture 38 is formed exposing a portion of the underlying silicon. The wafer is then subjected to an etching process by which a quantity of N+ silicon, defined by the outline is removed. This etching may be achieved by the vapor etch process of the present invention, or alternatively, by any conventional chemical

etching technique which does not substantially affect the oxide mask 37. The wafer is then placed in an epitaxial reactor such as the one shown in Figure 8, and P+ silicon is deposited within the vacant spaces created by the etching step. The P-type conductivity of the silicon may be produced by introducing a halide of boron, for instance, into the flask 33. After the P+ silicon has been formed within the wafer 35 as depicted in Figure 12, the entire wafer is subjected to hydrogen fluoride to completely remove the oxide mask 37, this removal having a negligible effect on the silicon material underneath.

As the next step in the fabrication, a series of mesas 41-44 are etched upon the surface of the wafer 35. The insulating oxide layers may now be formed upon the mesas as previously described. As an alternative, however, it may be desirable first to deposit, by conventional techniques, a layer 39 of metal, such as molybdenum or tungsten, as shown in Figure 13. Being adjacent the low resistivity substrate, the metal layer has the effect of further lowering the resistance in this area. The silicon oxide layer 40 is then formed over the metal layer 39, and the two layers are selectively removed in all regions except over the mesas 41-44, as shown in Figure 13. The semiconductor material 45 is then grown over the entire top surface of the wafer 35, as heretofore described.

The structure of Figure 13 is then subjected to a lapping and polishing step, whereby the substrate material is removed except for the portions making up the mesas 41-44, and the device is rotated 180°. The resulting structure is depicted in Figure 14 where the low resistivity P+ region at the location 44 is electrically isolated from the low resistivity N+ regions at the locations 41, 42 and 43 which are electrically isolated from each other.

The wafer 35 now has an oxide mask 48 formed upon the surface, as depicted in Figure 15 (the manner of formation being similar to that of the oxide layer 22, as described with reference to Fig. 6), and the wafer is then subjected to the selective vapor etch and epitaxial redeposition steps which have been previously described in connection with Figures 6-8. After the N-type regions are formed at the locations 41-43, the oxide mask 48 may be altered at these locations to form the configuration represented by the dotted lines, and another series of selective vapor etch and redeposition steps are utilized to produce regions of P-type silicon above the N-type layers. Similarly, through the use of subsequent oxide masking, selective vapor etching and the redeposition of silicon having different types of doping, or by conventional N- and P-

type diffusions (during which a naturally occurring silicon oxide film forms over the surfaces exposed by the openings in the wide mask 48 shown in Fig. 15), the structure of Figure 16 is produced where a PNP transistor is formed at location 44, a P-N diode at location 43, a resistor at location 42 and an NPN transistor at location 41, all of these components being joined by a common substrate 45 but yet electrically isolated through the substrate. The oxide layer 48 is then selectively cut away and ohmic contacts and interconnections deposited in the form of metal film at the desired locations as shown in Figure 17.

Although specific integrated circuit structures have thus been described, it is obvious that using the method of this invention, a multitude of configurations of circuit components may be formed within one substrate. The use of the selective vapor etch, along with other advantages, accomplishes the cleaning of the oxide and substrate at the same time as it etches away a predescribed portion of the silicon, thus avoiding two steps. The dimensions of the active regions of the various circuit components may be closely controlled by the combination of the vapor etch and epitaxial redeposition, thus increasing the reliability of the device.

While the invention has been described with reference to specific methods and embodiments, it is to be understood that this description is not to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, may become apparent to persons skilled in the art without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. A method for use during fabrication of semiconductor devices, comprising forming individual surface exposed regions of low resistivity semiconductor material in a substrate, the said regions being isolated from each other by insulating material, forming an insulating mask on a surface of the substrate adjacent the said individual regions to leave uncovered selected portions of at least some of those regions, those regions, and depositing high resistivity semiconductor material of the same conductivity type as the low resistivity material within the respective spaces previously occupied by the material removed from those regions.

2. A method according to claim 1, in which the said individual regions are isolated from each other by respective layers of insulating material disposed between the regions and the substrate.

3. A method for fabricating circuit components comprising the steps of forming individual low resistivity semiconductor mesa

regions of one conductivity type on a surface of a semiconductor wafer, forming an insulating layer over each of the mesa regions, depositing support material to overlie the mesa regions, removing the semiconductor material except for the low resistivity material forming the mesa regions, masking parts of the individual low resistivity mesa regions to leave uncovered selected surface portions of at least some of those regions, removing part of the uncovered surface portions of the individual mesa regions to a depth insufficient to penetrate those regions, depositing high resistivity semiconductor material of the said one conductivity type within the respective spaces previously occupied by the material removed from those regions, and forming circuit components in the said high resistivity semiconductor material.

4. A method according to claim 3, in which the circuit components are formed by diffusion of impurities into the high resistivity semiconductor material.

5. A method according to any one of the preceding claims in which the or each insulating layer or mask is formed of silicon oxide.

6. A method according to any one of the preceding claims, in which the removal of parts of the uncovered portions of the said individual regions is effected by vapor etching.

7. A method according to any one of the preceding claims, in which the high resistivity semiconductor material is formed as an epitaxial extension of the low resistivity material remaining in the said individual regions.

8. A method according to any one of the preceding claims, in which the said individual regions are monocrystalline orientated in other than the $\langle 111 \rangle$ plane.

9. The product of a method carried out in accordance with any one of the preceding claims.

10. A semiconductor device comprising a plurality of bodies of monocrystalline semiconductor material in and exposed at a surface of a substrate, the bodies being isolated from each other by regions of insulating material each body comprising a first region of low resistivity semiconductor material containing a second region of high resistivity material of the same conductivity type as the low resistivity material, both the first and second regions being exposed only at the said substrate surface and the second region being of smaller depth than the first region, an insulating layer overlying the said substrate surface and having apertures therein exposing parts of the respective first regions, each aperture containing an ohmic contact to the underlying first region.

type diffusions (during which a naturally occurring silicon oxide film forms over the surfaces exposed by the openings in the wide mask 48 shown in Fig. 15), the structure of Figure 16 is produced where a PNP transistor is formed at location 44, a P-N diode at location 43, a resistor at location 42 and an NPN transistor at location 41, all of these components being joined by a common substrate 45 but yet electrically isolated through the substrate. The oxide layer 48 is then selectively cut away and ohmic contacts and interconnections deposited in the form of metal film at the desired locations as shown in Figure 17.

Although specific integrated circuit structures have thus been described, it is obvious that using the method of this invention, a multitude of configurations of circuit components may be formed within one substrate. The use of the selective vapor etch, along with other advantages, accomplishes the cleaning of the oxide and substrate at the same time as it etches away a predescribed portion of the silicon, thus avoiding two steps. The dimensions of the active regions of the various circuit components may be closely controlled by the combination of the vapor etch and epitaxial redeposition, thus increasing the reliability of the device.

While the invention has been described with reference to specific methods and embodiments, it is to be understood that this description is not to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, may become apparent to persons skilled in the art without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. A method for use during fabrication of semiconductor devices, comprising forming individual surface exposed regions of low resistivity semiconductor material in a substrate, the said regions being isolated from each other by insulating material, forming an insulating mask on a surface of the substrate adjacent the said individual regions to leave uncovered selected portions of at least some of those regions, those regions, and depositing high resistivity semiconductor material of the same conductivity type as the low resistivity material within the respective spaces previously occupied by the material removed from those regions.

2. A method according to claim 1, in which the said individual regions are isolated from each other by respective layers of insulating material disposed between the regions and the substrate.

3. A method for fabricating circuit components comprising the steps of forming individual low resistivity semiconductor mesa

regions of one conductivity type on a surface of a semiconductor wafer, forming an insulating layer over each of the mesa regions, depositing support material to overlie the mesa regions, removing the semiconductor material except for the low resistivity material forming the mesa regions, masking parts of the individual low resistivity mesa regions to leave uncovered selected surface portions of at least some of those regions, removing part of the uncovered surface portions of the individual mesa regions to a depth insufficient to penetrate those regions, depositing high resistivity semiconductor material of the said one conductivity type within the respective spaces previously occupied by the material removed from those regions, and forming circuit components in the said high resistivity semiconductor material.

4. A method according to claim 3, in which the circuit components are formed by diffusion of impurities into the high resistivity semiconductor material.

5. A method according to any one of the preceding claims in which the or each insulating layer or mask is formed of silicon oxide.

6. A method according to any one of the preceding claims, in which the removal of parts of the uncovered portions of the said individual regions is effected by vapor etching.

7. A method according to any one of the preceding claims, in which the high resistivity semiconductor material is formed as an epitaxial extension of the low resistivity material remaining in the said individual regions.

8. A method according to any one of the preceding claims, in which the said individual regions are monocrystalline orientated in other than the $\langle 111 \rangle$ plane.

9. The product of a method carried out in accordance with any one of the preceding claims.

10. A semiconductor device comprising a plurality of bodies of monocrystalline semiconductor material in and exposed at a surface of a substrate, the bodies being isolated from each other by regions of insulating material each body comprising a first region of low resistivity semiconductor material containing a second region of high resistivity material of the same conductivity type as the low resistivity material, both the first and second regions being exposed only at the said substrate surface and the second region being of smaller depth than the first region, an insulating layer overlying the said substrate surface and having apertures therein exposing parts of the respective first regions, each aperture containing an ohmic contact to the underlying first region.



11. A device according to claim 10, including electrical circuit components formed by the first and second regions, the circuit components being electrically interconnected.
12. A device according to claim 11, in which the electrical interconnections are supported by the insulating layer overlying the substrate layer.
13. A method according to claim 3, substantially as described herein with reference to and as illustrated by Figures 1—8 of the accompanying drawings.
14. A method according to claim 13 substantially as further described herein with reference to and as illustrated by Figures 9—11 of the accompanying drawings.
15. A method for fabricating circuit components substantially as described herein with reference to and as illustrated by Figures 12—17 of the accompanying drawings.
16. The product of a process as claimed in any one of claims 13—15.

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