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DRAWINGS ATTACHED



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(54) INFORMATION STORAGE CIRCUITS

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195 Broadway, New York City, New York State, United States of America, a Corporation organized and existing under the laws of the State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to bistable transistor circuits which may be used in semiconductor systems adapted for storage and manipulation of digitally coded information described in our copending Application No. 42607/69 (Serial No. 1,285,956).

As techniques for fabricating monolithic integrated circuits have advanced and integrated circuit costs have decreased, a growing interest in semiconductor memory systems has become evident, and a number of such systems have been proposed heretofore.

In such systems it is generally considered desirable to minimise power dissipation while simultaneously maximising speed of operation and noise margin. In this context, a problem characteristic of prior art systems is that in those systems the amplitudes of the reading signals and the writing signals are dependent upon the standby power levels of bistable circuits therein because the reading and the writing signals must flow through the same resistance circuitry through which the standby current flows. This is disadvantageous because a reduction in standby current (to decrease power dissipation) in such systems entails a corresponding reduction in the amplitudes of reading and writing signals which tends to reduce speed of operation and noise margin.

According to the invention a circuit arrangement for storing and transferring electrical signals received from an information signal path includes a bistable device comprising

first and second bipolar transistors having their emitters connected to a first common potential point the potential of which causes the arrangement to assume an operating or a stand-by state, a first cross-coupling connection from the collector of the first transistor to the base of the second transistor comprising first and second resistors connected in series, a second cross-coupling connection from the collector of the second transistor to the base of the first transistor comprising third and fourth resistors connected in series, fifth and sixth resistors connecting the collectors of the first and second transistors respectively to a second common potential point with no intervening components, and a connection for applying signals from the signal path to the junction point between the first and second resistors, said signal-applying connection including an asymmetrically conducting arrangement connected to the junction point by a seventh resistor, the resistances of the first and second resistor, the fifth resistor and the seventh resistor being so relatively proportioned that the amplitude of the information signals derived from the circuit arrangement through the asymmetrically conducting arrangement are essentially independent of the stand-by power levels.

The coupling means may be any of a variety of apparatus having asymmetrically conducting properties; such as, for example, diodes, transistors, or circuit apparatus comprising diodes, transistors, and/or other circuit elements.

The memory cell is of simple construction and can be made by integrated circuit techniques. It has a low stand-by power dissipation.

When used in a word-organised storage system the emitters are connected to the word line and the digit lines associated with each cell are coupled through the asymmetrical conducting means, which in the preferred embodiment are diodes.

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Information is written into a cell by reducing the voltage on a selected word line and supplying a current to an associated digit line such that current flows through one of the coupling diodes into the cell and sets the cell to a state appropriate to the digit to be stored therein.

Nondestructive readout is achieved by reducing the voltage on a selected word line and detecting the polarity of a voltage differential between the digit lines.

It will be appreciated that the combination of the storage cell and the nonlinear coupling can be used advantageously in digital systems other than memories, for example, in shift registers, adders and counters.

The invention will be better understood from the following more detailed description of an embodiment taken in conjunction with the accompanying drawing, in which:

Fig. 1 shows in block circuit form a word-organized semiconductive memory;

Fig. 2 shows a schematic diagram of a storage cell forming an embodiment of the present invention;

With reference now to the drawing, in Fig. 1 are shown the basic elements of the word-organized memory 10 disclosed in our Application No. 42607/69 (Serial No. 1,285,956). A plurality of individual storage cells 100 are arranged in a two-dimensional array of rows and columns in conventional fashion. Each cell in essence is a flip-flop having two stable states between which it can be switched for the storage of binary digits. As seen, each cell is provided with four terminals, of which one, 101 is connected to a source of electric power, one, 102, is connected to an associated word line, and two, 103 and 104, are connected through coupling diodes, 105 and 106, to separate lines of an associated digit line pair, 107 and 108. Each word line is driven by a word select circuit 110, to which is supplied binary address and timing inputs in the usual fashion. Each pair of digit lines in turn is connected to its own writing circuit 111, to which are applied storage data and timing inputs in the usual fashion. Each pair of digit lines is further connected to its own digit detection circuit 112, to which timing inputs are applied and from which data is extracted in conventional fashion.

Write-in of a word to the cells associated with a particular word line is achieved by supplying a current from the one of the digit lines through one of the diodes connected to each cell in one of the rows while the word line connected to that row is held at a reduced voltage level. For example, to write a word, binary address and timing inputs are applied to the word select circuits 110, one of which in turn reduces the voltage on the particular word line to which it is connected.

Then, information and timing inputs are applied to each write circuit 111 such that a current is supplied to an appropriate one of each digit line pair. Inasmuch as the selected word line is now at a lower voltage than are the other word lines, the digit line current flows into the appropriate cell and sets the flip-flop to a state appropriate to the digit to be stored therein. After the flip-flops are set, the selected word line is returned to the higher stand-by voltage common to the other word lines.

At stand-by, word line and digit line voltage levels are such that the coupling diodes 105 and 106 are reverse-biased. This reverse-biasing electrically isolates a particular cell from the digit lines at all times except when the status of the cell is being detected or changed.

For nondestructive readout of a stored word, the word line voltage is again reduced, and timing inputs are applied to each digit detection circuit 112. The reduced word line voltage is in such relation to other voltages in the system that the coupling diodes 105 and 106 associated with the selected cells tend to become forward-biased. However, only one of the transistors in each cell is "on" at a given time. The coupling diode associated with the "on" transistor will conduct more current from its associated digit line into the cell than does the other coupling diode connected to the cell. In this operation the current which flows from the digit lines through the coupling diodes is primarily a dynamic current, i.e., a current associated with discharging of parasitic capacitances associated with the digit lines and the circuitry attached thereto. Little or no current need be supplied by either the driver circuit 111 or the detection circuit 112 during a read cycle. Accordingly, the unequal current flow from the digit lines causes an unequal discharge of those parasitic capacitances. The detection circuit 112 is a balanced detector which transforms the voltage differential caused by the unequal discharging of parasitic capacitances on the digit lines to a binary output.

In Fig. 2 there is shown a flip-flop according to the present invention especially suited for use as the cell 100 in the memory shown in Fig. 1. More specifically, the circuitry inside the broken line 19 in Fig. 2 comprises the inner structure of a preferred form of each of the cells 100 in Fig. 1. The flip-flop comprises a pair of matched junction transistors 20 and 21, shown here illustratively of the NPN type, connected to form a flip-flop. To this end, the base 23 of transistor 20 is connected through a resistor 29 to a circuit node 33 which is in turn connected through a resistor 30 to the collector 25 of transistor 21. The base 26 of transistor 21 is connected through a

resistor 31 to a circuit node 32 which is in turn connected through a resistor 28 to the collector 22 of transistor 20. The collector 22 of transistor 20 and the collector 25 of transistor 21 are connected through separate load resistors 34 and 35, respectively, to a common terminal 101 which is in turn connected to a source of electric power (+V). The emitters 24 and 27 of transistors 20 and 21 are connected together and to a common terminal 102 which is connected to a word line 109.

Circuit node 32, a common node between the cross-coupling series-pair of resistors 28 and 31, is connected through a resistor 36 to a terminal 103, which in turn is connected through a coupling diode 105 to one line 107 of a pair of digit lines 107 and 108 associated with the cell. Similarly, circuit node 33, a common node between the cross-coupling series-pair of resistors 29 and 30, is connected through a resistor 37 to a terminal 104, which in turn is connected through another coupling diode 106 to the other digit line 108 of the digit line pair.

Typical voltages in the cell may include a power supply voltage (+V) of about 4.5 volts, a standby voltage on digit lines 107 and 108 of about 1.7 volts, and a standby voltage on word line 109 of about 3.5 volts. Under these voltage relationships, diodes 105 and 106 will be reverse-biased, i.e., nonconducting, at standby. This feature enables the elimination of DC current from the digit lines at standby.

During reading and writing operations, the voltage relations are changed such that one or both diodes 105 and 106 become forward-biased and additional current flows from one or both digit lines 107 and 108 into the cell. This feature of bringing an independent amount of additional current into the cell during reading and writing operations achieves the object of having the amplitudes of reading and writing signals independent of standby power dissipation.

It will be apparent from Fig. 2 that for a particular power supply voltage (+V) and for a particular standby voltage on the word line 109, resistor 34 and 35, e.g., 30,000 ohms, primarily determine the power dissipation of the cell during standby. Inasmuch as the dynamic currents, i.e., reading and writing signals, do not flow through resistors 34 and 35, standby power dissipation may be designed to be substantially as low as desired without affecting the dynamic characteristics of the cell.

To exemplify writing into cell 100, assume transistor 20 is "on", and it is desired to switch the state of the cell, i.e., it is desired to switch transistor 21 "on" and transistor 20 "off". The word line 109 is first reduced from standby voltage, e.g., 3.5 volts, to a

lower voltage, e.g., 0.25 volt. Digit line 107 is supplied with a current which flows through diode 105 and resistor 36 into terminal 32. Inasmuch as transistor 20 is "on", most of this current initially flows through resistor 28 and into the collector 22 of transistor 20. This additional current through resistor 28 increases the voltage over resistor 28, which, in turn, increases the voltage at node 32; and current quickly begins to divide and flow through resistor 31 into the base 26 of transistor 21, thus tending to turn transistor 21 "on". In the regenerative manner characteristic of flip-flops, once current commences flowing into the base of transistor 21, its collector voltage, and consequently the base voltage of transistor 20, is lowered, and transistor 20 switches "off". When this switch is completed, current is removed from digit line 107, and word line 109 may be returned to standby voltage, or a read operation may be commenced without first returning the word line voltage to standby.

For nondestructive readout of data from the cell in Fig. 2, the voltage on word line 109 is reduced below its standby value, e.g., to about 0.25 volt, and the voltage difference between digit lines 107 and 108 is sensed. If transistor 21 is "on", a current flows from digit line 108, through diode 106 and resistor 37, and into the collector of transistor 21. This current is a dynamic current which tends to discharge, to some degree, the capacitance associated with digit line 108. A smaller dynamic current also flows from digit line 107, through diode 105, resistor 36, resistor 31, and into the base 26 of transistor 21. Inasmuch as the current flowing from digit line 108 is greater than that flowing from digit line 107, the capacitances associated with digit line 108 will discharge more than those associated with digit line 107. This unequal capacitance discharge causes a voltage difference between digit lines 107 and 108 which is detected by digit detector 112, in Fig. 1, and translated into an output signal. Similarly, if transistor 20 were "on", digit line 107 would discharge more than digit line 108; a voltage difference of opposite polarity would develop between digit lines 107 and 108; and this voltage difference would be detected and translated by detector circuit 112 into a complementary output signal. After readout is complete, the word line voltage may be returned to its standby level, or there may be a successive write operation into the cell without first restoring the word line voltage to standby.

Several system and circuit parameters and considerations of great importance to the best mode contemplated for carrying out our invention will now be described in detail.

First, it is of significant importance that load resistors 34 and 35 be coupled directly to collectors 22 and 25, respectively, as shown in Fig. 2 rather than through resistors 28 and 30, respectively, to these collectors, the latter being commonly done in the art. In one aspect, this feature is one important part of applicants' invention.

To appreciate the importance of this feature, consider the operation of the cell shown in Fig. 2 if load resistors 34 and 35 were coupled through resistors 28 and 30, respectively, to the collectors of transistors 20 and 21. In this case a decrease in word line voltage to initiate a read operation will cause an increased amount of current (above the standby current) to flow through load resistors 34 and 35 and necessarily also through resistors 28 and 30, respectively. This increased current through resistors 28 and 30 would decrease the amount of signal current (from the digit lines) which could be allowed to flow through resistor 28 or 30 before enough voltage were developed at node 32 or 33 to switch the state of the cell. Thus, the allowable signal current and, accordingly, the noise margin, in a read operation would be significantly reduced.

It is also important to use resistors 36 and 37 through which the cell of Fig. 2 is coupled to diodes 105 and 106, respectively. In the absence of resistors 36 and 37, the voltage on digit lines 107 and 108 would be limited and would have to be carefully controlled to avoid switching the state of the cell during a read operation because the only voltage drop between the cell and the digit lines then would be relatively constant (about 0.7 volt) drop over each of the diodes 105 and 106. To appreciate this it must be remembered that during a read operation, one must be careful to avoid developing a voltage on whichever of nodes 32 or 33 is coupled to the base of the "off" transistor sufficient to turn on that transistor. Otherwise, destructive readout would result and the stored information would be lost. Inclusion of resistors 36 and 37 tends to decrease the voltages at nodes 32 and 33; and so tends to increase the required signal amplitude and noise margins during a read operation.

Also of importance is that a particular ratio of resistors 36 and 37 to resistors 28 and 30, respectively, be maintained for optimum results. It is desirable that the ratio of resistor 36 to resistor 28 (and of resistor 37 to resistor 30) be maximised for a reading operation, but minimised for a writing operation. In general, the reconciliation of these opposing requirements will depend upon obtaining the best balance between noise margin and speed of operation. However, in all cases the ratio should

be at least 1; in most cases the ratio should be about 1.5—2.0; and seldom, if ever, should the ratio be greater than 3 or 4, for optimum results.

The inclusion of resistors 29 and 31 (rather than coupling nodes 32 and 33 to bases 26 and 23, respectively) is important to maximise the voltage difference developed between the digit lines during a read operation. For optimum results, the resistance of resistor 29 should approximately equal that of resistor 28, and the resistance of resistor 31 should approximately equal that of resistor 30.

Since balanced bistable operation is contemplated, corresponding elements in the two halves of the flip-flop of Fig. 2 should be matched for optimum results. That is, the characteristics of transistors 20 and 21 should be as similar as possible; resistor 29 should equal resistor 31; resistor 28 should equal resistor 30; resistor 36 should equal resistor 37; and resistor 34 should equal resistor 35 also; the characteristics of diodes 105 and 106 should be as similar as possible.

30,000 ohms is typical for load resistors 34 and 35; 1000 ohms is typical for resistors 28, 29, 30, and 31; and 1500—2000 ohms is typical for resistors 36 and 37. Coupling diodes 105 and 106 advantageously are Schottky-barrier diodes so that (1) capacitive loading of digit lines is minimised, and (2) a minimum amount of charge is leaked from a cell to its digit lines as the coupling diodes turn off (because of the minimal minority carrier storage in a forward-conducting Schottky-barrier diode). At the termination of a writing operation a significant portion of the charge stored in the "on" transistor (20 or 21) must not be coupled back out to the digit lines as the coupling diodes turn off, such as would be the case if an unduly great amount of minority carriers were stored in the coupling diodes. Of course, junction diodes may also be used, provided the minority carrier charge storage therein is less than the minority carrier charge storage in the "on" transistor.

It should be noted that throughout the description hereinabove the terms "collector", "base", and "emitter" have been used to refer to the three functional zones within a junction transistor. Generally, there is some parasitic resistance between the functional zone and the electrode coupled to that zone, e.g., a collector series resistance between the collector and the collector electrode; a base series resistance between the base and the base electrode; etc. Thus throughout the description of Fig. 2 it has been assumed that whatever resistance there may be between the true functional zones and their respective nodes 22 and 25 130

("collector"), 23 and 26 ("base"), and 24 and 27 ("emitter") is negligible compared to the resistance expressly specified in Fig. 2.

It will be appreciated by those in the art that when the circuit of Fig. 2 is fabricated in integrated circuit form, resistors 28 and 30 may be specially adapted parasitic collector series resistance; and resistors 29 and 31 may be specially adapted parasitic base resistances. In this case node 32 may be thought of as both the "collector electrode" of transistor 20 and the "base electrode" of transistor 21. Similarly, node 33 could then be thought of as both the "collector electrode" of transistor 21 and the "base electrode" of transistor 20. In this case, load resistors 34 and 35 would not be thought of as being coupled to the collector electrodes, but rather for example, may be thought of as epitaxial resistance zones which terminate at the collector zones within the integrated circuit.

An important advantage of the memory which has been described is that the simplicity of the unit cell 100 readily permits fabrication of at least the basic cell array in monolithic semiconductor integrated circuit form. The design and fabrication of such structures has become well known in the art and will not be described further herein.

Similarly the word select circuit and reading and writing circuits also can take a variety of forms.

In an embodiment, the word lines were at about 3.5 volts during standby periods and during dynamic periods, that is, during reading and writing, were at about 0.25 volts, whilst the digit lines were at about 1.7 volts during standby and at about 1.25 volts during dynamic periods.

It will be appreciated that pairs of digit lines need not be used as shown in Fig. 1 and the cells in a column need be coupled only to one digit line, provided the storage cells are correspondingly adapted for unbalanced operation, in accordance with principles well known in the art. However, balanced operation with pairs of digit lines, as described in detail hereinabove, is considered preferable for optimum system performance.

WHAT WE CLAIM IS:—

1. A circuit arrangement for storing and transferring electrical signals received from an information signal path, including a bi-stable device comprising first and second bipolar transistors having their emitters connected to a first common potential point the potential of which causes the arrangement to assume an operating or a stand-by state, a first cross-coupling connection from the collector of the first transistor to the

base of the second transistor comprising first and second resistors connected in series, a second cross-coupling connection from the collector of the second transistor to the base of the first transistor comprising third and fourth resistors connected in series, fifth and sixth resistors connecting the collectors of the first and second transistors respectively to a second common potential point with no intervening components, and a connection for applying signals from the signal path to the junction point between the first and second resistors, said signal-applying connection including an asymmetrical conducting arrangement connected to the junction point by a seventh resistor, the resistances of the first and second resistor, the fifth resistor and the seventh resistor being so relatively proportioned that the amplitude of the information signals derived from the circuit arrangement through the asymmetrical conducting arrangement are essentially independent of the stand-by power levels.

2. A circuit arrangement according to claim 1 including a second connection for applying signals from an other signal path to the junction point between the third and fourth resistors, the second signal-applying path also including an asymmetrical conducting arrangement connected to the junction point by an eighth resistor, the resistances of the third and fourth resistor, the sixth resistor and the eighth resistor being so relatively proportioned that the amplitude of the information signals derived from the circuit arrangement through the asymmetrical conducting arrangement are essentially independent of the stand-by power levels.

3. A circuit according to claim 1 or 2 wherein the asymmetrical conducting means is a diode.

4. A circuit according to claim 1 wherein the ratio of the resistance of the seventh resistor to the resistance of that one of the first and second resistors which is connected to the collector of the first transistor is less than 4 to 1 and is preferably from 1.5 to 2.0 to 1.

5. A circuit according to claim 2 wherein the ratio of the resistance of the eighth resistor to the resistance of that one of the third and fourth resistors which is connected to the collector of the second transistor is less than 4 to 1 and is preferably from 1.5 to 2.0 to 1.

6. A circuit according to claim 4 wherein the resistance of the fifth resistor is from 15 to 30 times as great as that of the first, second and seventh resistors.

7. A circuit according to claim 5 wherein the resistance of the sixth resistor is from

("collector"), 23 and 26 ("base"), and 24 and 27 ("emitter") is negligible compared to the resistance expressly specified in Fig. 2.

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base of the second transistor comprising first and second resistors connected in series, a second cross-coupling connection from the collector of the second transistor to the base of the first transistor comprising third and fourth resistors connected in series, fifth and sixth resistors connecting the collectors of the first and second transistors respectively to a second common potential point with no intervening components, and a connection for applying signals from the signal path to the junction point between the first and second resistors, said signal-applying connection including an asymmetrical conducting arrangement connected to the junction point by a seventh resistor, the resistances of the first and second resistor, the fifth resistor and the seventh resistor being so relatively proportioned that the amplitude of the information signals derived from the circuit arrangement through the asymmetrical conducting arrangement are essentially independent of the stand-by power levels.

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5. A circuit according to claim 2 wherein the ratio of the resistance of the eighth resistor to the resistance of that one of the third and fourth resistors which is connected to the collector of the second transistor is less than 4 to 1 and is preferably from 1.5 to 2.0 to 1.

6. A circuit according to claim 4 wherein the resistance of the fifth resistor is from 15 to 30 times as great as that of the first, second and seventh resistors.

7. A circuit according to claim 5 wherein the resistance of the sixth resistor is from



15 to 30 times as great as that of the third,
fourth and eighth resistors.

8. A circuit arranged and adapted to
operate substantially as herein described
5 with reference to and as shown in Fig. 2 of
the accompanying drawings.

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