TWO STEP ETCHING OF A BOTTOM ANTI-REFLECTIVE COATING LAYER IN DUAL DAMASCENE APPLICATION

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention generally relates to semiconductor processing technologies and, more specifically, to methods for etching a bottom anti-reflective coating (BARC) layer in a dual damascene etching process.

Description of the Related Art

[0002] Integrated circuits have evolved into complex devices that can include millions of components (*e.g.*, transistors, capacitors and resistors) on a single chip. The evolution of chip designs continually requires faster circuitry and greater circuit density. The demands for greater circuit density necessitate a reduction in the dimensions of the integrated circuit components.

[0003] As the dimensions of the integrated circuit components are reduced (*e.g.* sub-micron dimensions), the materials used to fabricate such components contribute to their electrical performance. For example, metal interconnects with low resistance (*e.g.*, copper and aluminum) provide conductive paths between the components on integrated circuits.

[0004] Copper is particularly advantageous for use in interconnect structures due to its desirable electrical properties. Copper interconnect system are typically fabricated using a damascene process in which trenches and vias are etched into dielectric layers. The trenches and vias are filled with copper which is then planarized using, for example, a chemical-mechanical planarization (CMP) process.

[0005] Copper interconnects are electrically isolated from each other by an insulating material. When the distance between adjacent metal interconnects and/or thickness of the insulating material has sub-micron dimensions, capacitive coupling may potentially occur between such interconnects. Capacitive coupling between adjacent metal interconnects may cause cross talk and/or resistance-capacitance (RC) delay which degrades the overall

performance of the integrated circuit. In order to prevent capacitive coupling between adjacent metal interconnects, low dielectric constant (low k) insulating materials (e.g. dielectric constants less than about 4.0) are needed.

[0006] Figures 1A-1D illustrate an exemplary dual damascene structure formed by a "via-first" processing sequence. Referring first to Figure 1A, a dielectric bulk insulating layer 110 and an underlying dielectric barrier layer 108 are stacked on another previously formed interconnect having a conductive layer 106 embedded in another dielectric bulk insulating layer 104 disposed on a substrate 102. An optional polish stop layer or anti-reflective coating (ARC) 112 may be disposed on the dielectric bulk insulating layer 110. The dielectric bulk insulating layer 110 is typically formed from a dielectric material having a dielectric constant lower than 4.0, such as FSG, polymer material, carbon containing silicon layer (SiOC), and the like.

[0007] A bottom anti-reflective coating (BARC) layer 114 is spin-applied to fill vias 128 formed by a via etching process and covers dielectric bulk insulating layer 110 before trench lithography. A photoresist layer 116 is disposed on the BARC layer 114 and patterned to define an opening 130 for forming trenches. A BARC etching process is performed to clear away a portion of the BARC layer 114 over the via opening 128 masked by the patterned photoresist layer 116 before etching the trenches, as shown in Figure 1B. The BARC etching process is performed until the optional polish stop layer 112 defined by the photoresist layer 116 is exposed and the BARC layer 114 filling the via 128 is etched to a predetermined depth, as shown in Figure 1B. Subsequently, a trench etching process is performed to etch the exposed polish stop layer 112 and the underlying dielectric bulk insulating layer 110 defined by the patterned photoresist layer 116, as shown in Figure 1C. The trench etching process etches the dielectric bulk insulating layer 110 into a predetermined depth and defines trenches 122 in the dielectric bulk insulating layer 110. After the trench 122 has been formed, the remaining BARC layer 114 filling the via 128 and the photoresist layer 116 on the top surface of the dielectric bulk insulating layer 110 are removed from the substrate 102, thereby forming dual damascene structure on the substrate 102, as shown in Figure 1D.

[0008] Typically, during the BARC 114 or photoresist layer 116 removal

process, an oxygen containing plasma etch process is performed to react with the remaining BARC layer 114 and the photoresist layer 116 on the substrate 102, forming a carbon oxide polymer which is pumped out of the processing chamber. However, oxygen present plasma during the removal of BARC layer 114 and photoresist layer 116 may attack the exposed sidewall 120 and surface 126 of the trenches 122 and/or vias 128 formed in the dielectric bulk insulating layer 110. Oxygen may form a Si-O bond on the surface of the dielectric bulk insulating layer 110, which adversely affect the dielectric properties of the dielectric bulk insulating layer 110. For example, oxygen may accumulate on the sidewall 120 or exposed surface 126 of the low-k dielectric bulk insulating layer 110, and penetrate into the porous low-k dielectrics, thereby causing the carbon depletion at the film surface. Carbon depletion may cause the dielectric constant of the low-k material to undesirably increase, resulting in a "k loss" of the material dielectric properties. As a result, cross-talk and RC delay may increase after the BARC and photoresist etching process.

[0009] Furthermore, removal of the BARC and/or photoresist layer removal process may also leave contaminants 124, such as residual BARC, residual photoresist layer, impurities, organic or inorganic byproducts in the vias 128 and/or trenches 122. The contaminants 124 present in the vias 128 and/or trenches 122 may adversely effect the overall integration of the interconnection structure, resulting in poor device reliability and electrical performance.

[0010] Therefore, there is a need for an improved process for removing BARC in an interconnection structure.

SUMMARY OF THE INVENTION

[0011] Methods for removing a BARC layer from a feature are provided in the present invention. In one embodiment, the method includes providing a substrate having a feature filled with a BARC layer in an etching chamber, supplying a first gas mixture comprising NH_3 gas into the chamber to etch a first portion of the BARC layer filling in the feature, and supplying a second gas mixture comprising O_2 gas into the etching chamber to etch the remaining portion of the BARC layer disposed in the feature.

[0012] In another embodiment, the method for removing a BARC layer from

a feature includes providing a substrate having features formed in a dielectric insulating layer and filled with a BARC layer in an etch chamber, supplying a first gas mixture comprising NH_3 into the chamber to etch a portion of the BARC layer filling in the feature, and supplying a second gas mixture comprising O_2 gas into the chamber to etch the remaining portion of the BARC layer in the feature.

[0013] In yet another embodiment, the method for removing a BARC layer from a feature includes providing a substrate having features formed in a dielectric insulating layer and filled with a BARC layer in an etch chamber, wherein the dielectric insulating layer has a dielectric constant less than 3.5, supplying a first gas mixture having NH_3 gas at between about 50 sccm and about 1000 sccm into the etch chamber to etch a portion of the BARC layer filling in the feature, and supplying a second gas mixture comprising O_2 gas at between about 50 sccm and about 500 sccm into the etch chamber to etch the remaining portion of the BARC layer in the feature.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] So that the manner in which the above recited features of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0015] Figures 1A-1D are a sequence of sectional views of an exemplary dual damascene fabrication process;

[0016] Figure 2 is a schematic cross-sectional view of a plasma etching chamber used according to one embodiment of the invention; and

[0017] Figure 3 is a process flow diagram illustrating one embodiment of a method for two step etching method for etching a BARC layer and/or a photoresist layer in a dual damascene structure; and

[0018] Figures 4A-4B are a sequence of sectional views of a dual damascene fabrication process according to one embodiment of the present invention.

[0019] To facilitate understanding, identical reference numerals have been

used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

[0020] It is to be noted, however, that the appended drawings illustrate only exemplary embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

DETAILED DESCRIPTION

[0021] Embodiments of the present invention include methods for two step etching of a BARC layer in a dual damascene structure. The methods preserve the quality of the low-k dielectric film while maintaining a high removal rate by using different gas mixtures at separate BARC layer etching steps in a dual damascene fabrication process.

[0022] The etch process described herein may be performed in any suitable plasma etch chamber. One such etch chamber is the ENABLER® processing chamber, available from Applied Materials, Inc., of Santa Clara, California. It is contemplated that the other etch reactors, including those from other manufacturers, may be adapted to benefit from the invention.

[0023] Figure 2 depicts a schematic cross-sectional view of one embodiment of a plasma etch system 202 suitable for performing one or more steps of the invention. The plasma etch system 202 may include a process chamber body 210 having a conductive chamber wall 230 and a lid 213. The temperature of the conductive chamber wall 230 is controlled using liquid-containing conduits (not shown) that are located in and/or around the conductive chamber wall 230. The conductive chamber wall 230 is connected to an electrical ground 234. A liner 231 is disposed in the process chamber body 210 to cover the interior surfaces of the conductive chamber wall 230. The liner 231 serves as a surface protection layer that protects the interior surface of the chamber wall 230 of the process chamber body 210. In one embodiment, the liner 231 may be fabricated by ceramic materials including Al_2O_3, AlN, silicon carbide, Y_2O_3, and the like.

[0024] The process chamber body 210 is a vacuum vessel that is coupled

through a throttle valve 227 to a vacuum pump 236. A support pedestal 216 is disposed in the bottom of the process chamber body 210 to support a substrate 260 positioned thereon during processing. The support pedestal 216 may include an electrostatic chuck 226 for retaining the substrate 260. A DC power supply 220 is utilized to control the power supplied to the electrostatic chuck 226. The support pedestal 216 is coupled to a radio frequency (RF) bias power source 222 through a matching network 224. The bias power source 222 is generally capable of producing an RF signal having a tunable frequency of from about 50 kHz to about 60 MHz, and a bias power of about 0 to about 5,000 Watts. The bias power source 222 may provide a signal at multiple frequencies, such as about 13.56 MHz and about 2 MHz. Optionally, the bias power source 222 may be a DC or pulsed DC source.

[0025] The temperature of the substrate 260 is at least partially controlled by regulating the temperature of the support pedestal 216. In one embodiment, the support pedestal 216 includes a cooling plate (not shown) having channels for flowing a coolant. In addition, a backside gas, such as helium (He) gas, provided from a gas source 248, fits provided into channels disposed between the back side of the substrate 260 and grooves (not shown) formed in the surface of the electrostatic chuck 226. The backside gas provides efficient heat transfer between the pedestal 216 and the substrate 260. The electrostatic chuck 226 may also include a resistive heater (not shown) disposed within the chuck 226 to heat the substrate 260 during processing. In one embodiment, the substrate 260 is maintained at a temperature of between about 10 to about 500 degrees Celsius.

[0026] A showerhead 232 is mounted to a lid 213 of the process chamber body 210 in a spaced-apart relation to the substrate pedestal 116 facing toward the substrate 260. A gas panel 238 is fluidly coupled to a plenum (not shown) defined between the showerhead 232 and the lid 213. The showerhead 232 includes a plurality of holes to allow gases provided to the plenum from the gas panel 238 to enter the process chamber body 210. The holes in the showerhead 232 may be arranged in different zones such that various gases can be released into the chamber body 210 with different volumetric flow rates.

[0027] The showerhead 232 and/or an upper electrode 228 positioned

proximate thereto is coupled to a RF plasma power source 218 through an impedance transformer 219 (*e.g.*, a quarter wavelength matching stub). The RF power source 218 is generally capable of producing an RF signal having a tunable frequency of about 50 kHz to about 160 MHz and a source power of about 0 to about 5,000 Watts. The RF plasma power source 218 may provide a signal at multiple frequencies, such as about 13.56 MHz or about 2 MHz.

[0028] The plasma etch system 202 may also include one or more coil segments or magnets 212 positioned exterior to the chamber wall 230, near the chamber lid 213. Power to the coil segment(s) 212 is controlled by a DC power source or a low-frequency AC power source 254.

[0029] During substrate processing, gas pressure within the interior of the chamber body 210 is controlled using the gas panel 238 and the throttle valve 227. In one embodiment, the gas pressure within the interior of the chamber body 210 is maintained at about 0.1 to about 999 mTorr.

[0030] A controller 240, including a central processing unit (CPU) 244, a memory 242, and support circuits 246, is coupled to the various components of the system 202 to facilitate control of the processes of the present invention. The memory 242 can be any computer-readable medium, such as random access memory (RAM), read only memory (ROM), floppy disk, hard disk, or any other form of digital storage, local or remote to the system 202 or CPU 244. The support circuits 246 are coupled to the CPU 244 for supporting the CPU 244 in a conventional manner. These circuits include cache, power supplies, clock circuits, input/output circuitry and subsystems, and the like. A software routine or a series of program instructions stored in the memory 242, when executed by the CPU 244, causes the plasma etch system 202 to perform an etch process of the present invention.

[0031] Figure 2 only shows one exemplary configuration of various types of plasma etching chambers that can be used to practice the invention. For example, different types of source power and bias power can be coupled into the plasma chamber using different coupling mechanisms. Using both the source power and the bias power allows independent control of a plasma density and a bias voltage of the substrate with respect to the plasma. In some applications, the source power may not be needed and the plasma is

maintained solely by the bias power. The plasma density can be enhanced by a magnetic field applied to the vacuum chamber using electromagnets, such as the magnets 212, driven with a low frequency (*e.g.*, 0.1-0.5 Hertz) AC current source or a DC source. In other applications, the plasma may be generated in a different chamber from the one in which the substrate is located, *e.g.*, remote plasma source, and subsequently guided into the chamber using techniques known in the art.

[0032] Figure 3 illustrates a flow diagram of a BARC removal process 300 suitable for use in a dual damascene fabrication process according to one embodiment of the invention. Figures 4A-4B are sequential schematic cross-sectional views illustrating different stages of process 300 illustrating the BARC removal process 300. The process 300 may be stored in memory 242 as instructions that when executed by the controller 240 cause the process 300 to be performed in the chamber 202.

[0033] The process 300 begins at step 302 by providing a substrate having a film stack suitable for fabricating a dual damascene structure. As shown in Figure 4A, the film stack has been etched to form a dual damascene structure 400 having a trench 422 over a via 420. The film stack includes a dielectric bulk insulating layer 410 disposed on a dielectric barrier layer 408 stacked on an underlying dielectric insulating layer 404. In embodiments the dielectric barrier layer 408 not present, the dielectric bulk insulating layer 410 may be directly disposed on the underlying dielectric insulating layer 404. The underlying dielectric insulating layer 404 is disposed on a substrate 402 and has at least a conductive layer 406, such as a copper line, embedded therein.

[0034] In one embodiment, the dielectric insulating layer 410 is a dielectric material having a dielectric constant less than 4.0, such as less than 3.5. Examples of suitable materials include carbon-doped silicon oxides (SiOC), such as BLACK DIAMOND® dielectric material available from Applied Materials, Inc., and other polymers, such as polyamides. The dielectric barrier layer 408 is selected from a material having a dielectric constant of about 5.5 or less. In one embodiment, the dielectric barrier layer 408 is a carbon containing silicon layer (SiC), a nitrogen doped carbon containing silicon layer (SiCN), or the like. For example, the dielectric barrier layer 408 may be a BLOK® dielectric material, available from Applied Materials Inc.

[0035] The trench 422 is formed in the dielectric insulating layer 410 is open through a patterned photoresist layer 412. A BARC layer 414 filling in the via 420 is exposed at the bottom of the trench 422. In one embodiment, the photoresist layer 412 may be conventional carbon-based, organic or polymeric materials used to pattern integrated circuit. The BARC 414 may extend from the via 420 to a height beyond a bottom surface 428 of the trench 422, thereby slightly protruding out of the via 420. The BARC layer 414 may comprise, for example, organic materials such as polyamides and polysulfide typically having hydrogen and carbon containing elements, or inorganic materials, such as silicon nitride, silicon oxynitride, silicon carbide, and the like. In the embodiment depicted in Figure 4A, the BARC layer 414 is an organic material spun-on the substrate 402. In another exemplary embodiment, the BARC layer 414 may be coated, deposited, or filled in the vias in any other suitable manner.

[0036] The patterned photoresist layer 412 transfers a predetermined pattern and/or feature in the dielectric insulating layer 410. During the process of predetermined pattern and/or feature formation, the patterned photoresist layer 412 may be consumed or trimmed, leaving a portion of the patterned photoresist layer 412 on the upper surface 416 of the dielectric insulating layer 410. Alternatively, the patterned photoresist layer 412 may be substantially removed, thereby exposing the upper surface 416 of the dielectric insulating layer 410. In embodiments depicted in Figure 4A, a portion of the patterned photoresist layer 412 is remained on the dual damascene structure 400 after predetermined pattern and/or feature are transferred in the dielectric insulating

layer 410 to for the trench 422. In embodiments that the photoresist layer 412 is not present, the two step etching process may be performed to remove the BARC layer 414 remained in the vias 420.

[0037] At step 304, a first etching step is performed to initially etch a portion of the BARC layer 414 filling the via 420 and exposed through the trench 422 by supplying a first gas mixture in the etching chamber 202. If a portion of the patterned photoresist layer 412 may be remained on the substrate surface, the first BARC etching step may also etch the patterned photoresist layer 412.

[0038] In one embodiment, the first gas mixture supplied into the etching chamber 202 contains ammonia gas (NH_3). The first gas mixture is used to remove organic polymers and photoresist crust that may be generated from the previous etching processes and/or present on the substrate surface. The hydrogen element in the first gas mixture cleans the organic residues by forming volatile hydrogen carbon compounds which are pumped out of the etching system 202 without damaging the substrate surface. The first gas mixture may also passivate the sidewall 426 or exposed surface 428 of the dielectric insulating layer 410, thereby preventing the underlying low-k dielectric substrate from k value shift and dielectric constant increase. The first gas mixture may also purge and flush out the residual gas, *e.g.*, fluorine containing gas, from the previous etching process remaining in the etching chamber 202, thereby preventing defect generation or chemical reaction with residual fluorine chemistry which may further attack dielectric insulating layer surface.

[0039] In one embodiment, the BARC layer 414 and/or the patterned photoresist layer 412 is first etched by forming a plasma from the first gas mixture containing NH_3 gas. The BARC layer 414 and/or the patterned photoresist layer 412 may be etched in an etch chamber, such as the etching chamber 202 described in Figure 2, or in other suitable reactors.

[0040] Several process parameters are regulated at step 304 while the first gas mixture is supplied into the etching system 202. In one embodiment, a pressure of the gas mixture in the etch reactor is regulated between about 5 mTorr to about 300 mTorr, and the substrate temperature is maintained between about -10 degrees Celsius and about 55 degrees Celsius. RF source power may be applied at a power of about 150 Watts to about 2000 Watts. The

NH_3 gas may be flowed at a flow rate between about 50 sccm and about 1000 sccm, such as about 100 sccm and about 800 sccm. Other inert gas, such as N_2, Ar, He gas, may be flowed and supplied in the first gas mixture at a flow rate between about 50 sccm to about 1000 sccm.

[0041] In one embodiment, the first etching step may be terminated by expiration of a predefined time period. For example, the first etching step is terminated by processing between about 20 seconds to about 200 seconds. In another embodiment, the first BARC etching step may be terminated by other suitable method, for example, by monitoring optical emission or by other indicator.

[0042] At step 306, a second etching step is performed to etch and remove the remaining portion of the BARC layer 414 filling the via 402. The second step 306 also removes any patterned photoresist layer 412 remaining on the upper surface 416 of the dielectric insulating layer 410. The second etching step is performed using a second gas mixture supplied into the etching chamber 202. In one embodiment, the second gas mixture includes O_2 gas. The second gas mixture containing O_2 gas forms volatile polymers with the residuals and byproducts from the first etching step 304 and reacts with the remaining BARC 414 and photoresist layer 412 on the substrate 402, thereby efficiently removing the residuals, byproducts, remaining BARC 414 and photoresist layer 412 from the substrate 402 out of the etching system 202. The oxygen element in the second gas mixture provides a high etching rate and polymer removal rate that not only advantageously promotes removal of the residuals and contaminants but also cleans away the residuals and byproducts that may not be completely removed during the first etching process.

[0043] In one embodiment, the BARC layer 414 and/or the photoresist layer 412 is etched by forming a plasma from the second gas mixture containing O_2. The BARC layer and/or the photoresist layer 412 may be etched in an etch system, such as the etch system 202 described in Figure 2, or in other suitable reactors.

[0044] Several process parameters are regulated at step 306 while the second gas mixture is supplied into the system 202. In one embodiment, a pressure of the gas mixture in the etch reactor is regulated between about 5

mTorr to about 50 mTorr, and the substrate temperature is maintained between about -10 degrees Celsius and about 55 degrees Celsius. RF source power may be applied at a power of about 150 Watts to about 2000 Watts. The O_2 gas may be flowed at a flow rate between about 50 sccm to about 500 sccm. The etching time may be processed at between about 20 seconds and about 200 seconds, such as between about 10 seconds to about 60 seconds.

[0045] The second etching step 306 is terminated by expiration of a predefined time period. For example, the second BARC etching step may be terminated by processing between about 10 seconds to about 60 seconds. In one embodiment, the second etching step 306 may also be configured to have a process time substantially equal to the first etching step 304, as described above. Alternatively, the process time of the first etching step 304 and the second etching step 306 may be configured to have a time period ratio between about 1:1 to about 4:1. In another embodiment, the second etching step 306 is terminated by monitoring optical emissions or by other indicator that indicates that the BARC layer 414 and/or the photoresist layer 412 has been completely removed from the substrate 402 or the upper surface 416 of the dielectric insulating layer 410 and a bottom surface 418 in the via 420 has been exposed, as shown in Figure 4B.

[0046] Since the sidewall and surface of the dielectric insulating layer 410 are passivated and protected by the polymer formed from exposure to the first gas mixture at step 304, the second gas mixture 306 mainly etches the residuals, byproducts, and the remaining BARC layer 414 and/or the photoresist layer 412 disposed on the substrate without adversely affecting or etching the underlying structures on the substrate, such as the dielectric insulating layer 410. Furthermore, as the second gas mixture provided at the second etching step 306 reacts mainly with the BARC layer 414 and/or the photoresist layer 412, the second etching step 306 advantageously and efficiently removes both organic and/or inorganic materials from the substrate.

[0047] The two step etching process as described at step 304 and step 306 may be repeatedly and consecutively performed on the substrate as indicated by the loop 308 depicted in Figure 3. Alternatively, the two steps etching process described at step 304 and step 306 may be performed in the reverse

order. For example, the etching step as described at step 306 may be performed first, then followed the etching process as described at step 304.

[0048] The dual damascene structure 400 as depicted in Figure 4 only shows an exemplary embodiment that may be utilized to perform the two step etching process as described in the present invention. Other structures, such as single damascene structure, via only structure, trench-first structure, and the like, having a BARC layer disposed thereon may also be utilized to perform the two step etching process as described above. The method may also be utilized to etch BARC layer found in other substrates.

[0049] Thus, the present invention provides a two step etching method for etching a BARC layer with high removal rate and clean efficiency. The method advantageously facilitates removal of the BARC layer, photoresist layer, and associated residuals and byproducts from trenches and/or vias in a dual damascene structure without adversely damage underlying dielectric materials disposed on the substrate. The two step etching process also provides good sidewall and/or surface protection.

[0050] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method for removing a BARC layer from a feature formed in a dual damascene structure, comprising:

providing a substrate having a feature filled with a BARC layer in an etching chamber, wherein the feature includes a trench connected to a via defined in a dielectric bulk insulating layer, wherein the BARC layer is an organic material filled within the via;

supplying a first gas mixture comprising NH_3 gas into the chamber to etch a first portion of the BARC layer filling in the feature while providing sidewall protection of the dielectric bulk insulating layer; and

supplying a second gas mixture comprising O_2 gas into the etching chamber to etch the remaining portion of the BARC layer disposed in the feature, wherein a process time for etching the portion of the BARC layer in the presence of the first gas mixture relative to a process time for etching the remaining portion of the BARC layer has a ratio of between about 1:1 and about 4:1.

2. The method of claim 1, wherein the step of supplying the first gas mixture further comprises:

flowing NH_3 into the etching chamber having at a flow rate between 50 sccm and 1000 sccm.

3. The method of claim 1, wherein the step of supplying the first gas mixture further comprises:

maintaining a process pressure at between about 5 mTorr to about 300 mTorr.

4. The method of claim 1, wherein the step of supplying the first gas mixture further comprises:

controlling substrate temperature between about -10 degrees Celsius to about 55 degrees Celsius.

5. The method of claim 1, wherein the step of supplying the first gas mixture further comprises:

applying a plasma power at between about 150 Watts to about 2000 Watts.

6. The method of claim 1, wherein the step of supplying the first gas mixture further comprises:

etching the first portion of the BARC layer filling in the features at a process time between about 20 seconds and about 200 seconds.

7. The method of claim 1, wherein the step of supplying the second gas mixture further comprises:

flowing O_2 gas into the etching chamber at a flow rate between 50 sccm and 500 sccm.

8. The method of claim 1, wherein the step of supplying the second gas mixture further comprises:

maintaining a process pressure at between about 5 mTorr to about 50 mTorr.

9. The method of claim 1, wherein the step of supplying the second gas mixture further comprises:

controlling substrate temperature between about -10 degrees Celsius to about 55 degrees Celsius.

10. The method of claim 1, wherein the step of supplying the second gas mixture further comprises:

applying a plasma power at between about 150 Watts to about 2000 Watts.

11. The method of claim 1, wherein the step of supplying the second gas mixture further comprises:

etching the remaining portion of the BARC layer filling in the features at a process time between about 10 seconds and about 60 seconds.

12. The method of claim 1, wherein the damascene structure includes a dielectric insulating layer having a dielectric constant less than 3.5.

13. The method of claim 1, wherein the damascene structure includes a dielectric insulating layer comprising carbon doped silicon oxide.

14. The method of claim 1, wherein the step of providing further comprises:

providing the substrate having a photoresist layer disposed on an upper surface of the substrate.

15. The method of claim 14, wherein the first gas mixture and the second gas mixture supplied into the etching chamber etch the photoresist layer while etching the BARC layer.

16. A method for removing a BARC layer from a feature, comprising:

providing a substrate having a via formed in a dual damascene structure in an etch chamber, wherein the via is formed in a dielectric insulating layer under a trench and filled with a BARC layer, the BARC layer comprising an organic material;

supplying a first gas mixture comprising NH_3 into the chamber to etch a portion of the BARC layer filling in the via while providing sidewall protection of the dielectric insulating layer; and

supplying a second gas mixture comprising O_2 gas into the chamber to etch the remaining portion of the BARC layer in the via, wherein a process time for etching the portion of the BARC layer in the presence of the first gas mixture relative to a process time for etching the remaining portion of the BARC layer has a ratio of between about 1:1 and about 4:1.

17. The method of claim 16, wherein the step of supplying the first gas mixture further comprising:

flowing the NH_3 gas at a rate between about 50 sccm to about 1000 sccm.

18. The method of claim 16, wherein the step of supplying the second gas mixture further comprising:

flowing the O_2 gas at a rate between about 50 sccm to about 500 sccm.

19. The method of claim 16, wherein the dielectric insulating layer has a dielectric constant less than 3.5.

20. A method for removing a BARC layer from a feature, comprising:

providing a substrate having a via formed within a dielectric insulating layer in a dual damascene structure and filled with a BARC layer in an etch chamber, wherein the dielectric insulating layer has a dielectric constant less than 3.5, the BARC layer comprising an organic material;

supplying a first gas mixture having NH_3 gas at between about 50 sccm and about 1000 sccm into the etch chamber to etch a portion of the BARC layer filling in the via while providing sidewall protection of the dielectric insulating layer; and

supplying a second gas mixture comprising O_2 gas at between about 50 sccm and about 500 sccm into the etch chamber to etch the remaining portion of the BARC layer in the via, wherein a process time for etching the portion of the BARC layer in the presence of the first gas mixture relative to a process time for etching the remaining portion of the BARC layer has a ratio of between about 1:1 and about 4:1.