

“Improvements In Or Relating To Silicidation Techniques”

This invention relates to silicidation and more particularly to the formation of silicides on semiconductor devices.

Self-aligned silicides have been a key component of high performance CMOS devices for several technology nodes. They provide low sheet resistance on gate, source, and drain areas (minimising RC delays) to allow for high speed device operation. In addition, silicides constitute stable, low-resistance contacting structures, helping to minimise source/drain series resistance and optimising device performance.

TiSi₂ silicide has been the most prevalently used silicide for CMOS technology. In the TiSi₂ silicide process, a deposited Ti film is thermally reacted at a relatively low temperature in a N₂ ambient atmosphere to form TiSi₂ on the exposed Si areas. A high resistivity C49 phase (60-90 μΩ.cm) forms first. Any unreacted TiN or Ti remaining on the insulating areas (covered by either SiO₂ or SiN_x) are then etched away, and followed by a higher temperature second step anneal to transform the TiSi₂ from the C49 phase to a low resistance (13-16 μΩ.cm) C54 phase. During the first step, the temperature is kept at around 650 - 700°C. The second step anneal is carried out at a temperature of 850°C or above to obtain the low resistivity C54 phase. It should be noted that C54 phase TiSi₂ formation is suppressed on heavily As doped n⁺ polycrystalline silicon (poly-Si) and n⁺ source/drain regions, thus a second step anneal at 850°C or above is required.

The major drawback of TiSi₂ silicide is the so-called “narrow-line” effect. The sheet resistance of TiSi₂ silicide increases with decreasing poly-silicon line

width. This is because the C49-to-C54 phase transformation does not occur so readily for narrower polycrystalline silicon lines. Considerable increases in sheet resistance occur when the widths of polycrystalline silicon lines are narrower than $0.35\mu\text{m}$. So a process is required to facilitate C54 phase transformation even in ultra narrow lines, i.e. lines of less than $0.25\mu\text{m}$ width. Successful implementation of such a process for use with ultra narrow lines allows the industry to continue using TiSi_2 which has been in use since the early eighties.

To overcome the narrow-line effect of TiSi_2 silicide, numerous approaches have been proposed: (1) using TiN capping, (2) using a pre-amorphisation implant (PAI), (3) using a Mo implant before the TiSi_2 silicon is formed, and (4) using a combination of Mo and PAI implants.

The TiN capping process is relatively simple and the effectiveness of the process has been demonstrated on $0.35\mu\text{m}$ line width technology. For devices having a line width of $0.25\mu\text{m}$ or less, this process is not effective.

Using a pre-amorphisation implant (PAI) before Ti deposition to ameliorate the narrow-line effect has been widely studied. It has been found that, with PAI the sheet resistance of TiSi_2 is nearly constant down to gate widths of approximately $0.1\mu\text{m}$ for n^+ poly-Si gate. For gate widths narrower than $0.1\mu\text{m}$, however, considerable increase in sheet resistance has been observed. High leakage in source/drain junctions and transient enhanced diffusion (TED) of boron are also major concerns for the application of this process for ultra shallow devices, i.e. devices having source/drain junction depths of less than $0.1\mu\text{m}$.

Molybdenum (Mo) doping in the polycrystalline or crystalline Si has also proved effective in alleviating the narrow-line effect. The Mo doping process reasonably well ameliorates the narrow-line effect (down to $0.12\mu\text{m}$ for n^+ poly-Si gate and $0.1\mu\text{m}$ for p^+ poly-Si gate) without many drawbacks. Like the PAI process, this process begins to lose its effectiveness when gate widths become narrower than $0.1\mu\text{m}$.

It has been demonstrated that, when PAI is combined with Mo doping, a one-step rapid thermal process (RTP) of annealing at a temperature as low as 650°C can achieve low sheet resistance with no significant increase in resistance for line widths down to approximately $0.07\mu\text{m}$.

An adverse effect of the PAI Ti-silicide process (also for the Mo doping and PAI combination processes) is the introduction of implant-induced defects in source/drain junction regions. Although the pre-amorphised layer, and thus most implant damage, is consumed by the silicide film after silicidation, implant induced-residual defects can still form in the silicon. This is due to the fact that self-interstitial as well as many interstitial type impurities are fast diffusing species in silicon and can therefore diffuse into deep bulk regions and form defects during the silicidation process. The presence of these implant induced defects can have detrimental effects on device performance. For example, implant induced electrically active defects, in particular deep level defects, may cause high leakage in source/drain junctions while self-interstitial emission from implant induced interstitial type complexes or extended defects may contribute to transient enhanced diffusion of dopant, increasing junction depths.

Accordingly, one aspect of the present invention provides a method of forming TiSi_2 on a silicon substrate comprising the steps of: providing a layer of Si; providing a layer of Ti in contact with the layer of Si; annealing the layers at a temperature of 700°C to 770°C to promote silicidation.

Advantageously, the TiSi_2 is formed on the silicon substrate in a layer.

Preferably, the annealing step is performed after a low temperature RTP silicidation, in which the temperature ranges from 600°C to 700°C .

Conveniently, the layer of Ti is deposited by one of the following means: sputtering, filament evaporation, electron beam evaporation and chemical vapour deposition.

A further aspect of the present invention provides a method of forming TiSi_2 on a silicon substrate comprising the steps of: providing an amorphised layer of Si in at least one of a source/drain and gate region of a CMOS device using plasma ion implantation; providing a layer of Ti in contact with the amorphised layer of Si; and annealing the layers.

Another aspect of the present invention provides a method of forming TiSi_2 on a silicon substrate comprising the steps of: providing a raised source/drain region using silicon ion plasma implantation; providing a layer of Ti in contact with the amorphised layer of Si; and annealing the layers.

Advantageously, the TiSi_2 is formed on the silicon substrate in a layer.

Preferably, said plasma ion implantation is performed by introducing into a vacuum chamber; a gas consisting of at least one or any combination of: SiH_4 ,

Si_2H_6 , SiF_4 , GeH_4 , GeF_4 , and the inert gases, generating a plasma to create at least one of the group consisting of the ions of: Si, Ge, and the inert gases; and accelerating the ions to implant into the silicon substrate.

Another aspect of the present invention provides a semiconductor device incorporating a TiSi_2 layer formed by annealing at a temperature of between 700°C and 770°C .

A further aspect of the present invention provides a semiconductor device incorporating a TiSi_2 layer and a raised source/drain region formed by silicon ion plasma implantation.

Conveniently, said raised source/drain region is made by plasma ion implant of the source/drain region with silicon ions at a dose of 5×10^{16} to $1 \times 10^{18} \text{cm}^{-2}$.

Advantageously, a sacrificial layer is provided in the areas other than the source/drain region to absorb implanted silicon ions.

Preferably, the sacrificial layer is removed after silicon ion implantation.

Conveniently, the layers are annealed at a temperature in the range of 700°C to 770°C .

In order that the present invention may be more readily understood, it will now be described, by way of example, with reference to the accompanying drawings, in which:

Figures 1(1) to (4) are schematic cross-sections of a semiconductor device at different stages of a method embodying the present invention;

Figure 2 is a schematic view of an ion implant system for use with the claimed invention; and

Figure 3 illustrates schematically the process for fabricating raised source and drain structures using Si-ion plasma implantation.

In accordance with an embodiment of the present invention and referring to Figure 1 (1), a silicon wafer substrate having source/drain and gate regions amorphized by ion implantation. A Ti film is deposited on the substrate 1 as shown in Figure 1(2). A silicidation process involves the substrate 1 and Ti film 2 being annealed in a N_2 atmosphere to form regions of $TiSi_2$ as shown in Figure 1(3). Subsequently unreacted Ti film is etched off, as shown in Figure 1(4). Preferably, a conventional pre-amorphisation implant (PAI) has been performed before the Ti film is deposited although a conventional pre-amorphisation implant through the Ti film (ITM) after deposition and before annealing is also possible. The annealing conditions are discussed below.

The inventors have shown that, if PAI using a conventional ion beam current implant is used in the Ti silicidation process which typically results in 30nm thickness amorphized surface layer, an RTP silicidation at temperatures $\leq 700^\circ C$ is not enough to remove implant induced defects although the pre-amorphised layer is indeed consumed by the already formed silicide films. High concentrations of defects are observed in the near interface regions. The electronic states associated with these defects are located close to the mid-gap of the silicon bandgap, implying that they are effective recombination/generation centres for leakage currents in source/drain junctions. In addition, detailed analyses suggest that the capture cross-sections of some of the defects are much larger than those expected for point defects. This means that these defects are extended type defects (interstitial clusters, $\{311\}$ rod-like

defects, or dislocations). Since extended defects provide additional paths for leakage current in source/drain junctions, higher leakage currents are expected for the source/drain junctions silicided at temperatures of $\leq 700^{\circ}\text{C}$ in PAI or PAI + Mo combination Ti-silicidation processes.

For RTP silicidation temperatures of 800°C or higher, a considerable transient enhanced diffusion (TED) of dopants (in the presence of implant induced excess self-interstitials) as well as a severe agglomeration of thin silicide films takes place. Thus, it is concluded that, for single step RTP Ti-silicidation for Mo or other doping and pre-amorphization combined schemes, ideal RTP silicidation temperatures are within the range of $700\text{--}770^{\circ}\text{C}$ which not only results in low defects but also minimises other adverse effects such as TED and agglomeration, thus making it possible for obtaining high performance devices with enhanced reliability.

If low temperature RTP silicidation (600°C to 700°C) is applied to avoid bridging between source/drain and gate, a higher temperature (around 770°C) second step RTP is performed to anneal out the implant induced damage. Similar RTP silicidation within the critical temperature range of 700°C to 770°C can also minimise the defects even in the absence of Mo or other dopants.

Another aspect of the present invention relates to the fabrication of devices comprising of ultra shallow source/drain junctions with super steep dopant profiles. For such devices, the temperature range of 700°C to 770°C is still high enough to cause a considerable TED of boron. To avoid TED of boron without having an unacceptable level of implant induced defects, the lower limit of the processing window, i.e. the RTP temperature range, must be reduced further to in the region of 650°C to 700°C . To do this, the amorphised layer thickness as well as the pre-amorphisation implant dose must be reduced

provided that the reduction in the amorphised layer thickness does not reduce its ability to facilitate the transformation of TiSi_2 from C49 to C54.

The reduction in the pre-amorphised layer thickness can be achieved by reducing the implant ion energy. However, for a conventional PAI process, which employs ion beam current implant techniques, it is difficult to further reduce implant ion energy due to difficulties in controlling beam current for low energy ions, especially when a medium (around 1-2mA) or high beam current (around 5-30mA) implantor is used for pre-amorphisation. Thus, the choice of the amorphised layer with a $\approx 30\text{nm}$ thickness (a typical thickness of amorphised layer in PAI Ti-silicidation process) is not because this is thought to be an optimised thickness, but because of practical considerations in the use of the beam current implantor.

A method that is proposed by the inventors to reduce and thereby optimise the pre-amorphised layer thickness is the use of plasma immersion ion implantation instead of conventional ion beam current implantation. The principles of the process are illustrated in Figure 2. An example of a plasma immersion ion implantor 4 comprises an ion generating chamber 5 and an ion accelerating chamber 6. The two chambers are separated by a metal grid 7 formed with holes. During plasma ion implantation, a gas comprising one or any combination of the following gases: SiH_4 , Si_2H_6 , SiF_4 , GeF_4 , GeH_4 and the inert gases such as Ar, is introduced into the ion generating chamber from a gas supply 8. RF plasma is generated by applying RF bias between cathode and anode electrodes 9 inside the ion generating chamber 5. Ions, such as Ar^+ , Si^+ , and Ge^+ , are extracted from the ion generating chamber 5 into the accelerating chamber 6 through the holes in the metal grid 7 and then accelerated towards a silicon substrate 1 by a DC bias applied between the metal grid and the silicon substrate. The ions are eventually implanted into the silicon substrate 1 at an

energy of about the applied DC bias value (in terms of electron volts), for example, in the region of 5KeV. When the number of implanted ions exceeds a certain critical value, an amorphised layer is formed on the silicon substrate surface. The thickness of the amorphised layer mainly depends on the ion energy, which is controlled by the DC bias applied between the metal grid and silicon substrate. By applying a few KV (e.g. 1-5KeV) DC bias (in the case of Si⁺), an amorphised layer with a thickness of much less than 30nm (a typical value for conventional ion beam current pre-amorphisation implantation) is formed.

For a raised source and drain which requires Si deposition a Si-containing gas must be used. In this case, the gas can also be supplemented with an inert gas, but not essentially.

The benefits of using plasma immersion ion implantation for pre-amorphisation Ti-silicide process include:

1. Flexibility in ion energy control (from a few hundred eV (500eV) to a few KeV (20KeV). This is because, in plasma immersion ion implantation, there is no need to focus the ion beam as required in the case of conventional beam current implantation, thus allowing for low energy ion implantation and consequently reduced amorphised layer thickness (e.g. 10nm) and also reduction in pre-amorphisation implant dose (due to the reduction in the amorphised layer thickness);
2. The reduction in ion energy (thus reduction in the amorphised layer thickness) and implant dose will result in a reduction in the concentration of excess self-interstitials in Si (the former facilitates excess self-interstitials through surface/interface recombination due to short distance to

surface/interface; the latter on the other hand means that less excess self-interstitials are introduced in the first place) and a consequential reduction in the thermal budget (i.e. temperature) required to anneal implant induced defects (self-interstitial related). Thus, the processing temperature is considerably reduced without causing problems for C54 phase formation. This is a substantial advantage for the fabrication of ultra shallow junction with super steep dopant profiles due to reduced TED;

3. The high ion flux, which can be obtained by inputting high RF power into the ion generating chamber in the example given above, means that the pre-amorphisation process can be done in a much shorter time using less expensive equipment, thus reducing processing costs; and

4. The high ion flux in plasma ion implantation can also be used for raised source/drain processes for Ti-silicidation. This can be done by pre-amorphising the silicon surface using low energy ions at a high implant dose. For example, a low energy (1-5 KeV) Si⁺ ion implant at a dose of $1 \times 10^{17} \text{ cm}^{-2}$ can raise the source/drain regions by about 20nm, which can significantly reduce the constraints on the silicide film for the use of Ti-silicide to ultra shallow junctions. For the application of plasma ion implantation to a raised source/drain with a pre-amorphised layer scheme, a sacrificial layer (e.g. photo-resist) should be coated over the insulating regions of the silicon substrate (SiO₂ or SiN_x) as shown in Figure 3.

The proposed processes not only address the narrow-line effect of TiSi₂ silicide, but also assure the minimisation of process induced defects in source/drain regions of crystalline silicon wafers. Compared to conventional PAI Ti-silicide processes, the thermal budget for the second RTP is significantly reduced (from 850°C to around 770°C or less). In the case that plasma ion implant using low

ion energy is used, the thermal budget can be further reduced (650°C - 700°C), which is preferable for the fabrication of devices with ultra shallow junctions due to minimization of defects and reduced TED of dopant.

The silicidation process to minimise defect formation and make better devices is applicable irrespective of whether the ions used for the pre-amorphisation implant are the heavier ions, e.g., As, Ge, Sb, or Si, or inert gases.

The effectiveness of this process in eliminating implantation induced defects has been clearly demonstrated by deep level transient spectroscopy characterisation of pre-amorphised silicon wafer (pre-amorphised using silicon ions).

Other implant ions such as As, Ge, and Sb can also be used for pre-amorphisation in combination with Mo implant doping.

Ta, Nb, or W etc. can also be used in place of Mo in combination with pre-amorphisation implants.

In the present specification "comprises" means "includes or consists of" and "comprising" means "including or consisting of".

The features disclosed in the foregoing description, or the following claims, or the accompanying drawings, expressed in their specific forms or in terms of a means for performing the disclosed function, or a method or process for attaining the disclosed result, as appropriate, may, separately, or in any combination of such features, be utilised for realising the invention in diverse forms thereof.



CLAIMS

1. A method of forming TiSi_2 on a silicon substrate comprising the steps of:
 - providing a layer of Si;
 - providing a layer of Ti in contact with the layer of Si;
 - annealing the layers at a temperature of 700°C to 770°C to promote silicidation.
2. A method according to Claim 1, wherein the TiSi_2 is formed on the silicon substrate in a layer.
3. A method according to Claim 1 or 2, wherein the annealing step is performed after a low temperature RTP silicidation, in which the temperature ranges from 600°C to 700°C .
4. A method according to any preceding claim, wherein the layer of Ti is deposited by one of the following means: sputtering, filament evaporation, electron beam evaporation and chemical vapour deposition.
5. A method of forming TiSi_2 on a silicon substrate comprising the steps of:
 - providing an amorphised layer of Si in at least one of a source/drain and gate region of a CMOS device using plasma ion implantation;
 - providing a layer of Ti in contact with the amorphised layer of Si; and
 - annealing the layers.



6. A method of forming TiSi_2 on a silicon substrate comprising the steps of:
 - providing a raised source/drain region using silicon ion plasma implantation;
 - providing a layer of Ti in contact with the amorphised layer of Si; and
 - annealing the layers.
7. A method according to Claim 6, wherein said raised source/drain region is made by plasma ion implant of the source/drain region with silicon ions at a dose of 5×10^{16} to $1 \times 10^{18} \text{cm}^{-2}$.
8. A method according to any one of Claims 5 to 7, wherein the TiSi_2 is formed on the silicon substrate in a layer.
9. A method according to any one of Claims 5 to 8, wherein said plasma ion implantation is performed by introducing into a vacuum chamber; a gas consisting of at least one or any combination of: SiH_4 , Si_2H_6 , SiF_4 , GeH_4 , GeF_4 , and the inert gases, generating a plasma to create at least one of the group consisting of the ions of: Si, Ge, and the inert gases; and accelerating the ions to implant into the silicon substrate.
10. A method according to any one of Claims 5 to 9, wherein a sacrificial layer is provided in the areas other than the source/drain region to absorb implanted silicon ions.
11. A method according to Claim 10, wherein the sacrificial layer is removed after silicon ion implantation.



12. A method according to any one of Claims 5 to 11, wherein the layers are annealed at a temperature in the range of 700°C to 770°C.
13. A semiconductor device incorporating a TiSi_2 layer formed by annealing at a temperature of between 700°C and 770°C.
14. A semiconductor device incorporating a TiSi_2 layer and a raised source/drain region formed by silicon ion plasma implantation.