

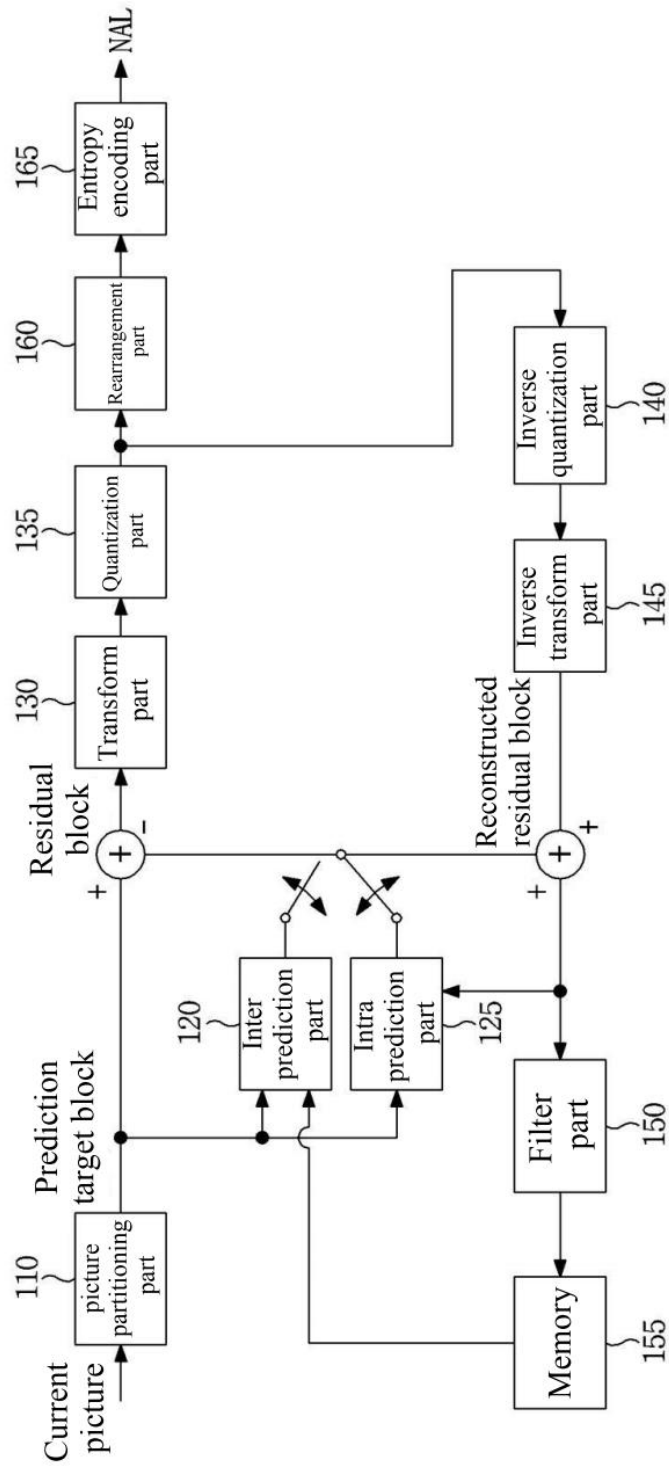


Fig. 1

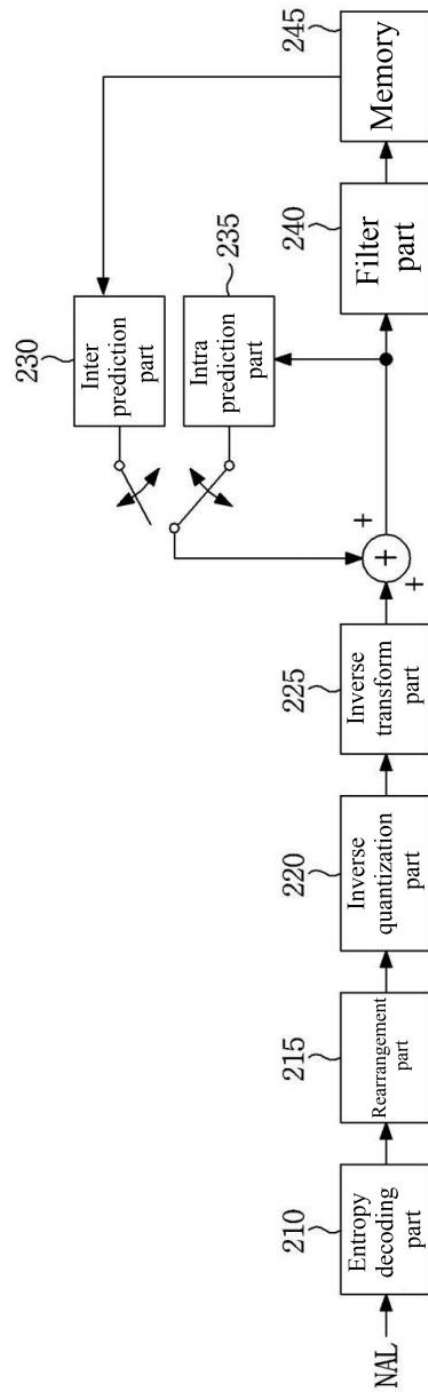


Fig. 2

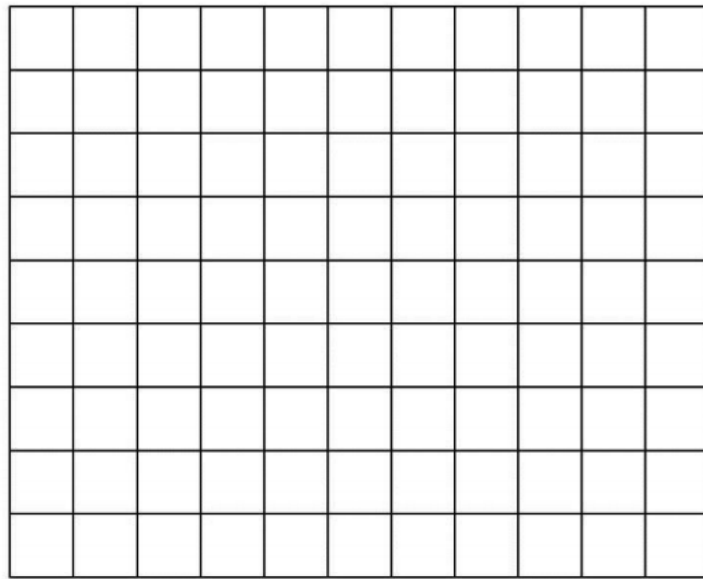


Fig. 3

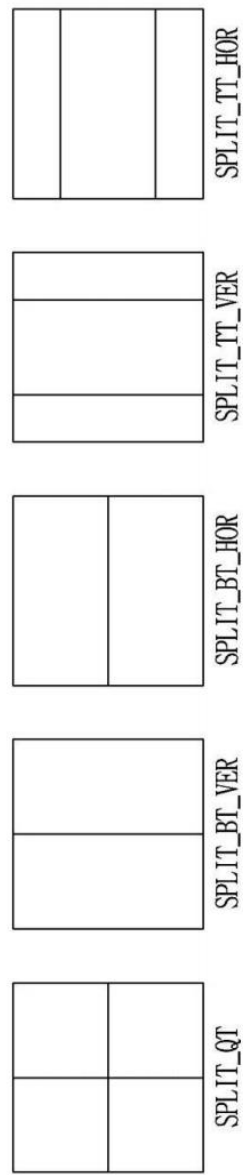


Fig. 4

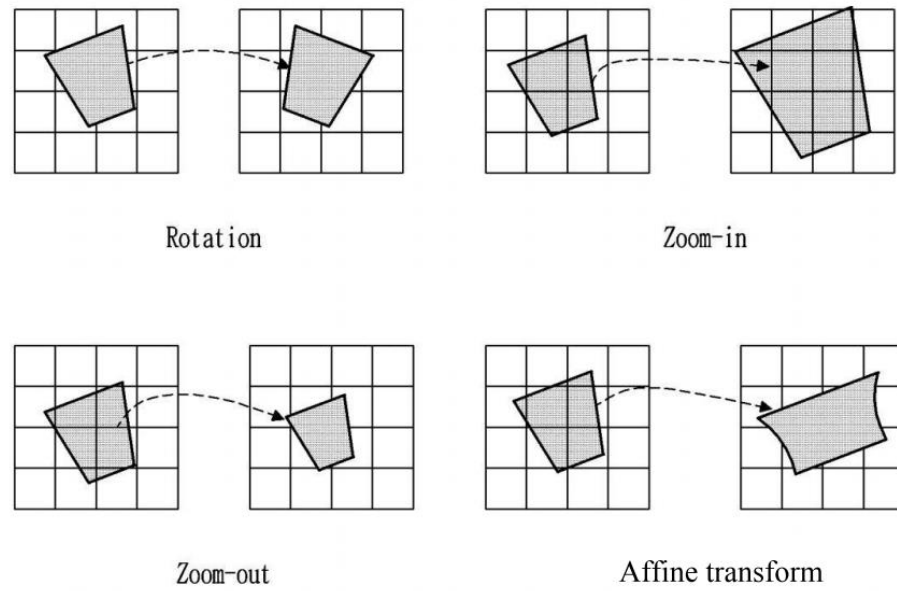


Fig. 7

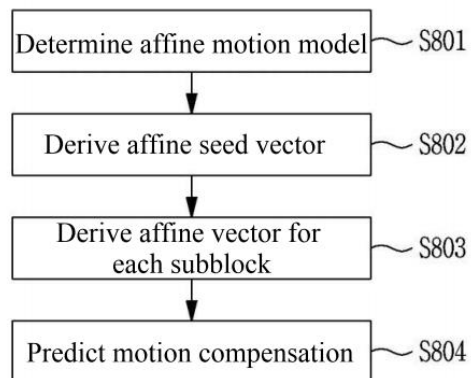


Fig. 8

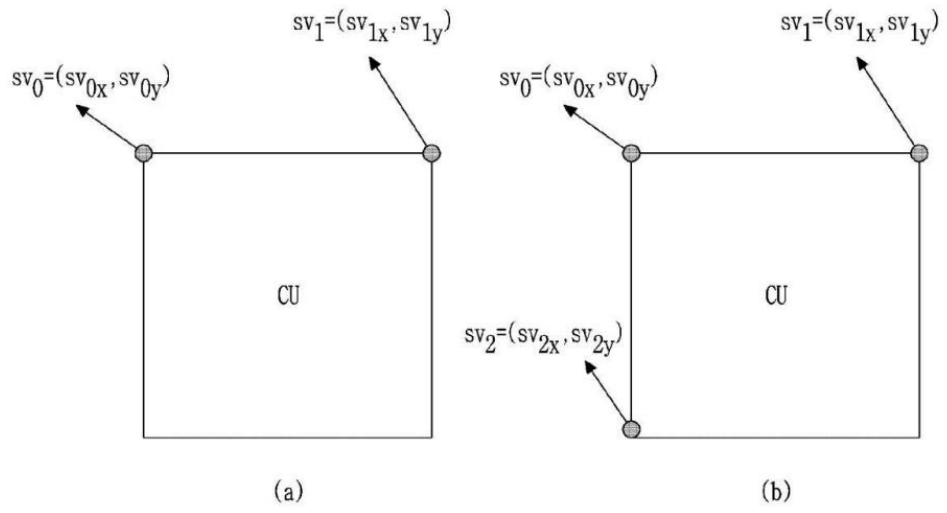


Fig. 9

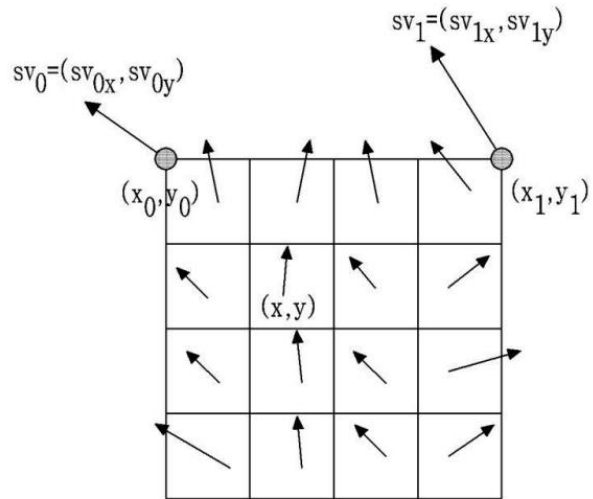


Fig. 10

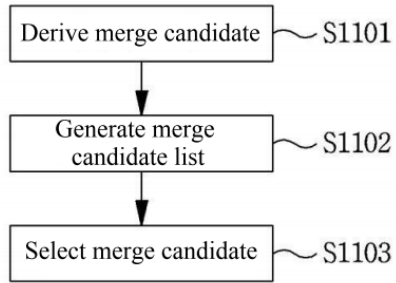


Fig. 11

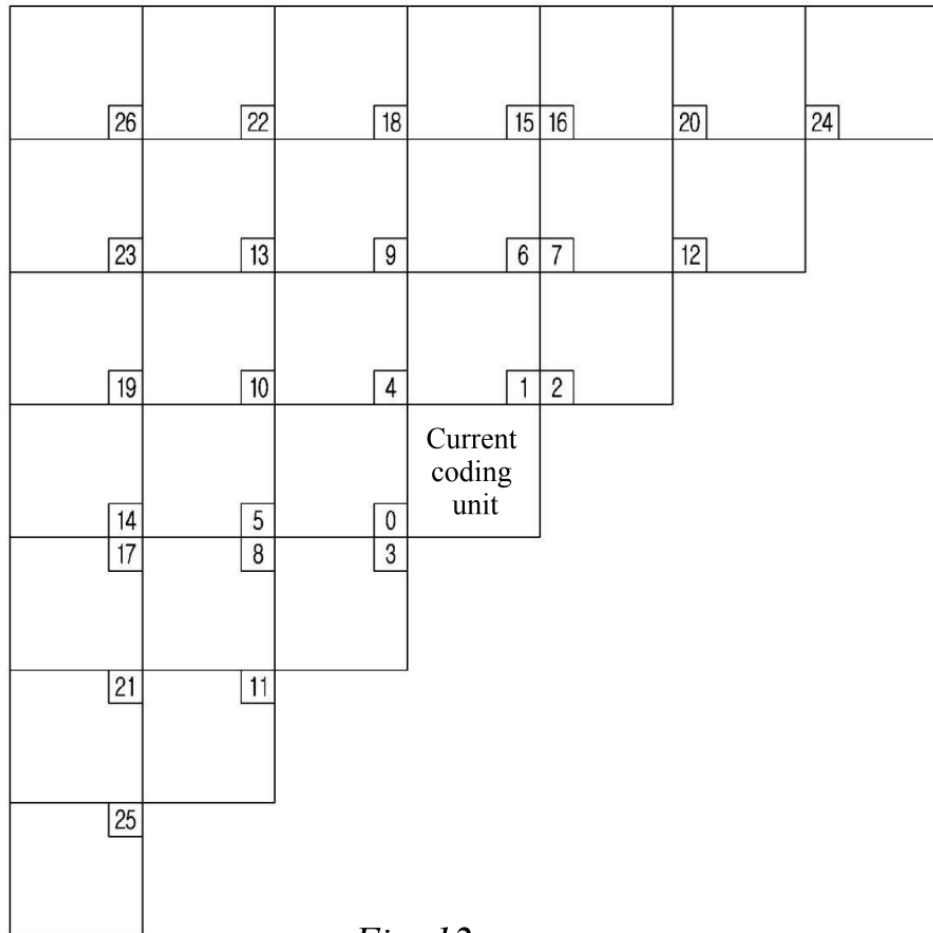


Fig. 12

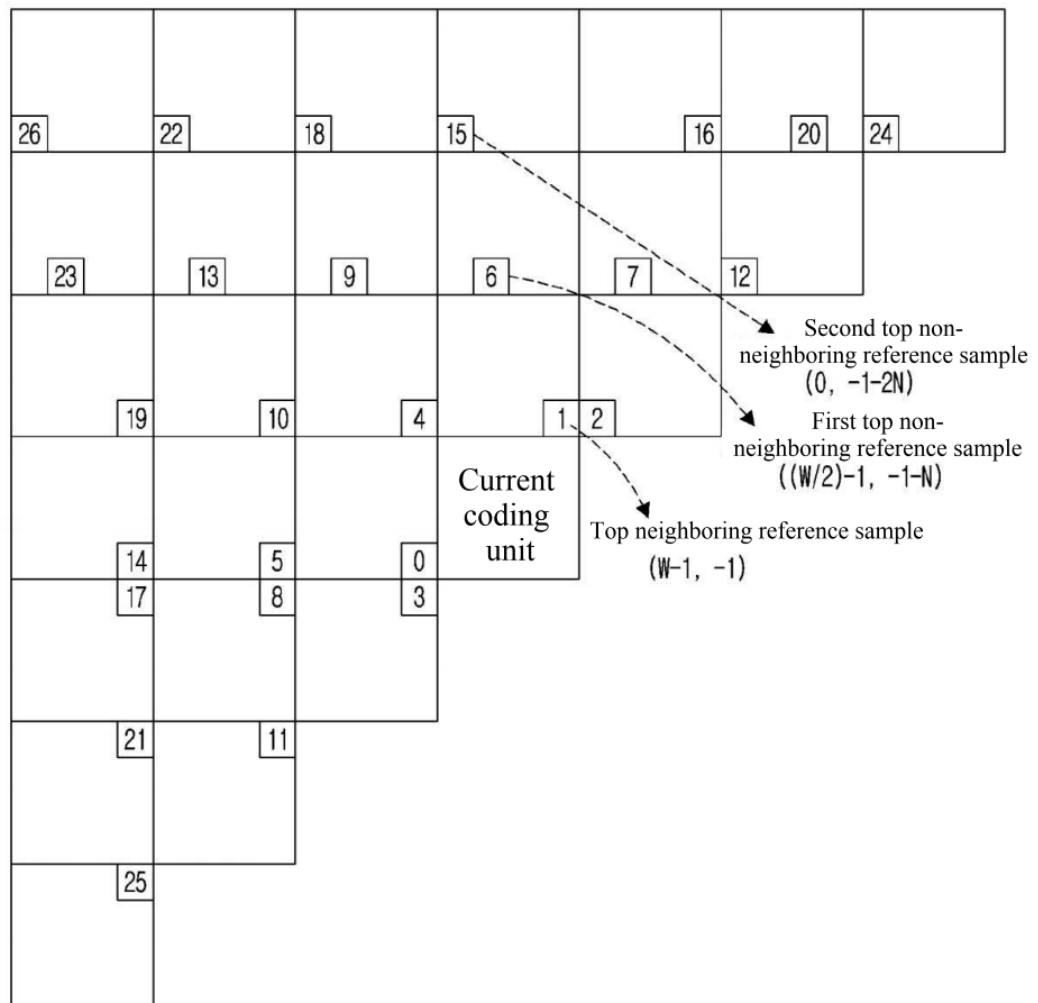


Fig. 13

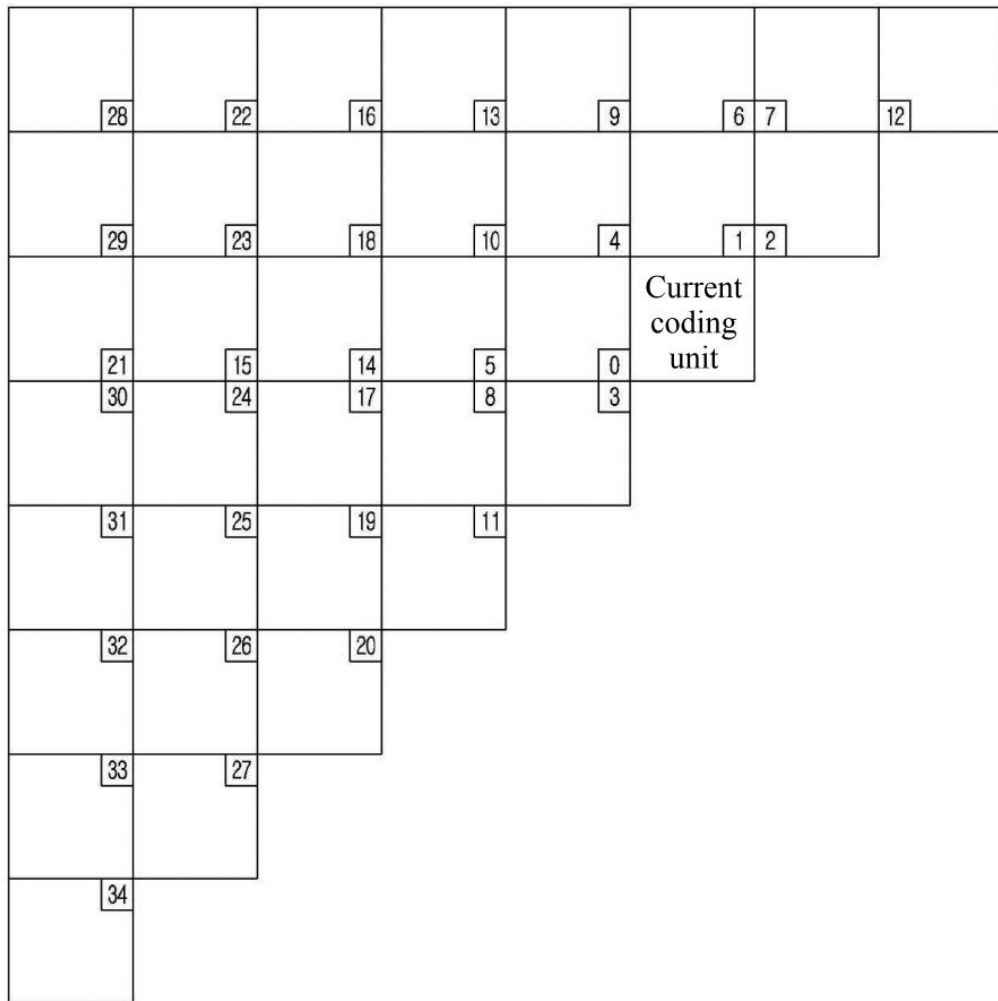


Fig. 14

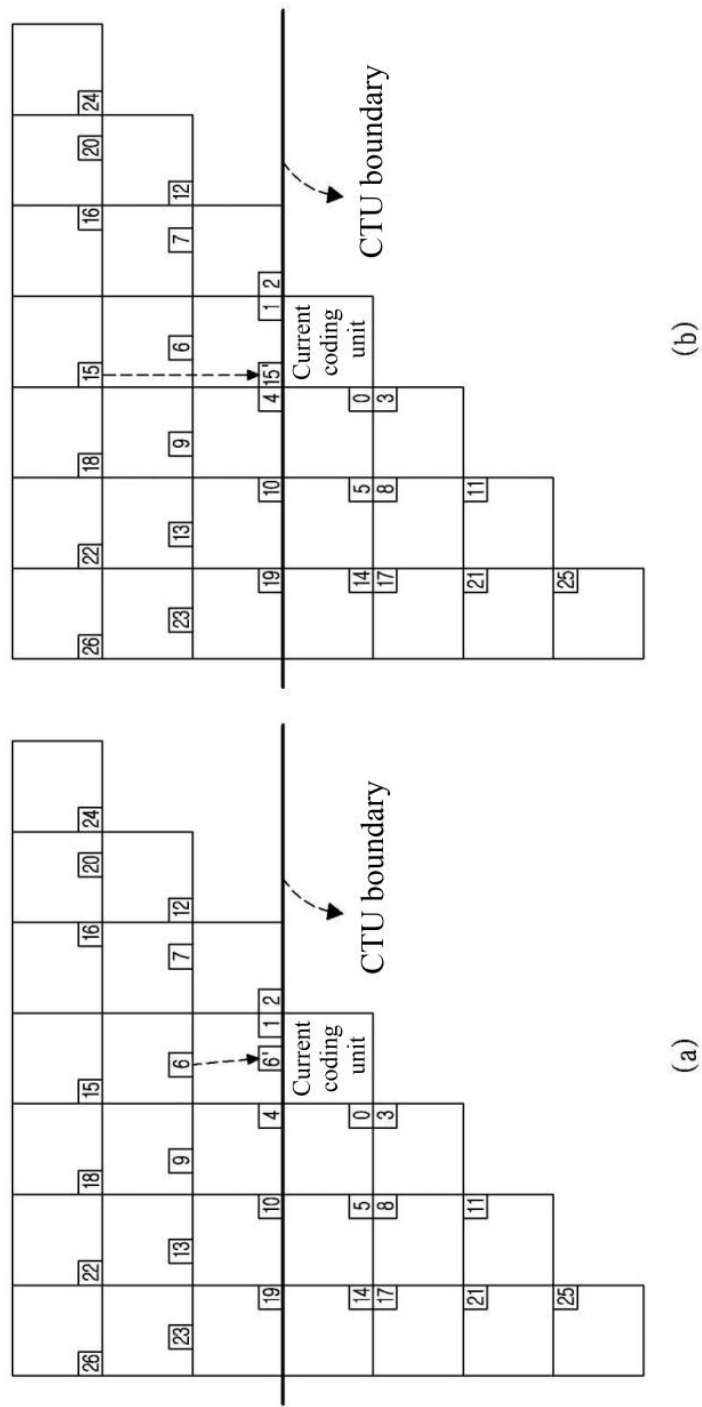


Fig. 15

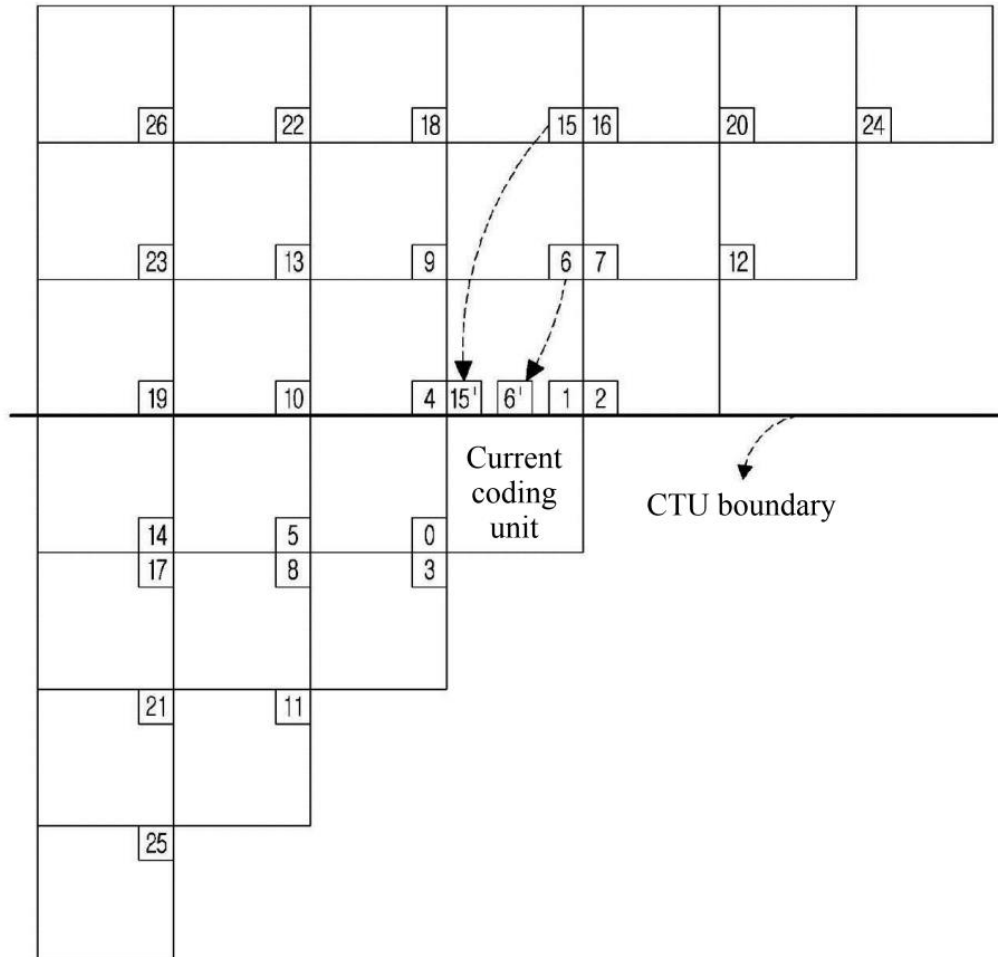


Fig. 16

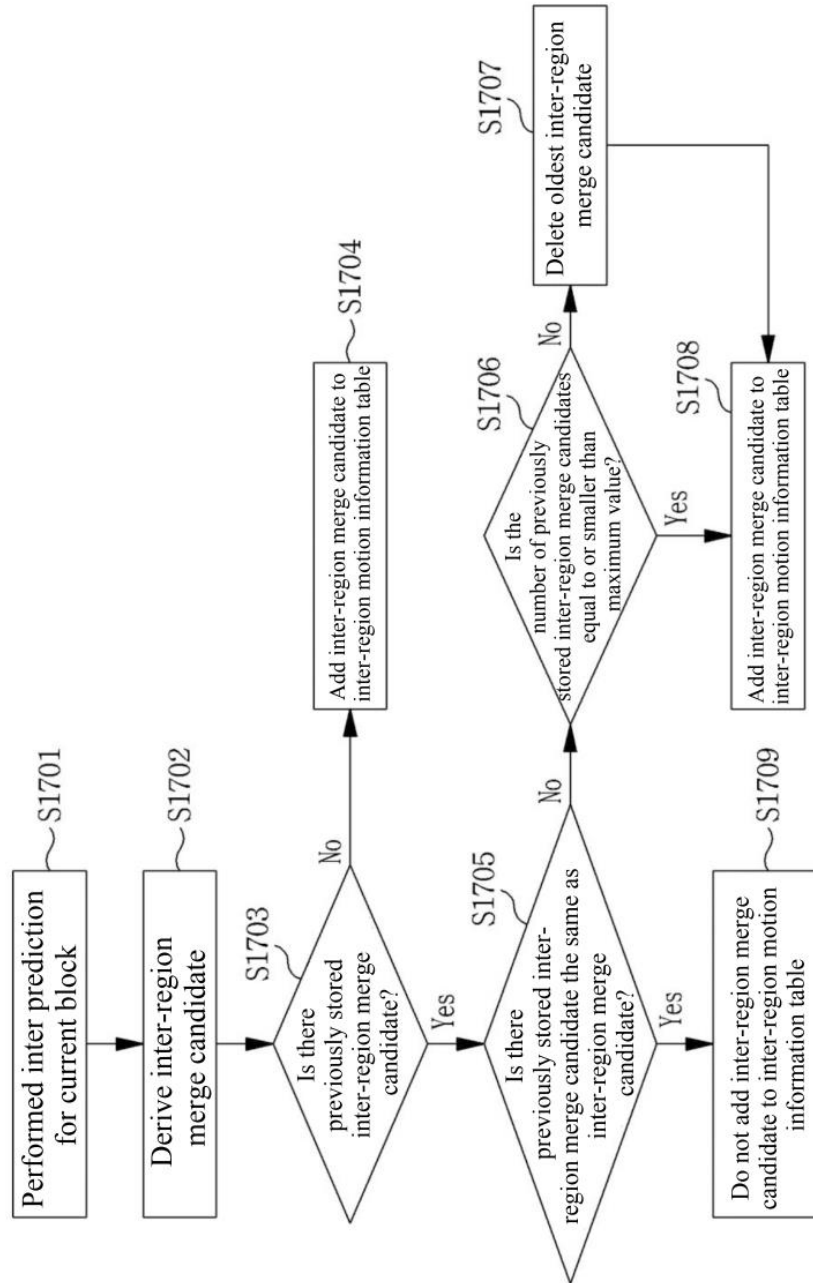


Fig. 17

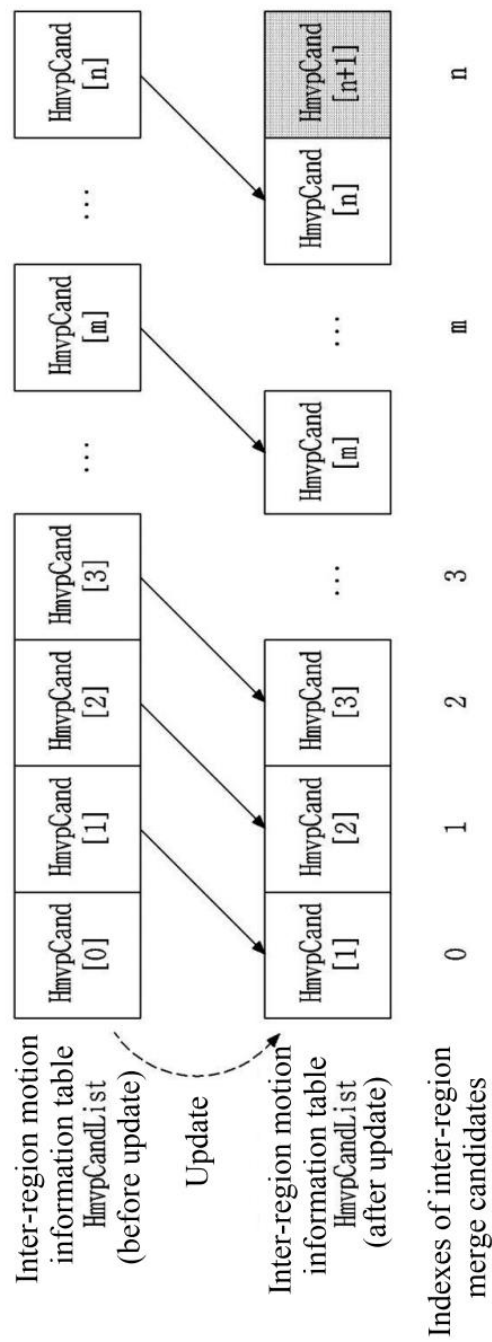


Fig. 18

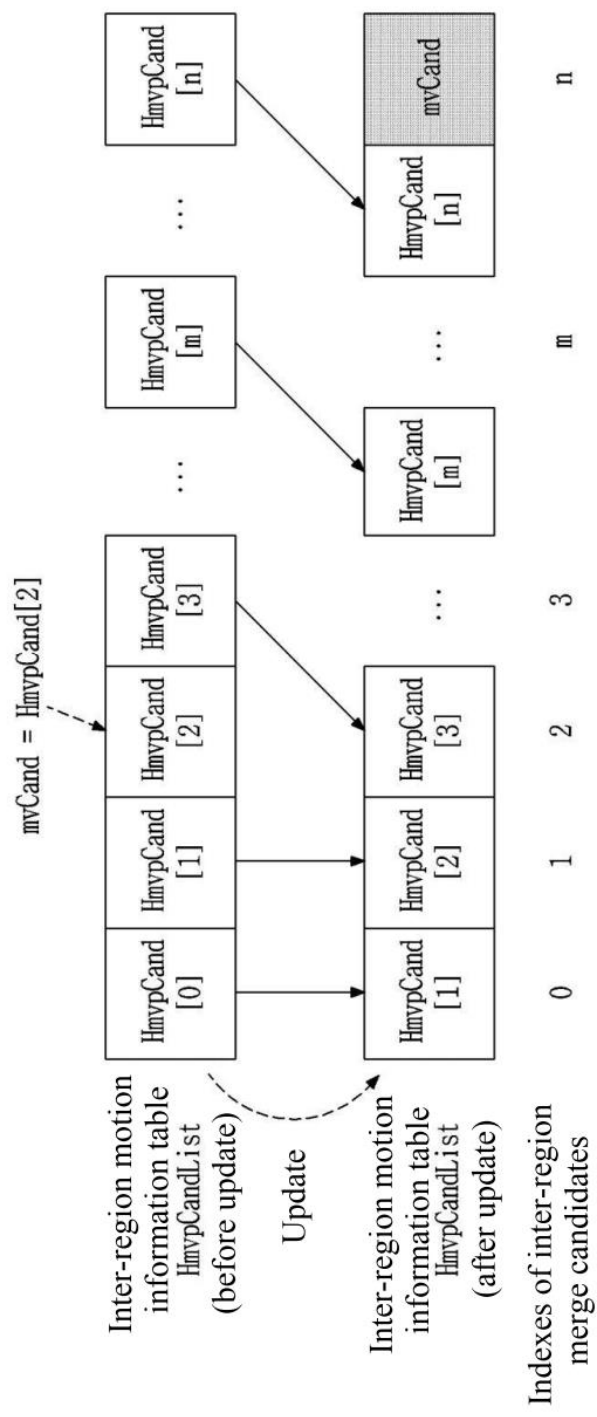
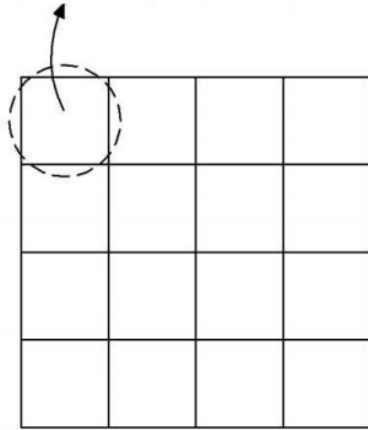


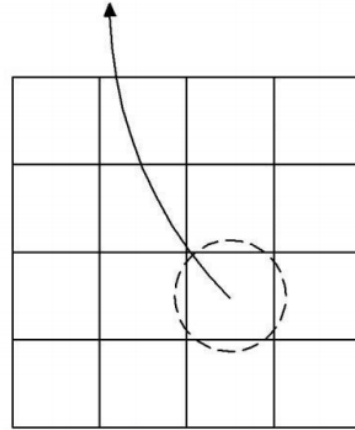
Fig. 19

Representative subblock



(a)

Representative subblock



(b)

Fig. 20

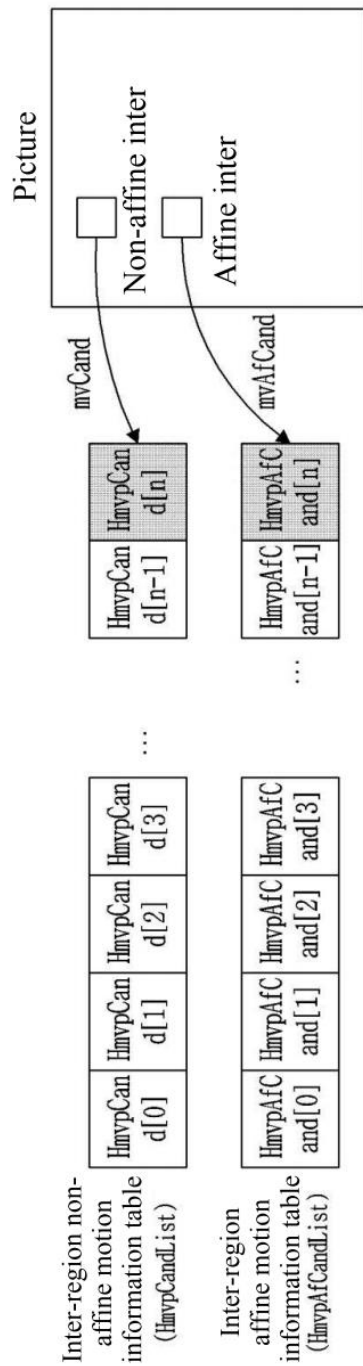


Fig. 21

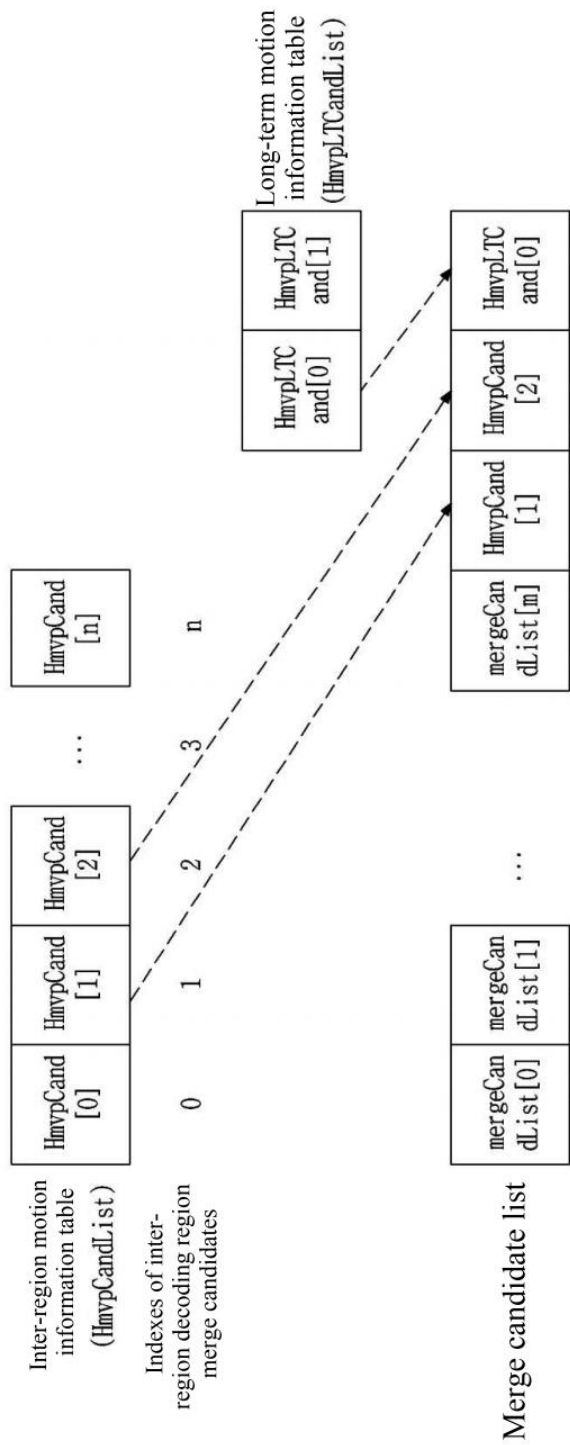


Fig. 22

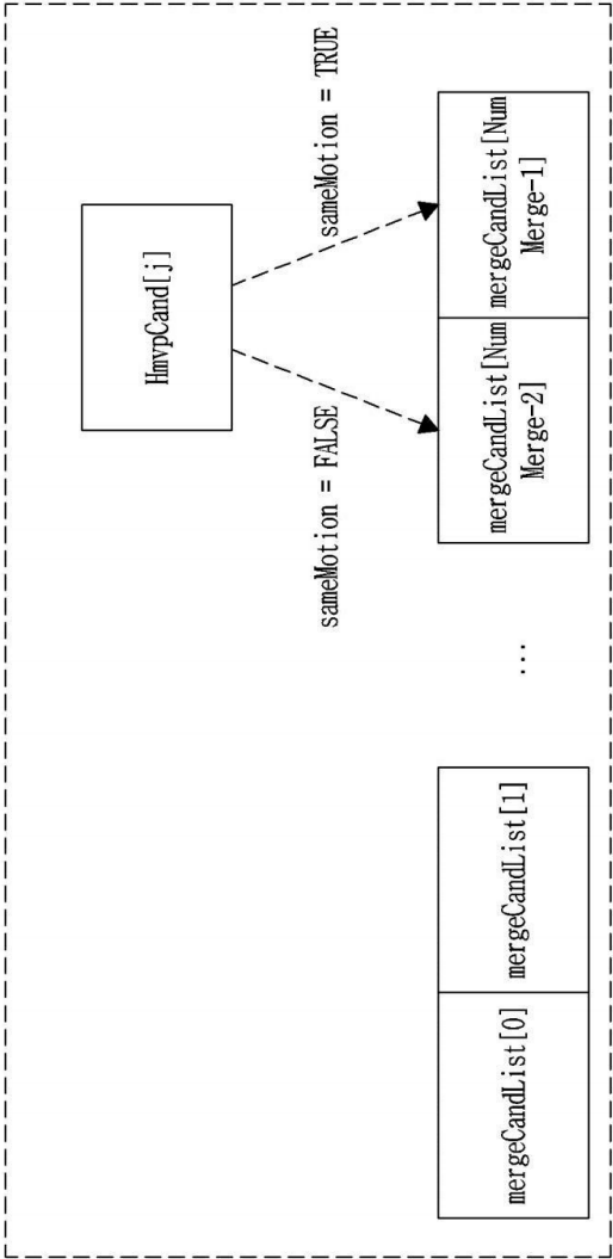


Fig. 23

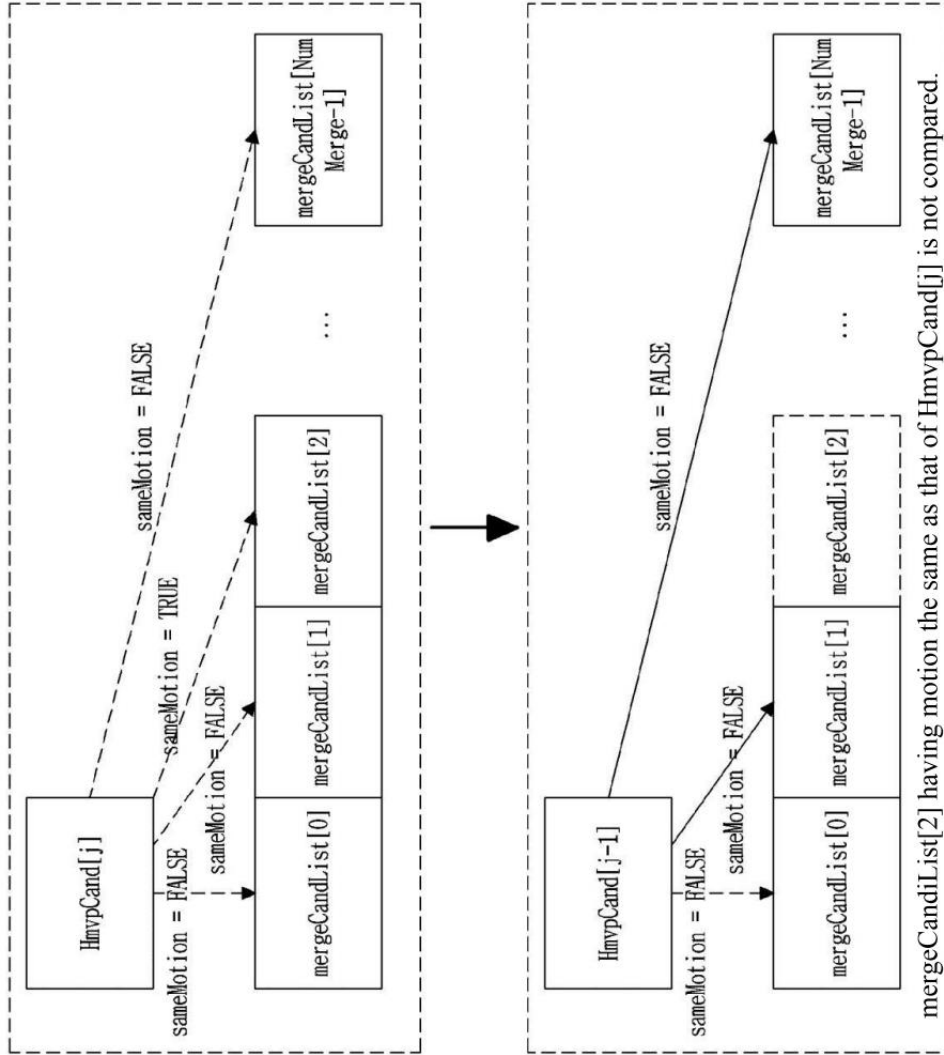


Fig. 24

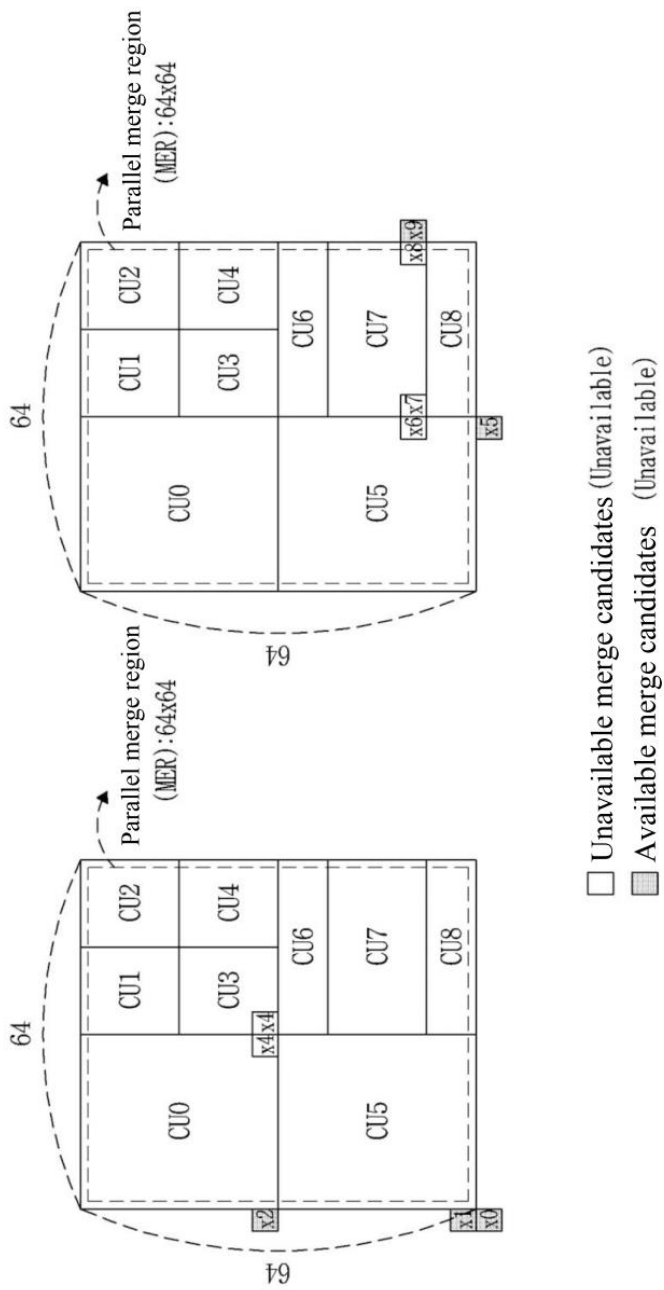


Fig. 25

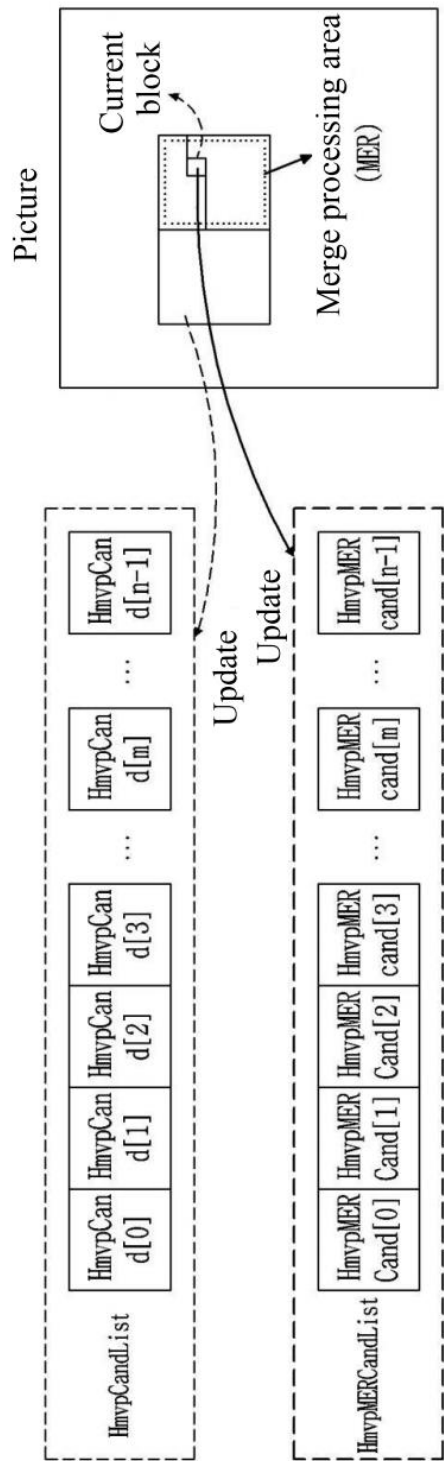


Fig. 26

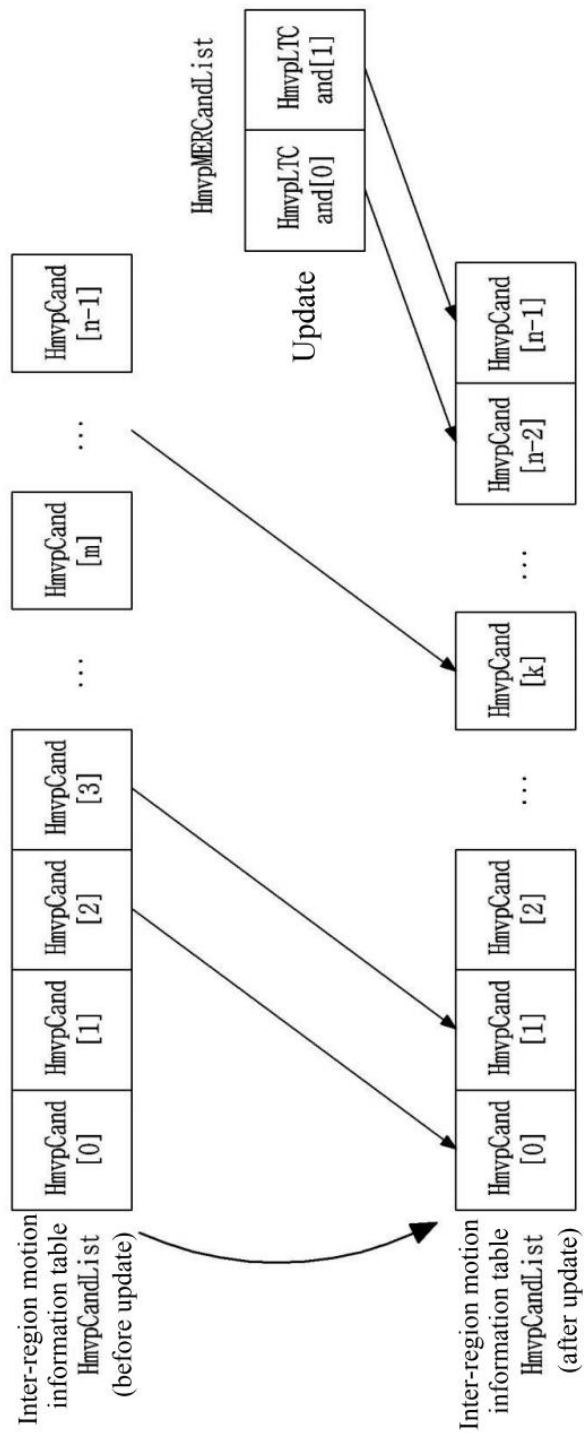


Fig. 27

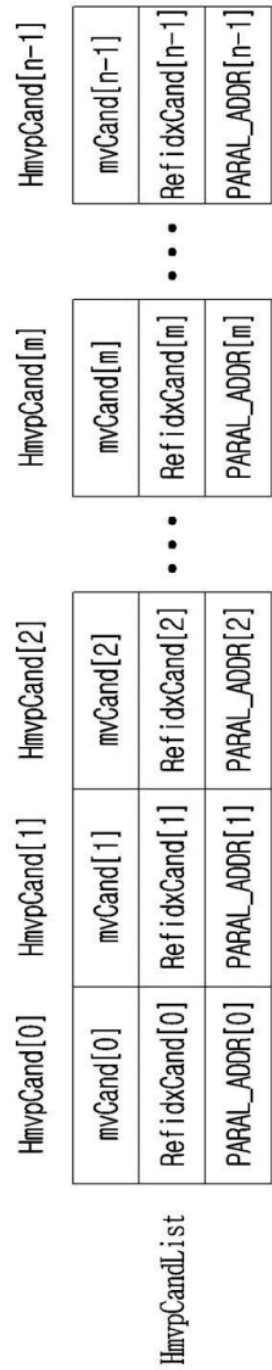


Fig. 28

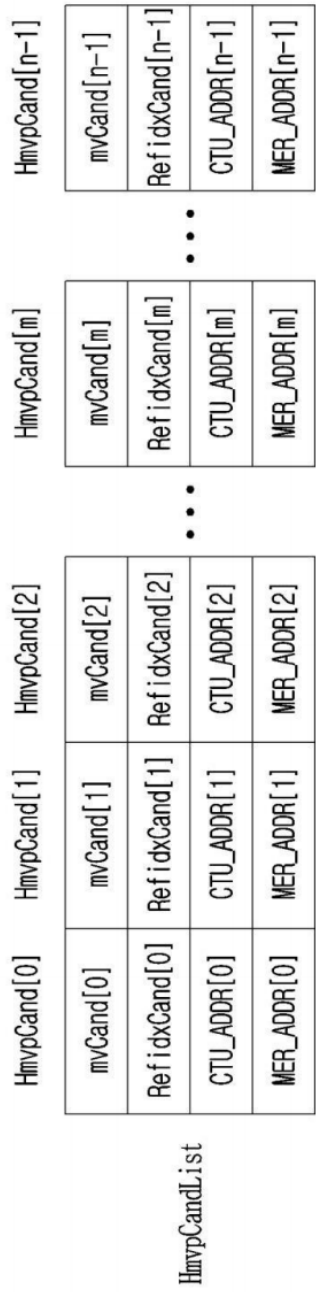


Fig. 29

HmvpCandList		HmvpCand[0]	HmvpCand[1]	HmvpCand[2]	HmvpCand[3]	HmvpCand[4]	HmvpCand[5]
		mvCand[0]	mvCand[1]	mvCand[2]	mvCand[2]	mvCand[2]	mvCand[2]
		RefIdxCand[0]	RefIdxCand[1]	RefIdxCand[2]	RefIdxCand[2]	RefIdxCand[2]	RefIdxCand[2]
		PARAL_ADDR[0]=0	PARAL_ADDR[0]=1	PARAL_ADDR[0]=4	PARAL_ADDR[0]=4	PARAL_ADDR[0]=4	PARAL_ADDR[0]=2

Fig. 30

HmvpCand[0]	HmvpCand[1]	HmvpCand[2]	HmvpCand[3]	HmvpCand[4]	HmvpCand[5]
mvCand[0]	mvCand[1]	mvCand[2]	mvCand[3]	mvCand[4]	mvCand[5]
RefIdxCand[0]	RefIdxCand[1]	RefIdxCand[2]	RefIdxCand[3]	RefIdxCand[4]	RefIdxCand[5]
CTU_ADDR[0]=0	CTU_ADDR[1]=0	CTU_ADDR[2]=1	CTU_ADDR[3]=1	CTU_ADDR[4]=2	CTU_ADDR[5]=2
MER_ADDR[0]=1	MER_ADDR[1]=2	MER_ADDR[2]=2	MER_ADDR[3]=2	MER_ADDR[4]=0	MER_ADDR[5]=1

HmvpCandList

Fig. 31