CLAIMS:

1. A method used in forming a memory array, comprising:

forming a stack comprising vertically-alternating first tiers and second tiers, a first insulator tier being above the stack; first insulator material of the first insulator tier comprising at least one of (a) and (b), where (a): silicon, nitrogen, and one or more of carbon, oxygen, boron, and phosphorus, and (b): silicon carbide; channel-material strings being in the stack and in the first insulator tier, conducting material being in the first insulator tier directly against sides of individual channel-material strings;

forming a second insulator tier above the first insulator tier and the conducting material, second insulator material of the second insulator tier comprising at least one of the (a) and the (b), the first and second insulator materials of the first and second insulator tiers, respectively, not being directly against one another; and

forming conductive vias extending through the second insulator tier that are individually directly electrically coupled to the individual channel-material strings through the conducting material.

2. The method of claim 1 comprising forming the first and second insulator materials to be of the same composition relative one another.

3. The method of claim 1 comprising forming the first and second insulator materials to be of different compositions relative one another.

4. The method of claim 1 comprising forming the second insulator material directly against tops of the conducting material.

5. The method of claim 1 wherein the second insulator material is not formed directly against tops of the conducting material.

6. The method of claim 1 comprising forming the conducting material to project upwardly from the first insulator material.

7. The method of claim 1 wherein the conducting material is not formed to project upwardly from the first insulator material.

8. The method of claim 1 wherein the first insulator material of the first insulator tier comprises the (a).

9. The method of claim 8 wherein said one or more of carbon, oxygen, boron, and phosphorus in the first insulator material has a total concentration of at least about 2 atomic percent.

10. The method of claim 8 wherein the one or more of the first insulator material comprises carbon.

11. The method of claim 8 wherein the one or more of the first insulator material comprises oxygen.

12. The method of claim 8 wherein the one or more of the first insulator material comprises boron.

13. The method of claim 8 wherein the one or more of the first insulator material comprises phosphorus.

14. The method of claim 1 wherein the first insulator material of the first insulator tier comprises the (b).

15. The method of claim 1 wherein the first insulator material of the first insulator tier comprises silicon, carbon, nitrogen, and one or more of oxygen, boron, and phosphorus.

16. The method of claim 1 wherein the second insulator material of the second insulator tier comprises the (a).

17. The method of claim 1 wherein the second insulator material of the second insulator tier comprises the (b).

18. A method used in forming a memory array, comprising:

forming a stack comprising vertically-alternating first tiers and second tiers;

forming a first insulator tier above the stack, first insulator material of the first insulator tier comprising at least one of (a) and (b), where (a): silicon, nitrogen, and one or more of carbon, oxygen, boron, and phosphorus, and (b): silicon carbide;

forming channel-material strings in the stack and in the first insulator tier, conducting material being in the first insulator tier directly against sides of individual channel-material strings;

forming multiple insulating tiers above the first insulator tier and the conducting material, one of the multiple insulating tiers comprising second insulator material comprising at least one of the (a) and the (b), the first and the second insulator materials of the first insulator tier and the one of the multiple insulating tiers, respectively, not being directly against one another, another of the multiple insulating tiers not comprising either of the (a) and the (b); and

etching contact openings through the one and another insulating tiers and thereafter forming conductive vias in the contact openings that are individually directly electrically coupled to the individual channel-material strings through the conducting material.

19. The method of claim 18 comprising forming the one of the multiple insulating tiers directly against tops of the conducting material.

20. The method of claim 18 wherein the one of the multiple insulating tiers is not formed directly against tops of the conducting material.

21. A memory array comprising:

a vertical stack comprising alternating insulative tiers and conductive tiers,

a first insulator tier above the vertical stack, first insulator material of the first insulator tier comprising at least one of (a) and (b), where (a): silicon, nitrogen, and one or more of carbon, oxygen, boron, and phosphorus, and (b): silicon carbide;

channel-material strings of memory cells in the vertical stack, channel material of the channel-material strings being in the first insulator tier;

conducting material in the first insulator tier directly against sides of individual channel-material strings;

a second insulator tier above the first insulator tier and the conducting material, second insulator material of the second insulator tier comprising at least one of the (a) and the (b), the first and second insulator materials of the first and second insulator tiers, respectively, not being directly against one another; and

conductive vias extending through the second insulator tier that are individually directly electrically coupled to the individual channel-material strings through the conducting material.