This Sheet Has Been Replaced

DIGITAL PROCESSOR AND VITERBI DECODER HAVING SHARED MEMORY

Abstract

An integrated circuit includes a digital signal processor (DSP) (e.g., 101) and an error correction co-processor (ECCP) (e.g., 113) that implements a Viterbi decoding function. The DSP and ECCP share a block of multi-port memory (e.g., 116), typically by bus multiplexing a dual-port RAM. When the ECCP possesses the RAM, it inhibits the DSP from accessing that block of the RAM by asserting an EBUSY flag. This technique conserves and optimizes the RAM usage, allowing the DSP and ECCP to advantageously be formed on the same integrated circuit chip.