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## (54) DIGITAL ELECTRONIC TIMEPIECE

(71) We, CITIZEN WATCH COMPANY LIMITED, a corporation organized under the laws of Japan, of No. 9-18, 1-chome, Nishishinjuku, Shinjuku-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

This invention relates to electronic timepieces and, more particularly, to a digital electronic timepiece which can serve as a chronograph.

Due to recent development in crystal oscillators and electronic components of a high quality, timepiece accuracy is highly improved so that daily time-keeping error can be kept within 0.05 seconds. Recent trend in the filed of digital electronic timepieces requires that the timepiece provide various functions such as a stop-watch otherwise known as a chronograph, a calendar function as well as a normal timekeeping function. In conventional digital electronic timepieces, it has been a usual practice to have the timepiece equipped with a numeral display section independently of display sections for a normal timekeeping data and calendar data. This makes it difficult to read chronograph information because of its rapid changes in displayed data.

According to the present invention, there is provided a digital electronic timepiece comprising: an oscillator circuit providing a relatively high frequency signal; a frequency divider dividing down the relatively high frequency signal to provide a first low frequency signal at 1 Hz and a second low frequency signal higher in frequency than the first low frequency signal; a first counter responsive to the first low frequency signal to provide time of day and calendar information signals and an additional time data signals a second counter responsive to the second low frequency signal to provide output signals indicating elapsed time in fractions of a second; first display means for displaying time and calendar data in response to the time and calendar information signals; second display means composed of a plurality of display segments for displaying elapsed time data said segments being activated in step-wise fashion in response to the output signals from the second counter, said display segments serving also as means for displaying the additional time data; and switching means for enabling said second display mean to display said additional data.

In the accompanying drawings:-

Figure 1 shows plan views of the faces of a liquid crystal display device of an embodiment of a digital electronic timepiece according to the present invention;

Figure 2A is a block diagram of the digital electronic timepiece shown in Figure 1;

Figure 2B is a detail circuitry for a part of the electronic timepiece shown in Figure 2A;

Figure 3 shows plan views illustrating the faces of a liquid crystal display device of another preferred embodiment of a digital electronic timepiece according to the present invention;

Figure 4 is a block diagram of the electronic timepiece shown in Figure 3;

Figure 5 is a plan view illustrating the face of a liquid crystal display device of another preferred embodiment of a digital electronic timepiece according to the present invention;

Figure 6 is a block diagram of the electronic timepiece shown in Figure 5;

Figure 7 shows plan views the face of a liquid crystal display device of another preferred embodiment of a digital electronic timepiece according to the present invention;

Figure 8 is a block diagram of the electronic timepiece shown in Figure 7;

Figure 9 shows plan views of the faces of a liquid crystal display device of another preferred embodiment of a digital electronic timepiece according to the present invention;

Figure 10 shows plan views of the faces of a liquid crystal display device of another preferred embodiment of a digital electronic timepiece according to the present invention;

Figure 11 shows plan views of the faces of a liquid crystal display device of another preferred embodiment of a digital electronic timepiece according to the present invention;

Figure 12 is a block diagram of another preferred embodiment of a digital electronic timepiece according to the present invention;

Figure 13 is a detail circuitry for a part of the electronic timepiece shown in Figure 12;

Figure 14 is a detail circuitry illustrating a modification of the circuit shown in Figure 13;

Figure 15 is a timing chart for the waveforms of various signals generated by the circuit of Figure 13;

Figure 16 is a timing chart for the waveforms of various signals produced by the circuit of Figure 14; and

Figure 17 is a block diagram of another preferred embodiment of an electronic timepiece according to the present invention.

Figure 1(1) shows the face of a liquid crystal display 22 which simultaneously displays time and calendar information. Reference numerals 1 to 6 respectively designate years, months, date, hours, minutes and seconds in the form of numerals. Reference numeral 7 denotes a band of seven segments for a days of the week display. Here, one of the segments is extinguished so as to reveal a character printed on a reflective plate or the like. A system is adopted in which the extinguished point is shifted or transposed from day to day in a continuous manner. Reference numeral 8 denotes a band of ten segments for a step-wise display in units of 1/10 second. In other words, from segment 8a to segment 8j the cumulative activation of successive segments indicates the passage of time in units of 1/10 second so that 0/10, 1/10, 2/10,.... can be displayed. In the state shown, all of the segments up to and including segment 8e are activated thereby showing the passage of 4/10 of one second. Figure 1(2) illustrates another example of a 1/10 second step-wise display in which the segments from 9a to 9j are in the activated state sequentially only one at a time so that a shift of transposition is made from one segment to another so that 0/10, 1/10, 2/10 can be displayed. In this case, also the passage of 4/10 of one second is shown.

It is possible to start either the cumulative or transposed display from the right as well as the left hand side and then reverse the direction of activation every second so that the segments will activate in one direction for one second and then activate and return in the opposite direction for the next second.

Figure 1(3) depicts another example of the display face in which a band of nine segments 10a to 10j indicating 1/10 second increments are activated step-wise and remain activated this providing a cumulative-type display. 0/10 second is indicated when all of the segments are extinguished. Each activated segment represents 1/10 second. In the diagram, segments 10a to 10c are activated thereby indicating 3/10 of one second. Figure 1(4) is still another example of the invention in which a band of nine segments 11a to 11j indicating 1/10 second increments are individually activated one at a time so that a shift is made from segment to adjacent segment thus providing a transposed display. 0/10 second is indicated when all of the segments are extinguished. Here, segments are activated one at a time from the left at increments of 1/10 second, and once again 3/10 of one second is illustrated since segment 11c is activated.

In the step-wise transposed display of Figures 1(2) and (4), there are cases where sufficient contrast is not obtained because the time interval required for one segment to shift to another is too short with respect to liquid crystal response. In other words, the extinguishment of a segment is not completed before the succeeding segment is activated. There is thus an operation in which extinguishment is delayed until activation is assured, namely an operation in which other successive segments are simultaneously activated. These are shifted as a group so as to display the passage of time. The same technique may be used in a timer mode.

Until the above occurs the progress of time is displayed by activation although it is also possible to express this in reverse manner by means of showing extinguishment. Figure 1(5) shows 10 segments 12a to 12j arranged in circular fashion. This is a step-wise cumulative display system in which segments indicative of 1/10 second are successively activated in the clockwise direction at increments of 1/10 second so that 0/10, 1/10, 2/10,.... seconds can be displayed. In the state shown, segments 12a to 12d are activated thereby indicating an elapsed time of 3/10 of one second. Reference numeral 3 denotes two digits for the purpose of displaying seconds units in terms of numerals. It is of course permissible to leave the

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center of the circle blank or insert information other than seconds information.

Figure 1(6) shows nine segments 24a to 24j arranged in circular fashion. This is a step-wise cumulative display in which segments indicative of 1/10 second are successively activated in the clockwise direction at increments of 1/10 second so that 1/10, 2/10.....seconds can be displayed. 0/10 second is indicated when all of the segments are extinguished. In the state shown, segments 14a through 14c are activated thereby indicating an elapsed time of 3/10 of one second. It is of course possible to adopt a step-wise transposed display and one in which the progress of time can be displayed by means of extinguishment. The direction of activation or extinguishment may be either clockwise or counter-clockwise although it goes without saying that the clockwise direction is in keeping with tradition. In addition, the circular arrangement may be replaced by another such as a square configuration.

Figure 2A shows a block diagram of the digital electronic timepiece shown in Figure 1(1). In Figure 2A, the digital electronic timepiece comprises an oscillator circuit 15 controlled by a quartz crystal (not shown) to provide a relatively high frequency signal of, for example, 32,768 Hz. This relatively high frequency signal is divided down by a frequency divider 16 to a 1/10 second signal a and one signal b. The one second signal b is applied to a timekeeping counter 17 composed of a seconds counter, minutes counter, hours counter, AM/PM counter, days of week counter, dates counter, months counter and years counter all of which are (not shown) which produce a seconds signal, minutes signal, hours signal, AM/PM signal, days of the week signal, date signal, months signal and years signal. The 1/10 second signal a is applied to a chronograph counter 18 composed of 1/10 counter (not shown) by which output signals are generated in units of 1/10 second so that outputs representative of 0/10, 1/10, 2/10.....of one second can be obtained. The electronic timepiece also comprises an external control member 19 composed of one or plurality of switches adapted to generate various switching signals, which are applied to a control circuit 20. The control circuit 20 is arranged to generate a start signal d to start the chronograph counter 18, a stop signal e to stop the same, and a reset signal f to reset the chronograph counter 18 in response to the switching signals c delivered from the external control member 19. When the start signal d is applied to the chronograph counter 18, it generates 0/10, 1/10, 2/10.....signals during a time interval in which the start signal d is at a high logic level. During the time interval in which the start signal d is generated, the switching circuit 21 allows to pass the output signals from the chronograph counter 18 to the display device 22 in response to a control signal g. A chronograph display signal h is also applied to the display device 22 from the control circuit 20 in response to the signals d and g. Under these circumstances, the band 8 of segments of the display device 22 provides a step-wise display for the data of the chronograph counter 18 in units of 1/10 second.

When the control signal g goes to a low logic level, the switching circuit 21 permits to pass the output signals from the timekeeping counter 17 to the display device 22 so that the data of the timekeeping counter 17 is displayed. Indicated as i is an AM/PM display enabling signal and j a days of week display enabling signal.

Figure 2B shows an example of a detail circuitry of an essential portion of the timepiece shown in Figure 2a. The switching circuit 21 is shown as comprising a first group of transmission gates TG1 through TG4 having respective control gates coupled through an inverter 23 to lead g connected to the control circuit 20 (see Figure 2A). The transmission gates TG1 through TG4 have data input terminals TG1a through TG4a which are connected to the days of week counter (not shown) of the timekeeping counter 17. During normal operating condition of the timepiece, since the control signal g is at a low logic level, the first group of the transmission gates TG1 through TG4 are turned on so that outputs of the days of the week counter are passed to output leads 24 through 27. The switching circuit 21 also comprises a second group of transmission gates TG5 through TG8 having their respective data input terminals TG5a through TG8a coupled to the chronograph counter 18 and controlled by the control signal g generated by the control circuit 20. When the chronograph counter 18 is started, the control signal g goes to a high logic level and the transmission gates TG5 through TG8 are turned on so that the outputs of the chronograph counter 18 are passed through output leads 24 through 27, respectively to a decoder 28. In this manner, the outputs of the days of week counter and the chronograph counter are selectively passed through the switching circuit 21 to the decoder 28 of the display device 22. The decoder 28 is composed of a plurality of decoding circuits 28a through 28j. The decoding circuit 28a is composed of a first OR gate OR1 having first through fourth inputs connected to the output leads 24 through 27, respectively, and a fifth input connected to the control circuit 20 to receive the days of week display enabling signal j; a second OR gate OR2 having a first input connected to the output lead 26, a second input connected to the output lead 27, and a third input connected to the control circuit 20 to receive the chronograph data display enabling signal h; and a third OR gate OR3 having first, second,

third and fourth inputs coupled to leads 24, 25, 26 and h. Outputs of these OR gates are connected to inputs of a NAND gate whose output is coupled to an output terminal labeled SUN. Similarly, the decoding circuit 28b comprises three OR gates and a NAND gate having its output coupled to a terminal MON. The decoding circuit 28c comprises four OR gates and a NAND gate whose output coupled to a terminal labeled TUE. The decoding circuit 28d comprises two OR gates and a NAND gate labeled WED. The decoding circuit 28e comprises three OR gates and a NAND gate whose output coupled to a terminal labeled THU. Similarly, outputs of respective NAND gates of the decoding circuits 28f through 28j are connected to terminals labelled FRI, STA, \*, AM and PM, respectively. The AM/PM data from the AM/PM counter of the timekeeping circuit 17 is applied to lead k to which one input of a fifth OR gate OR5 of the decoding circuit 28i is directly coupled and one input of an OR gate OR3 of the decoding circuit 28j is also coupled through an inverter (no numeral).

During the days of week data display, the control signal g is at a low logic level and, therefore, the first group of transmission gates TG1 through TG4 are turned on. In this condition, the outputs of the days of week counter of the timekeeping circuit 17 are applied through output leads 24 through 27 to the decoding circuits 28a through 28j, respectively. Also, the AM/PM signal k is applied to the decoding circuits 28a through 28j. Since, in this instance, the chronograph data display enabling signal h is at a high logic level, closing the OR gates OR2 and OR3 of the decoding circuit 28a, OR gates OR2 and OR3 of the decoding circuit 28b, OR gates OR2, OR3 and OR4 of the decoding circuit 28c, OR gate OR2 of the decoding circuit 28d, OR gates OR2 and OR3 of the decoding circuit 28e, OR gates OR2 and OR3 of the decoding circuit 28f, OR gates OR2, OR3 and OR4 of the decoding circuit 28g, OR gate OR2 of the decoding circuit 28h, OR gates OR2, OR3 and OR4 of the decoding circuit 28i, and OR gate OR2 of the decoding circuit 28j. Consequently, one of the OR gates OR1 of the decoding circuits 28a through 28g is selected in accordance with the content of the days of week counter and an output of the corresponding decoding circuit is applied through the output terminal to the display segment (not shown) by which the content of the days of week counter is displayed. At the same time, one of the OR gate OR5 of the decoding circuit 28i and the OR gate OR3 of the decoding circuit 28j is selected in response to the signal k and AM or PM is displayed.

During the chronograph data display, the control signal g is at a high logic level. Accordingly, the first group of transmission gates TG1 through TG4 are turned off whereas the second group of transmission gates TG5 through TG8 are turned on. Therefore, the outputs of the chronograph counter (1/10 second counter) 18 are applied to the decoding circuits 28a through 28j. Since, in this instance, the AM/PM display enabling and flashing signal is at a high of the decoding circuit 28j are closed. When the chronograph is in run-on condition, the chronograph data display enabling signal h is at a low logic level, and the decoding circuit 28a is selected when the content of the 1/10 second data remains in a range from 0/10 to 4/10. Similarly, the decoding circuits 28b, 28c, 28d, 28e, 28f, 28g, 28i and 28j are selected when the 1/10 second data remains in ranges of from 1/10 to 5/10, from 2/10 to 6/10, from 3/10 to 7/10, from 4/10 to 8/10, from 5/10 to 9/10, from 6/10 to 9/10 and 0/10, from 7/10 to 9/10, 0/10 and 1/10, from 8/10 to 9/10 and from 0/10 to 2/10, and 9/10 and from 0/10 to 3/10. When the chronograph is stopped, the chronograph data display signal enable signal goes to a high logic level. Since, in this condition, only the OR gates OR1 of the decoding circuits 28a through 28j are opened, one of the OR gates 1 of the decoding circuits is selected in dependence on the content of the chronograph counter 18 at the time instant when the chronograph is stopped. Thus, the output from the selected decoding circuit is applied through its output terminal to the corresponding display segment by which the content of the chronograph counter is displayed.

Figure 3 shows the face of a display in which a switch is made from a time to a calendar display. Figure 3(1) shows a case in which hours, minutes and seconds are displayed by numerals, 1/10 seconds are displayed by nine segments which are activated in a step-wise, cumulative fashion, with 3/10 of one second of elapsed time indicated in the present drawing. The application of a switch signal 30 switches the time display of Figure 3(1) to the calendar display of Figure 3(2). The application of the same signal reverses the display to its original state. In the calendar of Figure 3(2) the display numerals for the months, date and days presentation are common with the digits used for the hours, minutes and seconds of the time display. The days of the week display adopts a system in which the segments are extinguished in step-wise fashion with the illuminated segment shifting from day to day. Of the nine segments which comprise the 1/10 seconds display the first seven are adapted to reveal the printed characters of the day of the week while the last two are for the AM-PM display. In place of the arrangement of Figure 3(2), Figure 3(3) shows a case where the seven central segments are employed for the days of the week display while the two segments at either end are left for some other purpose.

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Figure 4 depicts a block diagram to explain the switchover from a time display to the calendar display of Figure 3(2). Reference numeral 31 denotes a quartz crystal controlled oscillator and reference numeral 32 a frequency divider which supplies a 1/10 second signal to a 1/10 second counter 33. Reference numeral 34 designates a seconds counter, 35 a minutes counter, 36 an hours counter, 37 an AM-PM counter (a divide by 12 counter for determining AM and PM), 38 a days of the week counter, 39 a dates counter, 40 a months counter and 41 a years counter. Reference numeral 42 denotes a switching gate for selecting between 1/10 second counter 33, AM-PM counter 37 and days of the week counter 38, reference numeral 43 denotes a switching gate for selecting between seconds counter 34 and dates counter 39, reference numeral 44 designates a switching gate for selecting between minutes counter 35 and months counter 40, and reference numeral 45 denotes a switching gate for selecting between hours counter 36 and years counter 41. Switching signal 30 simultaneously selects either a time mode or calendar mode, and display sections 42a to 45a display the mode so selected. Display section 42a has nine segments as illustrated in Figure 3(2), and makes joint use of a 1/10 second step-wise display, an AM-PM display, and a days of the week display. Display sections 43a to 45a have segments in the form of numerals which display the selected time system or calendar system shown in Figures 3(1) and (2).

Although the calendar display according to the above-mentioned switching method is somewhat complicated, this is permitted in wristwatches and is also advantageous in that an easy-to-read, comparatively large pattern with respect to the limited display area can be used. However, the main advantage resides in the fact that only 25 electrodes are necessary if a static step-wise display section and a dynamic numerical display section are adopted.

Next, an electronic timepiece will be described which is provided with a stop-watch function applied to a 1/10 second step-wise display. In other words, a digital timepiece with a chronograph function is as depicted in Figure 5. Here, reference numeral 50 denotes an elapsed time display section in which hours, minutes and seconds are displayed by numerical segments, while units of 1/10 second are represented by a band of nine segments which are illuminated step-wise in a cumulative manner. Among the step-wise display arrangements it is also possible to employ a circular array as previously described. Reference numeral 51 denotes a time of day display section in which hours, minutes and seconds are represented by numerals.

Figure 6 is a block diagram for an explanation of the timepiece shown in Figure 5. Reference numerals 31 to 36 designate the same components as previously described with reference to Figure 4. Reference numeral 34a, 35a and 36a designate decoder drivers for seconds, minutes and hours, respectively. Reference numeral 52 denotes a 1/10 second counter for elapsed time, 53 a seconds counter, 54 a minutes counter and 55 an hours counter. Reference numeral 52a designates a step-wise display section for units of 1/10 second, and reference numerals 53a to 55a denote numeral display sections for seconds, minutes and hours. Reference numeral 56 designates a control gate which decides whether to pass or block a counting signal supplied by frequency divider 32. Control gate 56 is operated by a signal S. R denotes a reset signal which resets the elapsed time counter to 0. If a latch circuit (not shown) is added to the elapsed time counter it is also possible to provide a lap measuring function.

Although this is a method of simultaneously displaying over the same display area both elapsed time and actual time, display elements and wiring raise the cost even if dynamic driving is adopted. However, if the timepiece is a wristwatch, it is permissible to switch between elapsed time and actual time and then display the mode so selected. Figure 7 is such an example.

In Figure 7 there is shown a display device for a digital electronic timepiece with a chronograph function that can be switched to at will. Figure 7(1) shows an elapsed time display in which hours, minutes and seconds of elapsed time are represented by numerals while elapsed time measured in units of 1/10 of a second is accomplished by step-wise, cumulative illumination of the band of segments. Figure 7(2) shows a time display in which hours, minutes and seconds are represented by numerals while units of 1/10 second are represented by the band-like segments which are illuminated step-wise in cumulative fashion. These two displays are selected by a switching signal 61 which is produced by the manipulation of an external control switch. Reference numeral 62 denotes a reference segment which distinguished the elapsed time display from the actual time display so that the two are not mistaken for each other. This segment may take any form whatsoever and can equally well be provided at the side of the actual display or in any desirable location. In order to further distinguish the displays it is also possible to adopt the cumulative and transposed methods for the 1/10 second step-wise display, adapt a system in which the passage of time is shown by illumination or extinguishment, and by selecting a desired direction for showing the passage of time or by allowing time to progress first in one direction and then the other. Although segment 60 makes use of band-like segments, a

circular arrangement may be adopted as previously mentioned.

Figure 8 depicts a block diagram for a description of the contents of a digital electronic timepiece equipped with a chronograph function which is selected by a switching operation. Reference numerals 31 to 36 and 52 to 55 designate the same components as previously described. Reference numerals 65, 66, 67 and 68 designate switching gates for switching between signals from 1/10 second counter and 1/10 second elapsed time counter 52, between signals from seconds counter 34 and seconds elapsed time counter 53, between signals from minutes counter 35 and minutes elapsed time counter 54, and between hours time counter 36 and hours elapsed time counter 55, respectively. Switching signal 61 simultaneously selects either actual time or elapsed time, and display sections 65a to 68a display the mode so selected. Display section 65a has a row of nine segments 60 as illustrated in Figure 7. These serve to display in stepwise fashion 1/10 second units of time or 1/10 second units of elapsed time.

Figure 9(1) depicts a display for elapsed time in which hours, minutes and seconds are represented by numerals while elapsed time in units of 1/10 second is shown by a band of nine segments. Here, 4/10 seconds of elapsed time is indicated. Figure 9(2) shows a display for actual time of day in which the date appears in the position previously occupied by seconds of elapsed time (48 in the Japanese system represents 1973 A.D.). Reference numeral 71 denotes a band of nine segments of which six are used to represent time in units of 10 seconds each. In the system adapted here each of these six segments is individually illuminated so that the time as displayed shifts step-wise from segment to segment. In Figure 9(2), segment 71d indicates time between the 30 and 40 seconds by flashing at a frequency of 1Hz. Reference numerals 71h and 71i are the two remaining segments of the nine segment display and are employed to indicate AM and PM. If a twist liquid crystal is utilized these segments can be made to display the characters printed on a reflective plate. In the diagram, segment 71h indicates AM. Reference numeral 70 denotes a switching signal generated by the manipulation of an external control switch, and reference numeral 62 designates a segment which allows the displays to be distinguished from each other, as previously described.

Figure 10(1) depicts a display for elapsed time and, as in Figure 9, shows that 4/10 second of time has elapsed. Figure 10(2) illustrates a display for actual time which has nine segments, seven of which are used to denote the days of the week while the remaining two are for an AM/PM display. Reference numeral 81 designates a flashing colon, and 80 a switching signal generated by the manipulation of an external control switch. Reference numeral 62 once again denotes a segment for distinguishing between displays.

Figure 11(1) shows an elapsed time display for a chronograph in which hours, minutes and seconds are represented by numerals composed of a plurality of segments. For the 1/10 second units display, segments are disposed within 10 printed frames 90a to 90j, each of these segments being activated individually so that activation shifts from segment to adjacent segment. A row of printed numeral segments 91 ranging from 0 to 9 along the 1/10 second segments are for the purpose of reading the elapsed time as it is displayed by the segments which are activated. As can be appreciated from the diagram, 4/10 seconds of time have elapsed. In addition, characters representative of days of the week and AM/PM have been printed on the face of the liquid crystal display. Although the row of numerals 91 may be printed as shown, they may be arranged to only appear on the display for elapsed time. In Figures 11(2) and (3) a modification is made in which the numerals do not appear.

Figure 11(2) depicts a time display and Figure 11(3) a calendar display. These display states are switched to from the elapsed time display state by a switching signal 92 formed by manipulating an external switch. Reference numeral 90b in Figure 11(3) makes use of a 1/10 second elapsed time display segment of Figure 11(1). In the diagram, days of the week are displayed, and reference numeral 90i designates an AM segment which is shown to be activated. Figure 11(3) shows a calendar display which is switched to from the time display by means of a switch signal 93 provided by the manipulation of a different external control switch. Here, year, month and date are displayed without changing the day of the week of AM/PM information depicted in Figure 11(2).

Figure 12 illustrates a block diagram of another preferred embodiment of an electronic timepiece in accordance with the invention. Reference numeral 100 denotes a crystal controlled oscillator with a frequency of 32,768 Hz, and reference numeral 102 designates a 15 stage frequency divider comprised of dividers 102a through 102o. The frequency of the output signals obtained from each of these stages is as follows:

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|    |         |                    |    |
|----|---------|--------------------|----|
|    | divider | 102a... 16384 Hz   |    |
|    | "       | 102b... 8192 Hz    |    |
|    | "       | 102c... 4096 Hz    |    |
|    | "       | 102d... 2048 Hz    |    |
| 5  | "       | 102e... 1024 Hz    | 5  |
|    | "       | 102f... 512 Hz     |    |
|    | "       | 102g... 256 Hz     |    |
|    | "       | 102h... 128 Hz     |    |
|    | "       | 102i... 64 Hz = f1 |    |
| 10 | "       | 102j... 32 Hz = f2 | 10 |
|    | "       | 102k... 16 Hz = f3 |    |
|    | "       | 102l... 8 Hz = f4  |    |
|    | "       | 102m... 4 Hz       |    |
|    | "       | 102n... 2 Hz       |    |
| 15 | "       | 102o... 1 Hz       | 15 |

Therefore, in order to produce a 10 Hz standard signal (1/10 second signal) from the divided signal frequencies as obtained from frequency divider 102 and the crystal controlled oscillator oscillating at a frequency of  $2^{15}$  (i.e., oscillating at a frequency of  $2^p$  according to the present embodiment), it is necessary to employ a frequency source capable of providing a signal frequency the lower limit of which has a value closest to and greater than 10 Hz, namely a frequency greater than  $2^4 = 16$  Hz.

Reference numeral 103 denotes a frequency reduction circuit which is supplied with frequencies f1 to f4 and adapted to reduce frequency f1 by a ratio of 5/8. The circuit removes 24 pulses from frequency f1 which is comprised of 64 pulses for each one second period, and then produces a frequency signal which consists of 40 pulses over a period of one second. Reference numerals 104 and 105 designate frequency dividers which constitute a frequency divider circuit 106 arranged to divide an input signal by 1/4. The circuit accordingly produces an output signal G having a frequency of 10 Hz.

Figure 13 is a diagram showing in detail an embodiment of circuit 103 illustrated in Figure 12. Figure 15 is a timing chart showing the signal waveforms associated with the main components of Figure 13. Reference numerals 107 to 110 indicate inverters, and reference numeral 111 is a circuit for removing pulses P1 from the frequency signal f1. Circuit 111 is composed of flip-flops constructed by NAND gates 111a and 111b, and an AND gate 111c, and is adapted to provide an output signal A. Reference numeral 112 denotes an AND gate for removing pulses P4 from frequency signal f1 and which supplies an output signal B. Reference numeral 113 designates a NOR gate for removing pulses P7 from frequency signal f1 and which supplies an output signal C. Reference numeral 114 denotes a NOR gate which produces a signal D from frequency signal f1. Accordingly, OR gate 114 which is supplied with signals A through C and a frequency signal f1 from inverter 110 operates to remove pulses P1, P4 and P7 from frequency signal f1 except when signals A, B and C attain low logic levels when f1 is at a low logic level. Consequently, NOR gate 114 produces a 40-pulse signal D for every one second period, and this signal is divided by dividing circuit 106 so as to provide a signal G having a frequency of 10 Hz.

Figure 14 shows another embodiment of circuit 103, and Figure 16 illustrates a timing chart showing the signal waveforms associated with its principal components. Here, reference numerals 115 through 117 denote inverters, reference numeral 118 denotes a circuit constituted by OR gate 118a and AND gate 118b for the purpose of removing pulses P2, P4 and P6 from frequency signal f1 whereby AND gate 118b produces signal E shown in Figure 16. Reference numeral 119 designates a NOR gate and is supplied with signal E and frequency signal f1 obtained from inverter 117. NOR gate 119 is adapted to remove pulses P2, P4 and P6 from frequency signal f1 whenever signal E attains a high logic level at such a time where f1 is at a low logic level. Consequently, NOR gate 119 produces a 40-pulse signal F for every one second period, and this signal is divided by dividing circuit 106 so as to provide a signal G having a frequency of 10 Hz.

It can be understood from Figures 12 through 16 that in this illustrated embodiment,

$$16 \times 2^n \times 5/8 \times 1/2^n = 10 \text{ (Hz)}.$$

Accordingly, with n taken as equal to 2 in the present embodiment, circuit 103 reduces the frequency, i.e., the pulse number, by a ratio of 5/8, taking as the frequency signal the signal f1 which has a frequency of 64 Hz ( $16 \times 2^2$ ) obtainable from the factor  $2^p$ . Thus, 24 pulses are removed, leaving signals D and F which consist of 40 suitably spaced pulses per one second period. Moreover, by using dividing circuit 106 to divide signals D or F by a ratio of  $1/2^2$ , a 10 Hz reference signal Ga is obtained.

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It should be stated here that for the sake of convenience the timing charts shown in Figures 15 and 16 are abbreviated to illustrate only one-half a period since the first and second halves of one period are identical. Furthermore,  $t_0$  through  $t_5$ , and  $t_{0a}$  through  $t_{5a}$  are instantaneous points in time. For the timing errors over the intervals  $t_0$  to  $t_5$  and  $t_{0a}$  to  $t_{5a}$ ,  $t_0$  is taken as representing an error of 0. By so doing,  $t_1$  shows as error of +0.00625,  $t_2$  an error of -0.003125,  $t_3$  an error of +0.003125,  $t_4$  an error of -0.00625, and  $t_5$  after 0.5 seconds of time shows as error of 0. Thus, after a long period of use the cumulative error is 0. Moreover, since the error at any instant in time is suppressed to within  $\pm 0.01$ , this has no practical detrimental effect.

In a similar manner the timing errors which arise in Figure 16 can be expressed as follows, taking the error at  $t_{0a}$  as 0: for  $t_{1a}$ , -0.009375 seconds; for  $t_{2a}$ , -0.003125 seconds; for  $t_{3a}$ , +0.003125 seconds; for  $t_{4a}$ , +0.009375 seconds; and 0 at  $t_{5a}$ . Again, there is no cumulative error after a long period, and instantaneous errors of  $\pm 0.01$  are negligible.

It can thus be appreciated that the illustrated embodiment of Figure 12 makes it possible by very simple means to produce a 0.1 second resolvable standard signal from a crystal controlled oscillator which oscillates at a frequency of  $a^p$ . This has a wide application in electronic timepieces and is particularly suited to adapting a stop-watch function for a wristwatch.

Figure 17 shows a block diagram of another preferred embodiment of an electronic timepiece of the present invention. Reference numeral 201 denotes a crystal controlled oscillator with a frequency of 32768 Hz, and reference numerals 202 through 213 designate flip-flops which constitute a frequency divider by which the following output frequencies are produced:

|         |        |          |
|---------|--------|----------|
| divider | 202... | 16384 Hz |
| "       | 203... | 8192 Hz  |
| "       | 204... | 4096 Hz  |
| "       | 205... | 2048 Hz  |
| "       | 206... | 1024 Hz  |
| "       | 207... | 512 Hz   |
| "       | 208... | 256 Hz   |
| "       | 209... | 128 Hz   |
| "       | 210... | 64 Hz    |
| "       | 211... | 32 Hz    |
| "       | 212... | 16 Hz    |
| "       | 213... | 8 Hz     |

Reference numerals 214 and 215 denote NAND gates, NAND gate 214 receiving signals from frequency dividers 207 and 208, and NAND gate 215 receiving signals from NAND gate 214 as well as flip-flops 209 through 213. An output signal obtained from NAND gate 215 and a signal supplied by flip-flop 206 are applied to AND gate 216 which produces a signal that appears at terminal 217.

Before proceeding with the operation of the above-mentioned circuit, it will be helpful for the sake of understanding to consider the following calculation:

$1024 \times 2^n \times 125/128 = 1000 \times 2^n$ , where  $n$  is an integer. Accordingly, if by way of example  $n = 0$ , a 1024 Hz signal is multiplied by 125/128 so that a 1000 pulse/sec signal appears at terminal 217. Now, if the outputs of frequency dividers 207 through 213 are considered to be at 1 logic levels, then 64 input pulses are required to raise flip-flop 213 to an H level, 32 input pulses are required to raise flip-flop 212 to an H level, and similarly, 16 are required for flip-flop 211, 8 are required for flip-flop 210, 4 are required for flip-flop 209, 1 input pulse is required in order for NAND gate 214 to maintain an H logic level. If the numbers of input pulses required to simultaneously raise flip-flops 209 through 213 and NAND gate 214 to H logic levels are added, the sum is found to be 125. Thus NAND gate 215 produces an H level signal until 125 of 128 input pulses are counted; since the signal maintains an L level signal only during the remaining three pulses, the logical product of flip-flop divider 206 and NAND gate 215 give a signal of 1000 pulse/sec. In other words, for one second of time, a

$$1024 \times 125/128 = 1000 \text{ pulse/sec}$$

signal is obtained. This signal is then divided by a frequency dividing circuit (not shown) which is capable of reducing the frequency by a factor of  $1/2^n$ . Although in the present embodiment no other frequency divider is in fact necessary since  $n = 0$ , a frequency divider with a dividing ratio of  $1/2$  may be employed for a case in which  $n = 1$ . A signal reduced in frequency by a factor of  $1/2^n$  is then applied to a plurality of series connected decimal counters (not shown), and by means of decoders and drivers the content of the decimal counters can be displayed by a display device consisting of liquid crystals or light emitting diodes.

The flip-flop 213 provides an output signal having a frequency of 8 Hz. The error for each 1/8 second is thus  $(128-125)/128$  or  $1/8 \times 3/128 = 0.3\%$  per second. If a 1/1000 second signal is not necessary, the error can be further reduced by 1/10 so as to obtain an error of 0.03% per second when counting in units of 1/100 second. Since in order to obtain a 1 second signal the information at terminal 217 is fed to 3 stages of divide-by 10(decimal) counters, the error for the 1 second signal is substantially reduced to 0 so that there is no cumulative error if measured over a long period of time. Accordingly, since the error is within an allowable tolerance of 0.03% for one second or less, it can be understood that this has sufficient practical value.

It can thus be appreciated that this embodiment of the present invention makes it possible to produce a 1/100 second resolvable signal from a crystal controlled oscillator which oscillates at a frequency of  $2^P$ . This has a wide application in electronic timepiece and is particularly suited to a stop-watch function for a wristwatch.

It will now be appreciated from the foregoing description that since a plurality of segments of a band of segments are arranged to be displayed as a group, it is possible to read time in units of 1/10 second even in a case in which the response speed of a liquid crystal display device is slow.

While the present invention has been shown and described with reference to particular embodiments by way of example, it should be noted that any other modifications or changes may be made without departing from the scope of the present invention.

#### WHAT WE CLAIM IS:-

1. A digital electronic timepiece comprising:  
an oscillator circuit providing a relatively high frequency signal; a frequency divider dividing down the relatively high frequency signal to provide a first low frequency signal at 1 Hz and a second low frequency signal higher in frequency than the first low frequency signal;

a first counter responsive to the first low frequency signal to provide time of day and calendar information signals and an additional time data signal;

a second counter responsive to the second low frequency signal to provide output signals indicating elapsed time in fractions of a second;

first display means for displaying time and calendar data in response to the time and calendar information signals;

second display means composed of a plurality of display segments for displaying elapsed time data; said segments being activated in step-wise fashion in response to the output signals from the second counter, said display segments serving also as means for displaying the additional time data; and

switching means for enabling said second display means to display said additional data.

2. A digital electronic timepiece as claimed in Claim 1, in which said additional data is days of the week.

3. A digital electronic timepiece as claimed in Claim 1, in which said additional data is AM/PM.

4. A digital electronic timepiece as claimed in Claim 1, in which said relatively high frequency signal has a frequency of  $16 \times 2^n$  Hz, where n is an integer, and in which said frequency divider comprises a first circuit for reducing said frequency by a ratio of 5/8, and a second circuit for dividing the output of said first circuit by a ratio of  $1/2^n$ .

5. A digital electronic timepiece according to claim 1, in which said relatively high frequency signal has a frequency of  $1024 \times 2^n$  Hz, where n is an integer, and in which said frequency divider comprises a first circuit for reducing said frequency by a ratio of 125/128, and a second circuit for dividing the output of said first circuit by a ratio of  $1/2^n$ .

6. A digital electronic timepiece substantially as shown and described with reference to the accompanying drawings.

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The flip-flop 213 provides an output signal having a frequency of 8 Hz. The error for each 1/8 second is thus  $(128-125)/128$  or  $1/8 \times 3/128 = 0.3\%$  per second. If a 1/1000 second signal is not necessary, the error can be further reduced by 1/10 so as to obtain an error of 0.03% per second when counting in units of 1/100 second. Since in order to obtain a 1 second signal the information at terminal 217 is fed to 3 stages of divide-by 10(decimal) counters, the error for the 1 second signal is substantially reduced to 0 so that there is no cumulative error if measured over a long period of time. Accordingly, since the error is within an allowable tolerance of 0.03% for one second or less, it can be understood that this has sufficient practical value.

It can thus be appreciated that this embodiment of the present invention makes it possible to produce a 1/100 second resolvable signal from a crystal controlled oscillator which oscillates at a frequency of  $2^p$ . This has a wide application in electronic timepiece and is particularly suited to a stop-watch function for a wristwatch.

It will now be appreciated from the foregoing description that since a plurality of segments of a band of segments are arranged to be displayed as a group, it is possible to read time in units of 1/10 second even in a case in which the response speed of a liquid crystal display device is slow.

While the present invention has been shown and described with reference to particular embodiments by way of example, it should be noted that any other modifications or changes may be made without departing from the scope of the present invention.

WHAT WE CLAIM IS:-

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an oscillator circuit providing a relatively high frequency signal; a frequency divider dividing down the relatively high frequency signal to provide a first low frequency signal at 1 Hz and a second low frequency signal higher in frequency than the first low frequency signal;  
a first counter responsive to the first low frequency signal to provide time of day and calendar information signals and an additional time data signal;  
a second counter responsive to the second low frequency signal to provide output signals indicating elapsed time in fractions of a second;  
first display means for displaying time and calendar data in response to the time and calendar information signals;  
second display means composed of a plurality of display segments for displaying elapsed time data; said segments being activated in step-wise fashion in response to the output signals from the second counter, said display segments serving also as means for displaying the additional time data; and  
switching means for enabling said second display means to display said additional data.

2. A digital electronic timepiece as claimed in Claim 1, in which said additional data is days of the week.

3. A digital electronic timepiece as claimed in Claim 1, in which said additional data is AM/PM.

4. A digital electronic timepiece as claimed in Claim 1, in which said relatively high frequency signal has a frequency of  $16 \times 2^n$  Hz, where n is an integer, and in which said frequency divider comprises a first circuit for reducing said frequency by a ratio of 5/8, and a second circuit for dividing the output of said first circuit by a ratio of  $1/2^n$ .

5. A digital electronic timepiece according to claim 1, in which said relatively high frequency signal has a frequency of  $1024 \times 2^n$  Hz, where n is an integer, and in which said frequency divider comprises a first circuit for reducing said frequency by a ratio of 125/128, and a second circuit for dividing the output of said first circuit by a ratio of  $1/2^n$ .

6. A digital electronic timepiece substantially as shown and described with reference to the accompanying drawings.

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