ABSTRACT OF THE DISCLOSURE

BALANCING NFET AND PFET PERFORMANCE USING STRAINING LAYERS

An integrated circuit structure includes a substrate and at least one pair of complementary transistors on or in the substrate. The pair of complementary transistors comprises a first transistor and a second transistor. The structure also includes a first stress-producing layer on the first transistor and the second transistor, and a second stress-producing layer on the first stress-producing layer over the first transistor and the second transistor. The first stress-producing layer applies tensile strain force on the first transistor and the second transistor. The second stress-producing layer applies compressive strain force on the first stress-producing layer, the first transistor, and the second transistor.

Fig. 3