What is Claimed is:

1. A method of forming an integrated circuit device, comprising:

forming an integrated circuit substrate having an electrically insulating layer thereon;

forming a mask layer pattern having at least first and second openings of different size therein, on the electrically insulating layer;

simultaneously etching first and second portions of the electrically insulating layer extending opposite the first and second openings, respectively, at first and second different etch rates that yield a first trench extending adjacent the first opening that is deeper than a second trench extending adjacent the second opening; and then

simultaneously etching the first and second trenches to substantially the same depths using an etching process that compensates for the first and second different etch rates associated with etching the first and second portions of the electrically insulating layer.

2. The method of Claim 1, wherein simultaneously etching first and second portions of the electrically insulating layer comprises exposing the first and second portions of the electrically insulating layer to an etching gas comprising C_xF_y, where $2x \geq y$, $x>0$ and $y>0$.

3. The method of Claim 2, wherein simultaneously etching the first and second trenches comprises exposing the first and second trenches to an etching gas comprising $C_{x'}F_{y'}$, where $2x' \leq y'$, $x'>0$ and $y'>0$.

4. The method of Claim 2, wherein simultaneously etching the first and second trenches comprises exposing the first and second trenches to an etching gas comprising $C_{x'}H_zF_{y'}$, where $2x' \leq y'$, $x'>0$, $y'>0$ and $z>0$.

5. The method of Claim 1, wherein simultaneously etching the first and second trenches comprises exposing the first and second trenches to an etching gas comprising $C_{x'}F_{y'}$, where $x' \leq y'$, $x'>0$ and $y'>0$.

~~6. The method of Claim 5, wherein the etching gas comprises $C_xH_zF_y$.~~

7. The method of Claim 1, wherein simultaneously etching first and second portions of the electrically insulating layer comprises exposing the first and second portions of the electrically insulating layer to an etching gas selected from a group consisting of C_4F_8, C_4F_6 and C_5F_8.

8. The method of Claim 7, wherein the etching gas further comprises argon and oxygen.

9. The method of Claim 2, wherein hydrogen is absent from the etching gas.

10. The method of Claim 6, wherein simultaneously etching the first and second trenches comprises exposing the first and second trenches to an etching gas selected from a group consisting of CH_2F_2 and CHF_3.

11. The method of Claim 5, wherein simultaneously etching the first and second trenches comprises exposing the first and second trenches to an etching gas selected from a group consisting of CF_4.

12. A method of forming an integrated circuit device, comprising:

forming a mask layer pattern having at least first and second openings of different size therein, on an electrically insulating layer;

simultaneously etching first and second portions of the electrically insulating layer extending opposite the first and second openings, respectively, at first and second different etch rates that yield a first trench extending adjacent the first opening that is deeper than a second trench extending adjacent the second opening; and then

simultaneously etching bottoms of the first and second trenches at different rates using an etching process that compensates for the first and second different etch rates associated with etching the first and second portions of the electrically insulating layer.

13. The method of Claim 12, wherein simultaneously etching first and second portions of the electrically insulating layer comprises exposing the first and second portions of the electrically insulating layer to an etching gas comprising C_xF_y, where $2x \geq y$, $x>0$ and $y>0$.

14. The method of Claim 13, wherein simultaneously etching the first and second trenches comprises exposing the first and second trenches to an etching gas comprising $C_{x'}F_{y'}$, where $2x' \leq y'$, $x'>0$ and $y'>0$.

15. The method of Claim 13, wherein simultaneously etching the first and second trenches comprises exposing the first and second trenches to an etching gas comprising $C_{x'}H_zF_{y'}$, where $2x' \leq y'$, $x'>0$, $y'>0$ and $z>0$.

16. The method of Claim 12, wherein simultaneously etching first and second portions of the electrically insulating layer comprises exposing the first and second portions of the electrically insulating layer to an etching gas selected from a group consisting of C_4F_8, C_4F_6 and C_5F_8.

17. A method of fabricating a semiconductor integrated circuit device, the method comprising:

providing a semiconductor substrate which is defined into a first region and a second region;

forming a low dielectric constant insulating layer on the semiconductor substrate;

forming a first mask layer pattern having a first opening on the low dielectric constant insulating layer of the first region and forming a second mask layer pattern having a second opening, which is wider than the first opening, on the low dielectric constant insulating layer of the second region;

performing a first etching process, in which the low dielectric constant insulating layer is etched using the first and second mask layer patterns as etching masks, to form a first trench in the low dielectric constant insulating layer exposed by the first opening and a second trench in the low dielectric constant insulating layer

exposed by the second opening wherein an etching speed of the first trench is controlled to be faster than that of the second trench; and

performing a second etching process, in which the first and second trenches are formed deeper, using the first and second mask layer patterns as the etching masks wherein the etching speed of the second trench is controlled to be faster than that of the first trench.

18. The method of Claim17, wherein the first and second trenches formed in the first and second etching processes have substantially equal depths.

19. The method of Claim 17, wherein the first trench is formed deeper than the second trench in the first etching process.

20. The method of Claim 17, wherein the first etching process is performed using an etching gas which comprises C_xF_y where $2x \geq y$, $x>0$ and $y>0$.

21. The method of Claim 20, wherein the first etching process is performed using an etching gas which comprises at least one of C_4F_8, C_4F_6, and C_5F_8.

22. The method of Claim 17, wherein the first etching process is performed using an etching gas which does not comprise hydrogen.

23. The method of Claim 17, wherein the second etching process is performed using an etching gas which comprises $C_aH_bF_c$.

24. The method of Claim 23, wherein the etching gas further comprises C_dF_e where $d \leq e$.

What is claimed is:

1. A method of forming an integrated circuit device, comprising:

forming an integrated circuit substrate having an electrically insulating layer thereon;

forming a mask layer pattern having at least first and second openings of different size therein, on the electrically insulating layer;

simultaneously etching first and second portions of the electrically insulating layer extending opposite the first and second openings, respectively, at first and second different etch rates that yield a first trench extending adjacent the first opening that is deeper than a second trench extending adjacent the second opening, by exposing the first and second portions of the electrically insulating layer to an etching gas comprising C_xF_y, where $2x \geq y$, $x>0$ and $y>0$; and then

simultaneously etching the first and second trenches to substantially the same depths using an etching process that compensates for the first and second different etch rates associated with etching the first and second portions of the electrically insulating layer, said etching process comprising exposing the first and second trenches to an etching gas comprising $C_{x'}F_{y'}$, where $2x' \leq y'$, $x'>0$ and $y'>0$;

wherein a first width of the first openings is smaller than a second width of the second openings.

2. The method of Claim 1, wherein simultaneously etching the first and second trenches comprises exposing the first and second trenches to an etching gas selected from a group consisting of CF_4.

3. A method of forming an integrated circuit device, comprising:

forming a mask layer pattern having at least first and second openings of different size therein, on an electrically insulating layer;

simultaneously etching first and second portions of the electrically insulating layer extending opposite the first and second openings, respectively, at first and second different etch rates that yield a first trench extending adjacent the first opening that is deeper than a second trench extending adjacent the second opening, by exposing the first and second portions of the electrically insulating layer to an etching gas comprising C_xF_y, where $2x \geq y$, $x>0$ and $y>0$; and then

simultaneously etching bottoms of the first and second trenches at different rates using an etching process that compensates for the first and second different etch rates associated with etching the first and second portions of the electrically insulating layer, said etching process comprising exposing the first and second trenches to an etching gas comprising $C_{x'}F_{y'}$, where $2x' \leq y'$, $x'>0$ and $y'>0$;

wherein a first width of the first openings is smaller than a second width of the second openings.

4. A method of forming an integrated circuit device, comprising:

forming an integrated circuit substrate having an electrically insulating layer thereon;

forming a mask layer pattern having at least first and second openings of different size therein, on the electrically insulating layer, wherein a first width of the first openings is smaller than a second width of the second openings;

simultaneously etching first and second portions of the electrically insulating layer extending opposite the first and second openings, respectively, at first and second different etch rates that yield a first trench extending adjacent the first opening that is deeper than a second trench extending adjacent the second opening; and then

simultaneously etching the first and second trenches to substantially the same depths using an etching process that compensates for the first and second different etch rates associated with etching the first and second portions of the electrically insulating layer.