

SUBSTRATE BACKSIDE TEXTURING

[0001] This application claims priority to U.S. Non-Provisional Patent Application No. 14/833,044, filed August 22, 2015, the contents of which is incorporated herein by reference in its entirety.

[0002] In order to expose a semiconductor substrate during manufacture of an integrated circuit (IC), the substrate may be chucked on an imaging scanner or camera. During chucking, the wafer can be thought of as a “pancake” that is able to “wrinkle”, resulting in significant distortion of images projected onto the wafer. This impacts overall performance when aligning multiple lithographic layers in integrated circuit manufacturing.

[0003] Embodiments described herein relate to a method and apparatus for reducing lithographic distortion. A backside of a semiconductor substrate may be texturized. Then a lithographic process may be performed on the semiconductor substrate having the texturized backside.

[0003a] According to a first aspect, there is provided a method for determining backside texturing of a semiconductor substrate that is processed on a photolithography tool, including: determining one or more contact areas on the photolithography tool for the semiconductor substrate; determining a backside surface texturing for the semiconductor substrate that is based, at least in part, on: a frequency of backside features of the semiconductor substrate at one or more portions of the semiconductor substrate, an amplitude of the backside features at the one or more portions of the semiconductor substrate, or a size of the one or more contact areas; and processing the semiconductor substrate to obtain a target backside surface texturing that reduces the coefficient of friction between the substrate and the one or more contact areas.

[0003b] According to a second aspect, there is provided a method of reducing lithographic distortion including: texturizing a backside of a semiconductor substrate; and performing a lithographic process on the semiconductor substrate having the texturized backside with a lithographic tool which supports the substrate at one or more contact areas, the texturing reducing the coefficient of friction between the backside and the one or more contact areas.

[0004] A detailed description of several embodiments will now be provided, taken in conjunction with the accompanying drawings, of which:

[0005] FIG. 1 is a simplified diagram of chuck pins and a semiconductor substrate;

[0006] FIG. 2 is a schematic illustration of a process according to an embodiment;

[0007] FIG. 3 is a schematic diagram of apparatus according to an embodiment;

[0008] FIG. 4 is a chart illustrating semiconductor substrate materials and corresponding etchants;

[0009] FIG. 5 is a schematic illustration of apparatus according to an embodiment;

[0010] FIG. 6 is a schematic illustration of a process according to an embodiment; and

[0011] FIG. 7 is a schematic illustration of roughness associated with a backside of a semiconductor substrate.

[0012] Typically in IC manufacturing, the backside of semiconductor substrates may be contaminated during processing. The contamination may include residual films and organic and inorganic particles. Such contamination may result from many steps in the manufacturing process such as thermal material growth, e.g., growing SiN or SiO₂ films, photoresist processing, rapid thermal annealing and/or chemical vapor deposition (CVD). In addition, the backside substrate surface may also become