A problem arises from the fact that such a circuit is not symmetrical. Indeed both branches may have different designs concerning dimensions of the respective transistors (T1 being compared to T4, and T2 being compared to T3). Moreover, the first and second nodes N1, N2 are operated in a different manner and with different loads (with nodes N1 and N2 being either both inputs or both outputs). Moreover, the operating points of all transistors may usually differ from each other during the sensing process (once again T1 is compared to T4, and T2 to T3). Thus for ensuring proper operation of the circuit, widths and lengths of the transistors must be thoroughly designed (and T1 and T4, respectively T2 and T3, may intentionally differ). Reference, bias and supply voltage must also be well defined and well controlled.

In practice however, all these parameters and the transistor properties (current drive capability, threshold voltage, transconductance, drain conductance, etc.) are prone to variations (PVT: process, voltage, temperature). As the single-ended sense amplifier is a non-symmetrical circuit, PVT induced variations do not compensate for each other in the two branches and malfunction of the circuit may result.

SUMMARY OF THE INVENTION

The invention aims to provide a single-ended sense amplifier which is not prone to PVT variations.

In this respect, the invention relates, according to its first aspect, to a semiconductor memory device comprising:

- a single-ended sense amplifier circuit for reading data sensed from selected memory cells in a memory array, the sense amplifier having a first node used to feed in a reference signal, a second node coupled to a bit line, and sense transistors responsible for amplifying the content of a selected memory cell during a sense operation,
- a reference circuit having replica transistors of the sense transistors and further comprising a regulation network designed so that each replica transistor operates in a stable operating point, and wherein the regulation network generates a control voltage which is applied to the sense amplifier circuit;

wherein the sense amplifier circuit and the reference circuit each have first and second circuit branches, each of said branches having at least one first transistor of a first conductivity type and a second transistor of a second conductivity type connected in series, wherein the second transistor of each branch of the sense amplifier circuit is a sense transistor and wherein the second transistor of each branch of the reference circuit is a replica transistor of the second transistor of each branch of the sense amplifier; and

wherein the regulation network of the reference circuit comprises a first regulation loop designed to maintain the drain voltage of the replica transistor of the second branch in the reference circuit at a voltage level corresponding to the voltage level on the data line at the onset of a sense operation under condition that the voltage sensed on the bit line at the onset of a sense operation corresponds to the mean value between the voltage which would be sensed on the bit line from a logical "1" stored within the selected memory cell and the voltage which would be sensed on the bit line from a logical "0" stored within the selected memory cell.

Other preferred, although non limitative, embodiments of this memory device are as follows:

- the regulation network of the reference circuit is designed to set the operating point of each replica transistor equal to the operating point of the respective sense transistor at the onset of a sense operation of a selected memory cell performed by the sense amplifier circuit, said operating point at the onset of a sense operation being defined under condition that the voltage sensed on the bit line corresponds to the mean value between the voltage

which would be sensed on the bit line if a logical "1" were stored within the selected memory cell and the voltage which would be sensed on the bit line if a logical "0" were stored within the selected memory cell;

- the control voltage generated by the regulation network is applied to one terminal of a replica transistor in the reference circuit and to the respective terminal of the respective sense transistor in the sense amplifier circuit;

~~- the sense amplifier circuit and the reference circuit each have first and second circuit branches, each of said branches having at least one first transistor of a first conductivity type and a second transistor of a second conductivity type connected in series, wherein the second transistor of each branch of the sense amplifier circuit is a sense transistor and wherein the second transistor of each branch of the reference circuit is a replica transistor of the second transistor of each branch of the sense amplifier;~~

~~- the regulation network of the reference circuit comprises a first regulation loop designed to maintain the drain voltage of the replica transistor of the second branch in the reference circuit at a voltage level corresponding to the voltage level on the data line at the onset of a sense operation;~~

- the sense transistors and the replica transistors are double gate transistors having first and second control gates, and the regulation network of the reference circuit comprises a second regulation loop designed to drive the second control gate of the replica transistor of the first branch so that the current ratio between the replica transistor of the first branch and the replica transistor of the second branch is equal to the current ratio between the sense transistor of the first branch and the sense transistor of the second branch at the onset of a sense operation;

- the second regulation loop generates a control voltage which is applied to the second control gate of the replica transistor of the first branch of the reference circuit and to the second control gate of the sense transistor of the second branch of the sense amplifier circuit;

- the at least one first transistors of a first conductivity type in the branches of the reference circuit are arranged so as to form a current mirror;

- the replica transistors have the same lengths as the corresponding sense transistors and the same width ratio;

- it has a plurality of sense amplifier circuits arranged as stripes (STSA) of sense amplifier circuits.

CLAIMS

1. A semiconductor memory device comprising:

- a single-ended sense amplifier circuit for reading data sensed from selected memory cells in a memory array, the sense amplifier having a first node used to feed in a reference signal, a second node coupled to a bit line, and sense transistors responsible for amplifying the content of a selected memory cell during a sense operation,
- a reference circuit having replica transistors of the sense transistors and further comprising a regulation network designed so that each replica transistor operates in a stable operating point, and wherein the regulation network generates a control voltage which is applied to the sense amplifier circuit;

wherein the sense amplifier circuit and the reference circuit each have first and second circuit branches, each of said branches having at least one first transistor of a first conductivity type and a second transistor of a second conductivity type connected in series, wherein the second transistor of each branch of the sense amplifier circuit is a sense transistor and wherein the second transistor of each branch of the reference circuit is a replica transistor of the second transistor of each branch of the sense amplifier; and

wherein the regulation network of the reference circuit comprises a first regulation loop designed to maintain the drain voltage of the replica transistor of the second branch in the reference circuit at a voltage level corresponding to the voltage level on the data line at the onset of a sense operation under condition that the voltage sensed on the bit line at the onset of a sense operation corresponds to the mean value between the voltage which would be sensed on the bit line from a logical "1" stored within the selected memory cell and the voltage which would be sensed on the bit line from a logical "0" stored within the selected memory cell.

2. The semiconductor memory device of claim 1, wherein the regulation network of the reference circuit is designed to set the operating point of each replica transistor equal to the operating point of the respective sense transistor at the onset of a sense operation of a selected memory cell performed by the sense amplifier circuit, said operating point at the onset of a sense operation being defined under condition that the voltage sensed on the bit line corresponds to the mean value between the voltage which would be sensed on the bit

line if a logical "1" were stored within the selected memory cell and the voltage which would be sensed on the bit line if a logical "0" were stored within the selected memory cell.

3. The semiconductor memory device of claim 1, wherein the control voltage generated by the regulation network is applied to one terminal of a replica transistor in the reference circuit and to the respective terminal of the respective sense transistor in the sense amplifier circuit.

~~4. The semiconductor memory device of claim 1, wherein the sense amplifier circuit and the reference circuit each have first and second circuit branches, each of said branches having at least one first transistor of a first conductivity type and a second transistor of a second conductivity type connected in series, wherein the second transistor of each branch of the sense amplifier circuit is a sense transistor and wherein the second~~

~~transistor of each branch of the reference circuit is a replica transistor of the second transistor of each branch of the sense amplifier.~~

~~5. The semiconductor memory device of claim 4, wherein the regulation network of the reference circuit comprises a first regulation loop designed to maintain the drain voltage of the replica transistor of the second branch in the reference circuit at a voltage level corresponding to the voltage level on the data line at the onset of a sense operation under condition that the voltage sensed on the bit line at the onset of a sense operation corresponds to the mean value between the voltage which would be sensed on the bit line from a logical "1" stored within the selected memory cell and the voltage which would be sensed on the bit line from a logical "0" stored within the selected memory cell.~~

~~6~~4. The semiconductor memory device of claim ~~5~~1, wherein the sense transistors and the replica transistors are double gate transistors having first and second control gates, and wherein the regulation network of the reference circuit comprises a second regulation loop designed to drive the second control gate of the replica transistor of the first branch so that the current ratio between the replica transistor of the first branch and the replica transistor of the second branch is equal to the current ratio between the sense transistor of the first branch and the sense transistor of the second branch at the onset of a sense operation under condition that the voltage sensed on the bit line corresponds to the mean value between the voltage which would be sensed on the bit line from a logical "1" stored within the selected memory cell and the voltage which would be sensed on the bit line from a logical "0" stored within the selected memory cell.

~~7~~5. The semiconductor memory device of claim ~~6~~4, wherein the second regulation loop generates a control voltage which is applied to the second control gate of the replica transistor of the first branch of the reference circuit and to the second control gate of the sense transistor of the second branch of the sense amplifier circuit.

~~8~~6. The semiconductor memory device of any one of claims ~~4-7~~1 to 5, wherein the at least one first transistors of a first conductivity type in the branches of the reference circuit are arranged so as to form a current mirror.

~~9~~7. The semiconductor memory device of any one of claims ~~4-8~~1 to 6, wherein the replica transistors have the same lengths as the corresponding sense transistors and the same width ratio.

~~10~~8. The semiconductor memory device of any one of claims ~~1-9~~1 to 7 having a plurality of sense amplifier circuits arranged as stripes of sense amplifier circuits.

~~11~~9. A semiconductor memory comprising a semiconductor memory device according to any one of claims ~~1-10~~1 to 8.

~~12~~10. A process of operating a semiconductor memory device according to any one of claims ~~1-10~~1 to 8, comprising the steps of:

- operating each replica transistor in a stable operating point,
- generating a control voltage in the reference circuit and applying said control voltage to the sense amplifier circuit.