Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a carrier;

providing a substrate;

forming a ~~plurality of first contact pads~~ first conductive layer over a first surface of the substrate;

forming a second conductive layer over a second surface of the substrate, the second conductive layer including a dummy pattern to approximately balance the second conductive layer with the first conductive layer;

~~forming a plurality of second contact pads over a second surface of the substrate; and~~

~~forming a dummy pattern over the second surface of the substrate~~ disposing the substrate on the carrier;

disposing a semiconductor die on the carrier laterally offset from the substrate; and

depositing an encapsulant over the carrier between a side surface of the semiconductor die and a side surface of the substrate that opposes the side surface of the semiconductor die.

2. The method of claim 1, further including forming an indentation in a sidewall of the substrate.

3. The method of claim 1, further including forming an opening through the substrate.

4. The method of claim 3, further including depositing an encapsulant in the opening of the substrate.

5. The method of claim 1, further including:

~~disposing a semiconductor die adjacent to the substrate;~~ ~~and~~

~~depositing an encapsulant over the semiconductor die and substrate~~ forming an insulating layer over the second surface of the substrate; and

forming a dummy opening in the insulating layer.

6. ~~A method of making a semiconductor device, comprising:~~

~~providing a substrate;~~

~~forming a first conductive layer over a first surface of the substrate; and~~

~~forming a dummy pattern over a second surface of the substrate~~ The method of claim 1, wherein the first surface of the substrate includes a width that is greater than a width of the second surface of the substrate.

~~7. The method of claim 6, further including forming an indentation in a sidewall of the substrate.~~

~~8. The method of claim 6, further including forming an opening through the substrate.~~

~~9. The method of claim 6, further including:~~

~~forming an insulating layer over the second surface of the substrate; and~~

~~forming a dummy opening in the insulating layer.~~

~~10. The method of claim 6, wherein the first surface of the substrate includes a width that is greater than a width of the second surface of the substrate.~~

~~11~~7. A semiconductor device, comprising:

a carrier;

a substrate disposed on the carrier, the substrate including,~~:~~

a first conductive layer formed over a first surface of the substrate~~:~~, and

~~a dummy pattern formed over a second surface of the substrate~~ a second conductive layer formed over a second surface of the substrate, the second conductive layer including a dummy

pattern to approximately balance the second conductive layer with the first conductive layer;

a semiconductor die disposed on the carrier laterally offset from the substrate; and

an encapsulant deposited over the carrier between a side surface of the semiconductor die and a side surface of the substrate that opposes the side surface of the semiconductor die.

~~12~~8. The semiconductor device of claim ~~11,~~7 wherein a sidewall of the substrate includes an indentation.

~~13~~9. The semiconductor device of claim ~~11~~7, wherein the substrate includes an opening.

1~~4~~0. The semiconductor device of claim ~~13~~9, ~~further including an~~ wherein the encapsulant is disposed in the opening of the substrate.

1~~5~~1. The semiconductor device of claim ~~11~~7, wherein the first surface of the substrate includes a width greater than a width of the second surface of the substrate.

12. A semiconductor device, comprising:

a substrate including a conductive via formed through the substrate;

a first conductive layer formed over a first surface area of a first surface of the substrate including over the conductive via;

a second conductive layer formed over a second surface area of a second surface of the substrate including over the conductive via;

a dummy conductive pattern formed over a third surface area of the first surface of the substrate, wherein a sum of the first surface area and third surface area is approximately equal to the second surface area;

a first insulating layer formed over the first surface of the substrate with an opening in the first insulating layer over the first conductive layer; and

a second insulating layer formed over the second surface of the substrate with a first opening in the second insulating layer over the second conductive layer and a dummy opening in the second insulating layer outside a footprint of the second

conductive layer, wherein the dummy opening is configured to balance a first weight of the first insulating layer with a second weight of the second insulating layer.

13. The semiconductor device of claim 12, wherein a sidewall of the substrate includes an indentation.

14. The semiconductor device of claim 12, wherein the substrate includes an opening.

15. The semiconductor device of claim 14, further including an encapsulant disposed in the opening of the substrate.

16. The semiconductor device of claim 12, wherein the substrate includes a molding compound.

17. The semiconductor device of claim 12, further including:
a semiconductor die disposed adjacent to the substrate; and
an encapsulant deposited between opposing side surfaces of the semiconductor die and substrate.

18. A semiconductor device, comprising:
a substrate;
a plurality of first contact pads formed over a first surface of the substrate;
a plurality of second contact pads formed over a second surface of the substrate; and
a dummy pattern formed over the second surface of the substrate, wherein an area of the first surface covered by the first contact pads is approximately equal to an area of the

second surface covered by the second contact pads plus an area of the dummy pattern.

19. The semiconductor device of claim 18, wherein a sidewall of the substrate includes an indentation.

20. The semiconductor device of claim 18, further including an opening through the substrate.

21. The semiconductor device of claim 20, further including an encapsulant disposed in the opening of the substrate.

22. The semiconductor device of claim 18, further including an insulating layer formed over the second surface of the substrate with a dummy opening in the insulating layer.

23. The semiconductor device of claim 18, further including:
a semiconductor die disposed adjacent to the substrate; and
an encapsulant disposed over the semiconductor die and substrate.