

Description

The present invention relates to a passive optical network, and in particular to the recovery of information from signals transmitted from terminations to a head-end station in such a network.

The present applicant has developed a bit transport system (BTS) for use in a TPO (telephony on a passive optical network) network. In this BTS a head-end station broadcasts time division multiple access (TDMA) frames to all the terminations on the network. The transmitted frames include both traffic data and control data. Each termination recognises and responds to an appropriately addressed portion of the data in the broadcast frame and ignores the remainder of the frame. The BTS is described in greater detail in WO-A-89/05070 and WO-A-88/09093.

In the upstream direction, each termination transmits data in a predetermined time slot, and the data from the different terminations are assembled at the head-end into a TDMA frame of predetermined format.

One feature necessary to such a network is the provision of compensation for the differing delays and attenuation associated with the different distances of the various terminations from the head-end station. To this end, in the BTS each termination is arranged to transmit a ranging pulse timed to arrive in a respective predetermined portion of the upstream TDMA frame. The head-end station is arranged to monitor the timing, i.e. phase and amplitude of the arrival of the pulse from each of the terminations and to return a servo-control signal to the termination to retard or advance its transmissions as appropriate and to adjust the launch power. This active fine ranging enables the BTS to ensure stability of the upstream TDMA frame and, for example, to compensate for fluctuations in timing and received power due to such effects as changes in the operating temperature of the network. However this places severe demands on the design of the head-end station, requiring the measurement of the timing of received signals to within a fraction of a clock cycle and amplitude to within a fraction of a dB in real time.

The present invention provides a method of operating a passive optical network including a head-end station and a plurality of terminations, the terminations being responsive to control signals from the head-end station, and the head-end station being arranged to receive frames having a predetermined bit rate and comprising signals transmitted by the plurality of terminations, the method comprising the steps of transmitting respective ranging pulses from the terminations to the head-end station, sampling the received ranging pulses and producing corresponding data samples, applying the data samples to processor means arranged to determine the respective phases of the ranging pulses relative to respective expected

values and to determine the respective amplitudes of the ranging pulses, and generating respective control signals for the terminations to modify the phase and amplitude of transmissions from the terminations accordingly, characterised in that the received ranging pulses are sampled at a sampling rate greater than the predetermined bit rate.

By sampling the received ranging pulses at such a (high) sampling rate it is possible to capture the phase and amplitude information from a ranging pulse in a form which can be readily processed to provide the necessary control signals. At the same time, the sampling process effectively provides a snapshot of the received pulse, which carries information relating to the overall shape of the pulse. This further information can be used to implement other control and diagnostic procedures simply by the provision of appropriate additional software for the processor.

There is residual phase jitter in the TDMA data received at the head-end due to varying path lengths and clock jitter in the terminations. With the method of the present invention, this jitter may be used effectively to increase the phase resolution by providing additional sampling points on the sloped edges of the received ranging pulses. The waveform data is then integrated and processed by a CPU over a period of time.

Preferably, the method further comprises writing the data samples into a plurality of latches connected to a clock signal source arranged to clock the latches at a clock rate less than the sampling rate, the clock signal for each latch having a different respective phase offset, writing data samples from each latch into a respective serial memory, and reading data samples from the serial memories into the processor means.

Although a high sampling rate is necessary initially to capture all the required information from the ranging pulse, it is advantageous to convert the data samples to a lower bit rate, and in particular to the bit rate of the frames before it is access by the processor.

Preferably, the head-end station includes a masterclock operating at one of the clock or the sampling rate, a clock signal being derived from the masterclock at the other of the clock rate or the sampling rate, and the plurality of latches are latched on the leading edge of a pulse of the clock signal at the clock rate and the serial memories are latched on the trailing edge of said pulse.

In a preferred embodiment, the method further comprises the steps of superimposing on the receive frames at the head-end station a locally-generated marker pulse having a phase locked to a masterclock for the system, subsequently sampling a portion of the frame including the marker pulse to produce corresponding data samples, and applying the data samples to a control processor having its own local clock, the control processor being arranged to determine

parameters of received signals in the sampled portion of the frame relative to those of the marker pulse.

The invention also provides a head-end station for use in a passive optical network system and arranged to transmit control signals to a plurality of terminations, the terminations being responsive to control signals from the head-end station, and the head-end station being arranged to receive frames having a predetermined bit rate and comprising signals transmitted by the plurality of terminations, the head-end station including means to receive respective ranging pulses from the terminations, sampling means arranged to sample the received ranging pulses and produce corresponding data samples, processor means responsive to data samples and arranged to determine the respective phase of the ranging pulses relative to respective expected values and to determine the respective amplitudes of the ranging pulses, and control signal generating means arranged to generate respective control signals to modify the phase and amplitude of transmissions from respective terminations, characterised in that the sampling means is arranged to sample the received ranging pulses at a sampling rate greater than the predetermined bit rate.

Preferably, the head-end station further comprises a plurality of latches connected to a clock signal source arranged to clock the latches at a clock rate less than the sampling rate, the clock signal for each latch having a different respective phase offset, and a respective serial memory for each of the plurality of latches, data samples being written in use from each latch into the respective serial memory for each of the plurality of latches, data samples being written in use from each latch into the respective serial memory, and each serial memory being reset by a reset pulse having a corresponding respective phase offset, thereby converting the data samples from the sampling rate to the clock rate.

Preferably, the serial memories comprises dual port serial FIFOs.

Preferably, the head-end station further comprises marker means disposed upstream of the sampling means and arranged to superimpose a marker pulse of predetermined phase and amplitude on the received frames and thereby provide a reference for use by the processor means.

A passive optical network in accordance with the present invention will now be described in detail with reference to the accompanying drawings, in which: -

Figure 1 is a block diagram showing a TPON network;

Figure 2 is a diagram showing the structure of an upstream TDMA frame;

Figure 3 is a block diagram of a head-end station;

Figure 4 is a block diagram showing the input stage in greater detail;

Figure 5 is a block diagram showing the converter

of Figure 3 in greater detail; and

Figure 6 is a diagram showing the sampling of the ranging pulse.

ATPON network comprises a head-end station 1, a number of terminations 2, and a passive optical fibre network 3 linking the head-end station 1 to the terminations 2. Although, for clarity, only three terminations are shown, in practice many more terminations will be connected to a single head-end station. Typically the head-end station is located in a local exchange and the terminations 2 are subscriber stations in domestic or commercial premises or street cabinets in the neighbourhood of the local exchange.

The head-end station 1 broadcasts data over the fibre network 3 as time division multiple access (TDMA) frames having a predetermined format. The frames include control channels addressed to specific ones of the terminations 2 to control, amongst other parameters, the amplitude and phase (timing) of the optical signals transmitted onto the fibre network 3 by the terminations 2.

In the upstream direction, each termination 2 transmits data in a predetermined time slot, which data is assembled into a TDMA frame at the head-end station 1. Since the TPON network is synchronous in operation it is necessary to control the timing of the terminations both to compensate for the different delays associated with different positions of the terminations on the fibre network 3 and to correct for any variation in the delay and amplitude arising, for example, from local fluctuations in the temperature of the network.

Figure 2 shows the format of the return frame. Traffic data is transmitted to the head-end station in 80 basic frames BF1 to BF80. The basic frames BF1 to BF80 are preceded by a header H which includes a phase-2 ranging section R 720 bits long. Each termination 2 is arranged to transmit onto the fibre network 3 a ranging pulse timed to arrive at a respective predetermined position within the ranging section R. Using the circuit described in further detail below the head-end station 1 determines the phase of each arriving ranging pulse relative to the respective predetermined positions of the ranging pulses within the ranging section R, and then transmits control signals to the respective termination 2 to retard or advance the timing of the transmission from that termination 2 in order to minimize the phase offset between the received data from that termination and the intended position of that data within the return frame structure.

Figure 3 shows the structure of the head-end station 1. The incoming optical signals are received by an input stage 4 which includes a conventional photoelectric detector followed by a linear gain block A. The output from the input stage 4 is branched, going both to a signal recovery stage 5 and to an A/D sampler 6. The sampler 6 operates under the control of a CPU 7 to sample any selected portion of the incoming sig-

nals. In the present example, the sampler 6 is arranged to sample the portion R of the incoming frame containing the ranging pulses and produce corresponding samples in the form of 8-bit data words (the data). The output from the sampler 6 is taken to a converter 8 which converts the data to the lower clock rate of a masterclock for the head-end station. The CPU 7 calculates from the data the phase and amplitude of the ranging pulses. These parameters are compared with expected values and, where necessary, control signals generated for a corresponding termination 2 to retard or advance the timing of transmissions from the termination 2 to minimize the phase offset, and/or to increase or reduce the amplitude of the transmissions until the received ranging pulse from that termination 2 has an amplitude falling within predetermined limits.

Figure 5 shows the converter in greater detail. The high-speed sampler 6 provides an input to the converter 8 comprising 8-bit data words having a clock rate, in the present example, of 81.92 MHz. The input to the converter 8 is fed in parallel to four 8-bit latches L. The latches L are locked to the masterclock with differing phase offsets of 0°, 90°, 180° and 270° respectively. The output from each latch is fed to a 8-bit dual port serial FIFO of the type known as a video line memory VLM. In order to ensure that the data written to the video line memories is correctly ordered the memories are reset by pulses having a predetermined phase with respect to the write clock. The write clock and reset pulses with appropriate phases are derived from respective shift registers, as shown in Figure 5. The video line memories VLM are polled consecutively by the CPU 7 so that the data received at the converter 8 as four 8-bit data words with a clock rate of substantially 80 MHz are read into the CPU as a single 32-bit word at a lower clock rate of substantially 20 MHz. A write gate signal having the same periodicity as the received TDMA frames is applied to the write enable inputs WE of the video line memories. The write gate is used to select the portion of the TDMA frame which is written into the video line memories.

The head-end station 1 includes a masterclock operating at the lower clock rate and the components of the head-end station, together with the rest of the TPN system are locked to the masterclock. In an alternative arrangement, the head-end station includes a clock operating at the high sampling rate of substantially 80 MHz and the 20 MHz system clock is derived from the 80 MHz clock. However, although the control systems provided for the head-end station and the network ensure that operation is synchronous at the system clock rate it is not possible to provide similarly synchronous operation at the higher clock rate used in the high-speed sampler. This rate is four times the masterclock rate in order to capture the necessary phase and amplitude information from the ranging

pulse. In order to provide the phase reference required at the higher sampling rate a marker pulse is superimposed on the incoming data upstream of the high-speed sampler 6.

As shown in Figure 4 the input stage includes a marker pulse generator 9, a photodetector 11 and a summing amplifier 10. The marker pulse generator 9 produces a marker pulse having a phase locked to the masterclock. The marker pulse is locally summed with the analogue input signal at the summing amplifier 10 and so appears in the data output from the sampler 6. The CPU 7 then detects the phase of a given sampled ranging pulse with respect to the marker pulse and compares this with the expected value to determine the appropriate phase control signal. Similarly, the marker pulse provides an amplitude reference for use by the CPU 7. The CPU 7 includes its own asynchronous clock. The execution of the CPU program is synchronised using 10mS interrupts (the TDMA frame rate) and data is read from the VLMs at a rate much lower than the system clock, controlled by the interrupts.

Claims

1. A method of operating a passive optical network (3) including a head-end station (1) and a plurality of terminations (2), the terminations being responsive to control signals from the head-end station, and the head-end station being arranged to receive frames having a predetermined bit rate and comprising signals transmitted by the plurality of terminations, the method comprising the steps of transmitting respective ranging pulses from the terminations to the head-end station, characterized by sampling the received ranging pulses and producing corresponding data samples, applying the data samples to processor means (7) arranged to determine the respective phases of the ranging pulses relative to respective expected values and to determine the respective amplitudes of the ranging pulses, and generating respective control signals for the terminations to modify the phase and amplitude of transmissions from the terminations accordingly, whereby the received ranging pulses are sampled at a sampling rate greater than the predetermined bit rate.
2. A method according to claim 1, further comprising the steps of writing the data samples into a plurality of latches (L) connected to a clock signal source arranged to clock the latches at a clock rate less than the sampling rate, the clock signal for each latch having a different respective phase offset, writing data samples from each latch into a respective serial memory (VLM), and reading

nals. In the present example, the sampler 6 is arranged to sample the portion R of the incoming frame containing the ranging pulses and produce corresponding samples in the form of 8-bit data words (the data). The output from the sampler 6 is taken to a converter 8 which converts the data to the lower clock rate of a masterclock for the head-end station. The CPU 7 calculates from the data the phase and amplitude of the ranging pulses. These parameters are compared with expected values and, where necessary, control signals generated for a corresponding termination 2 to retard or advance the timing of transmissions from the termination 2 to minimize the phase offset, and/or to increase or reduce the amplitude of the transmissions until the received ranging pulse from that termination 2 has an amplitude falling within predetermined limits.

Figure 5 shows the converter in greater detail. The high-speed sampler 6 provides an input to the converter 8 comprising 8-bit data words having a clock rate, in the present example, of 81.92 MHz. The input to the converter 8 is fed in parallel to four 8-bit latches L. The latches L are locked to the masterclock with differing phase offsets of 0°, 90°, 180° and 270° respectively. The output from each latch is fed to a 8-bit dual port serial FIFO of the type known as a video line memory VLM. In order to ensure that the data written to the video line memories is correctly ordered the memories are reset by pulses having a predetermined phase with respect to the write clock. The write clock and reset pulses with appropriate phases are derived from respective shift registers, as shown in Figure 5. The video line memories VLM are polled consecutively by the CPU 7 so that the data received at the converter 8 as four 8-bit data words with a clock rate of substantially 80 MHz are read into the CPU as a single 32-bit word at a lower clock rate of substantially 20 MHz. A write gate signal having the same periodicity as the received TDMA frames is applied to the write enable inputs WE of the video line memories. The write gate is used to select the portion of the TDMA frame which is written into the video line memories.

The head-end station 1 includes a masterclock operating at the lower clock rate and the components of the head-end station, together with the rest of the TPON system are locked to the masterclock. In an alternative arrangement, the head-end station includes a clock operating at the high sampling rate of substantially 80 MHz and the 20 MHz system clock is derived from the 80 MHz clock. However, although the control systems provided for the head-end station and the network ensure that operation is synchronous at the system clock rate it is not possible to provide similarly synchronous operation at the higher clock rate used in the high-speed sampler. This rate is four times the masterclock rate in order to capture the necessary phase and amplitude information from the ranging

pulse. In order to provide the phase reference required at the higher sampling rate a marker pulse is superimposed on the incoming data upstream of the high-speed sampler 6.

As shown in Figure 4 the input stage includes a marker pulse generator 9, a photodetector 11 and a summing amplifier 10. The marker pulse generator 9 produces a marker pulse having a phase locked to the masterclock. The marker pulse is locally summed with the analogue input signal at the summing amplifier 10 and so appears in the data output from the sampler 6. The CPU 7 then detects the phase of a given sampled ranging pulse with respect to the marker pulse and compares this with the expected value to determine the appropriate phase control signal. Similarly, the marker pulse provides an amplitude reference for use by the CPU 7. The CPU 7 includes its own asynchronous clock. The execution of the CPU program is synchronised using 10mS interrupts (the TDMA frame rate) and data is read from the VLMs at a rate much lower than the system clock, controlled by the interrupts.

Claims

1. A method of operating a passive optical network (3) including a head-end station (1) and a plurality of terminations (2), the terminations being responsive to control signals from the head-end station, and the head-end station being arranged to receive frames having a predetermined bit rate and comprising signals transmitted by the plurality of terminations, the method comprising the steps of transmitting respective ranging pulses from the terminations to the head-end station, characterized by sampling the received ranging pulses and producing corresponding data samples, applying the data samples to processor means (7) arranged to determine the respective phases of the ranging pulses relative to respective expected values and to determine the respective amplitudes of the ranging pulses, and generating respective control signals for the terminations to modify the phase and amplitude of transmissions from the terminations accordingly, whereby the received ranging pulses are sampled at a sampling rate greater than the predetermined bit rate.
2. A method according to claim 1, further comprising the steps of writing the data samples into a plurality of latches (L) connected to a clock signal source arranged to clock the latches at a clock rate less than the sampling rate, the clock signal for each latch having a different respective phase offset, writing data samples from each latch into a respective serial memory (VLM), and reading



data samples from the serial memories into the processor means.

3. A method according to claim 2, in which the clock rate is substantially the same as the bit rate of the received data frames. 5
4. A method according to claim 2 or claim 3, in which the head-end station includes a masterclock operating at one of the clock rate or the sampling rate, a clock signal being derived from the masterclock at the other of the clock rate or the sampling rate, and the plurality of latches are latched on the leading edge of a pulse of the clock signal at the clock rate and the serial memories are latched on the trailing edge of said pulse. 10 15
5. A method according to any one of claims 1 to 4, further comprising the steps of superimposing on the received frames at the head-end station a locally-generated marker pulse having a phase locked to a masterclock for the system, subsequently sampling a portion of the frame including a marker pulse to produce corresponding data samples, and applying the data samples to a control processor having its own local clock, the control processor being arranged to determine parameters of received signals in the sampled portion of the frame relative to those of the marker pulse. 20 25 30
6. A head-end station (1) for use in a passive optical network system (3) and arranged to transmit control signals to a plurality of terminations (2), the terminations being responsive to control signals from the head-end station, and the head-end station being arranged to receive frames having a predetermined bit rate and comprising signals transmitted by the plurality of terminations, the head-end station including means (4) to receive respective ranging pulses from the terminations, characterized by sampling means (6) arranged to sample the received ranging pulses and produce corresponding data samples, processor means (7) responsive to said data samples and arranged to determine the respective phase of the ranging pulses relative to respective expected values and to determine the respective amplitudes of the ranging pulses, and control signal generating means arranged to generate respective control signals to modify the phase and amplitude of transmissions from respective terminations, whereby the sampling means is arranged to sample the received ranging pulses at a sampling rate greater than the predetermined bit rate. 35 40 45 50 55
7. A head-end station according to claim 6, further comprising a plurality of latches (L) connected to a clock signal source arranged to clock the latch-

es at a clock rate less than the sampling rate, the clock signal for each latch having a different respective phase offset, and a respective serial memory (VLM) for each of the plurality of latches, data samples being written in use for each latch into the respective serial memory, and each serial memory being reset by a reset pulse having a corresponding respective phase offset, thereby converting the data samples from the sampling rate to the clock rate.

8. A head-end station according to claim 6 or claim 7, further comprising a masterclock operating at one of the clock rate or the sampling rate and means to derive from the masterclock a clock signal at the other of the clock rate or the sampling rate, and the plurality of latches (L) are latched on the leading edge of the pulse of the clock signal at the clock rate and the serial memories (VLM) are latched on the trailing edge of said pulse.
9. A head-end station according to claim 7, in which the serial memories (VLM) comprise dual port serial FIFOs.
10. A head-end station according to any one of claims 6 to 9, further comprising marker means (9) disposed upstream of the sampling means (6) and arranged to superimpose a marker pulse of predetermined phase and amplitude on the received frames and thereby provide a reference for use by the processor means (7).

Patentansprüche

1. Verfahren zum Betreiben eines passiven optischen Netzwerkes (3) mit einer Hauptstation (1) und einer Vielzahl von Anschlüssen (2), wobei die Anschlüsse auf Steuersignale von der Hauptstation reagieren und die Hauptstation so eingerichtet ist, daß sie Bilder mit einer vorgegebenen Bitrate und mit Signalen, die von der Vielzahl von Anschlüssen übertragen wurden, empfängt, wobei das Verfahren die Schritte der Übertragung jeweiliger Synchronisationspulse von den Anschlüssen an die Hauptstation umfaßt, gekennzeichnet durch
Abtasten der empfangenen Synchronisationspulse und Erzeugung von entsprechenden Abtastdaten, Abschicken der Abtastdaten an einen Prozessor (7), der dazu dient, die jeweiligen Phasen der Synchronisationspulse relativ zu den jeweiligen erwarteten Werten zu bestimmen und die jeweiligen Amplituden der Synchronisationspulse zu bestimmen, und Erzeugung von jeweiligen Steuersignalen für die Anschlüsse, um die Phase und Amplitude der Übertragungen von den An-



schlüssen entsprechend zu modifizieren, wodurch die empfangenen Synchronisationspulse mit einer Aufnahmerate aufgenommen werden, die größer als die vorgegebene Bitrate ist.

2. Verfahren nach Anspruch 1, das außerdem die Schritte des Schreibens der Abtastdaten in eine Vielzahl von Gattern (L), die mit einer Taktsignalquelle verbunden sind, die dazu dient, die Gatter mit einer Taktrate zu takten, die niedriger als die Abtastrate ist, wobei das Taktsignal für jedes Gatter eine jeweilig unterschiedliche Phasenverschiebung hat, das Schreiben der Abtastdaten von jedem Gatter in einen jeweiligen seriellen Speicher (VLM) und das Lesen der Abtastdaten aus den seriellen Speichern in den Prozessor umfaßt.
3. Verfahren nach Anspruch 2, bei welchem die Taktrate im wesentlichen dieselbe wie die Bitrate der empfangenen Datenbilder ist.
4. Verfahren nach Anspruch 2 oder 3, bei welchem die Hauptstation einen Haupttaktgeber hat, der mit der Taktrate oder der Abtastrate arbeitet, wobei ein Taktsignal von dem Haupttaktgeber mit der jeweils anderen der Taktrate oder Abtastrate abgeleitet wird und die Vielzahl der Gatter mit der Vorderflanke eines Pulses des Taktsignals bei der Taktrate verriegelt werden und die seriellen Speicher mit der Rückflanke des besagten Pulses verriegelt werden.
5. Verfahren nach einem der Ansprüche 1 bis 4, das außerdem die Schritte der Überlagerung der empfangenen Bilder mit einem lokal erzeugten Markierungspuls, der eine an einen Haupttaktgeber des Systems gekoppelten Phase hat, bei der Hauptstation und darauffolgend das Abtasten eines Teils des Bildes inklusive eines Markerpulses zur Erzeugung entsprechender Abtastdaten und das Absenden der Abtastdaten an einen Steuerungsprozessor mit eigener lokaler Uhr umfaßt, wobei der Steuerungsprozessor dazu dient, Parameter von empfangenen Signalen in dem abgetasteten Abschnitt des Bildes gegenüber solchen des Markierungspulses zu bestimmen.
6. Hauptstation (1) für ein passives optisches Netzwerkssystem (3) und eingerichtet, um Steuersignale zu einer Vielzahl von Anschlüssen (2) zu übertragen, wobei die Anschlüsse auf Steuersignale von der Hauptstation reagieren, und die Hauptstation so eingerichtet ist, daß sie Bilder empfängt, die eine vorgegebene Bitrate haben und Signale umfassen, die durch die Vielzahl von Anschlüssen übertragen wurden, wobei die Hauptstation eine Vorrichtung (4) zum Empfang

jeweiliger Synchronisationspulse von den Anschlüssen umfaßt, gekennzeichnet durch

Abtastvorrichtung (6), die eingerichtet ist zur Aufnahme der empfangenen Synchronisationspulse und zur Erzeugung entsprechender Abtastdaten, Prozessor (7), der auf die besagten Abtastdaten reagiert und dazu dient, die jeweilige Phase der Synchronisationspulse relativ zu den jeweiligen erwarteten Werten zu bestimmen und die jeweiligen Amplituden der Synchronisationspulse zu bestimmen, und Steuersignalerzeugungsvorrichtung, die dazu dient, entsprechende Steuersignale zu erzeugen, um die Phase und Amplitude von Übertragungen der jeweiligen Anschlüsse zu modifizieren, wodurch die Abtastvorrichtung sich dazu eignet, die empfangenen Synchronisationspulse bei einer höheren Abtastrate als die vorgegebene Bitrate abzutasten.

7. Hauptstation nach Anspruch 6, die außerdem eine Vielzahl von Gattern (L), die mit einer Taktsignalquelle verbunden sind, die dazu dient, die Gatter mit einer Taktrate zu takten, die geringer als die Abtastrate ist, wobei das Taktsignal für jedes Gatter eine unterschiedliche jeweilige Phasenverschiebung hat, und einen jeweiligen seriellen Speicher (VLM) für jedes der Vielzahl von Gattern umfaßt, wobei Abtastdaten bei Betrieb für jedes Gatter in den jeweiligen seriellen Speicher geschrieben werden, und jeder serielle Speicher durch einen Resetpuls mit entsprechender jeweiliger Phasenverschiebung zurückgesetzt wird, wodurch die Abtastdaten von der Abtastrate in die Taktrate umgesetzt werden.
8. Hauptstation nach Anspruch 6 oder 7, die außerdem einen Haupttaktgeber, der entweder bei der Taktrate oder der Abtastrate arbeitet, und eine Vorrichtung umfaßt, um aus dem Haupttaktgeber ein Taktsignal mit der anderen der Taktrate oder Abtastrate abzuleiten, und wobei die Vielzahl der Gatter (L) mit der Vorderflanke des Pulses des Taktsignales mit der Taktrate verriegelt werden und die seriellen Speicher (VLM) mit der Rückflanke des besagten Pulses verriegelt werden.
9. Hauptstation nach Anspruch 7, bei welcher die seriellen Speicher (VLM) Dualport-Serial-FIFOs umfassen.
10. Hauptstation nach einem der Ansprüche 6 bis 9, die außerdem eine Markierungsvorrichtung (9) oberhalb der Abtastvorrichtung (6) umfaßt, um einen Markierungspuls vorgegebener Phase und Amplitude den empfangenen Bildern zu überlagern und damit eine Referenz für den Prozessor (7) zu erzeugen.



Revendications

1. Un procédé d'exploitation d'un réseau optique passif (3) comprenant une station de tête de réseau (1) et une pluralité de terminaux (2), les terminaux répondant aux signaux de commande de la station de tête de réseau, et la station de tête de réseau étant agencée pour recevoir des trames ayant un débit binaire prédéterminé et comprenant des signaux émis par la pluralité de terminaux, le procédé comprenant les étapes de transmission des impulsions de mesure de distance respectives des terminaux vers la station de tête de réseau, caractérisé par l'échantillonnage des impulsions de mesure de distance reçues et la production d'échantillons de données correspondant, l'application des échantillons de données à des moyens formant processeur (7) agencés pour déterminer les phases respectives des impulsions de mesure de distance par rapport aux valeurs escomptées respectives et pour déterminer les amplitudes respectives des impulsions de mesure de distance, et l'émission de signaux de commande respectifs pour les terminaux afin de modifier la phase et l'amplitude des émissions provenant des terminaux en conséquence, de manière que les impulsions de mesure de distance reçues soient échantillonnées à une fréquence d'échantillonnage supérieure au débit binaire prédéterminé.
 2. Un procédé selon la revendication 1, comprenant en outre les étapes d'enregistrement d'échantillons de données dans une pluralité de registres de verrouillage (L) reliés à une source de signaux d'horloge agencée pour synchroniser les registres à une fréquence de base inférieure à la fréquence d'échantillonnage, le signal d'horloge de chaque registre ayant un déphasage respectif différent, l'enregistrement d'échantillons de données venant de chaque registre dans une mémoire série respective (mémoire de ligne vidéo VLM), et la lecture d'échantillons de données à partir des mémoires série dans les moyens formant processeur.
 3. Un procédé selon la revendication 2, dans lequel la fréquence de base est sensiblement la même que le débit binaire des trames de données reçues.
 4. Un procédé selon la revendication 2 ou 3, dans lequel la station de tête de réseau comprend une horloge mère fonctionnant à l'une des fréquences de base ou à la fréquence d'échantillonnage, et la pluralité de registres de verrouillage sont verrouillés sur le front avant d'une impulsion du signal d'horloge à la fréquence de base et les mé-
5. Un procédé selon l'une quelconque des revendications 1 à 4, comprenant en outre les étapes de superposition sur les trames reçues dans la station de tête de réseau d'une impulsion de marquage produite localement dont une phase est bloquée sur une horloge mère du système, ensuite, l'échantillonnage d'une partie de la trame comprenant une impulsion de marquage pour produire des échantillons de données correspondants, et l'envoi des échantillons de données à un processeur de commande ayant sa propre horloge locale, le processeur de commande étant agencé pour déterminer les paramètres des signaux reçus dans la partie échantillonnée de la trame relatifs à ceux de l'impulsion de marquage.
6. Une station de tête de réseau (1) utilisable dans un système à réseau optique passif (3) et agencée pour transmettre des signaux de commande à une pluralité de terminaux (2), les terminaux réagissant aux signaux de commande de la station de tête de réseau, et la station de tête de réseau étant agencée pour recevoir des trames ayant un débit binaire prédéterminé et comprenant des signaux transmis par la pluralité de terminaux, la station de tête de réseau comprenant des moyens (4) pour recevoir les impulsions de mesure de distance respectives des terminaux, caractérisée par des moyens d'échantillonnage (8) agencés pour échantillonner les impulsions de mesure de distance reçues et pour produire des échantillons de données correspondants, des moyens formant processeur (7) réagissant auxdits échantillons de données et agencés pour déterminer la phase respective des impulsions de mesure de distance par rapport aux valeurs escomptées respectives et pour déterminer les amplitudes respectives des impulsions de mesure de distance, et des moyens d'émission de signaux de commande agencés pour émettre des signaux de commande respectifs pour modifier la phase et l'amplitude des émissions des terminaux respectifs, de manière que les moyens d'échantillonnage soient agencés pour échantillonner les impulsions de mesure de distance reçues à une fréquence d'échantillonnage supérieure au débit binaire prédéterminé.
7. Une station de tête de réseau selon la revendication 6, comprenant en outre une pluralité de registres de verrouillage (L) reliés à une source de signal d'horloge agencée pour synchroniser les registres à une fréquence de base inférieure à la fréquence d'échantillonnage, le signal d'horloge de chaque registre ayant un déphasage respec-



tif différent, et une mémoire série respective (VLM) pour chaque registre de la pluralité de registres, les échantillons de données étant enregistrés en service pour chaque registre dans la mémoire série respective, et chaque mémoire série étant remise à zéro par une impulsion de remise à zéro ayant un déphasage respectif correspondant, de manière à convertir les échantillons de données de la fréquence d'échantillonnage à la fréquence de base.

8. Une station de tête de réseau selon la revendication 6 ou 7, comprenant en outre une horloge mère fonctionnant à l'une des fréquences de base ou à la fréquence d'échantillonnage et des moyens pour dériver de l'horloge mère un signal d'horloge à l'autre fréquence de base ou fréquence d'échantillonnage, et la pluralité de registres de verrouillage (L) est verrouillée sur le front avant de l'impulsion du signal d'horloge à la fréquence de base et les mémoires série (VLM) sont verrouillées sur le front arrière de ladite impulsion.
9. Une station de tête de réseau selon la revendication 7, dans laquelle les mémoires série (VLM) comprennent des modules FIFO série (premier entré, premier sorti) à double port.
10. Une station de tête de réseau selon l'une quelconque des revendications 6 à 9, comprenant en outre des moyens de marquage (9) disposés en amont des moyens d'échantillonnage (6) et agencés pour superposer une impulsion de marquage de phase et d'amplitude prédéterminées aux trames reçues et créer ainsi une référence utilisable par les moyens formant processeur.

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