

SPECIFICATION

TITLE OF THE INVENTION

PHASE MODULATING APPARATUS EFFECTIVELY USING WAVEFORM STORAGE UNIT

5 FIELD OF THE INVENTION

This invention relates to a phase modulating apparatus for modulating digital baseband signals with the Quadrature Phase Shift Keying (QPSK).

BACKGROUND OF THE INVENTION

10 Currently, the QPSK is widely used as a digital modulation method. For example, RCR STD-28 standard for Personal Handyphone System (PHS) stipulates that the $\pi/4$ -shift QPSK should be used as a modulation method. The QPSK including the $\pi/4$ -shift QPSK is a modulation method in which two bits of data are
15 transferred simultaneously by using the inphase (I-phase) component and quadrature-phase (Q-phase) component of a carrier wave.

Given below is the description of the $\pi/4$ -shift QPSK and conventional $\pi/4$ -shift QPSK modulating apparatus 600.

$\pi/4$ -shift QPSK modulating apparatus receives a baseband
20 signal as serial data. The baseband signal is converted through series-to-parallel conversion into a symbol (X_k, Y_k) which is a piece

of two-bit parallel data, where "k" represents a natural number, indicating that "(X_k, Y_k)" is the k-th symbol. The symbol (X_k, Y_k) is converted by a differential encoding circuit into a quadrature signal (I_k, Q_k). This conversion is performed based on the following
5 formula:

Formula 1

$$\begin{bmatrix} I_k \\ Q_k \end{bmatrix} = \begin{bmatrix} \cos[\Delta\Phi(X_k, Y_k)] & -\sin[\Delta\Phi(X_k, Y_k)] & I_{k-1} \\ \sin[\Delta\Phi(X_k, Y_k)] & \cos[\Delta\Phi(X_k, Y_k)] & Q_{k-1} \end{bmatrix},$$

where $\Delta\Phi(X_k, Y_k)$ has values shown in the following table:

Table 1

X _k	1	0	0	1
Y _k	1	1	0	0
ΔΦ	-3π/4	3π/4	π/4	-π/4

The quadrature signal (I_k, Q_k) obtained in this way is passed through a lowpass filter to have a limited band and to be converted into I-phase and Q-phase components. A modulating circuit provides the inphase and quadrature-phase components for a wireless circuit.

Fig.1 shows symbols (X_k, Y_k) mapped on a two-dimensional I-Q coordinate. By focusing on the movement of a signal point represented by a quadrature signal (I_k, Q_k), it is found that the signal point becomes any of signal points A-D and any of signal
5 points E-H alternately. As is apparent from Fig.1, signal points

A-D are represented by a two-dimensional coordinate system represented by vector $I\alpha$ on the I-axis and vector $Q\alpha$ on the Q-axis as the axes. Also, signal points E-H are represented by a two-dimensional coordinate system represented by vector $I\beta$ and vector $Q\beta$ as the axes, which are respectively equivalent to vectors $I\alpha$ and $Q\alpha$ rotated by $\pi/4$. For example, suppose a current baseband signal is a piece of information represented by symbol point F. Then, "0" is given as its $I\alpha$ coordinate, "0" as its $Q\alpha$ coordinate, "-1" as its $I\beta$ coordinate, and "+1" as its $Q\beta$ coordinate.

Suppose the coordinates of the k-th symbol using the above four vectors are respectively $I_{\alpha k}$, $Q_{\alpha k}$, $I_{\beta k}$, and $Q_{\beta k}$. Then, the quadrature coordinates of k-th symbol, I_k and Q_k , are represented by Formulae 2 and 3 respectively.

Formula 2

$$I_k = I_{\alpha k} + \frac{I_{\beta k}}{\sqrt{2}} - \frac{Q_{\beta k}}{\sqrt{2}}$$

Formula 3

$$Q_k = Q_{\alpha k} + \frac{I_{\beta k}}{\sqrt{2}} + \frac{Q_{\beta k}}{\sqrt{2}}$$

Accordingly, I-phase signal $I(t)$ and Q-phase signal $Q(t)$ output from the modulating circuit are represented by Formula 4 in which $h(t)$ represents a rectangular waveform response function used in the lowpass filter.

Formula 4

$$\begin{aligned}
 I(t) &= \sum_{k=-\infty}^{\infty} I_k h(t-kT) \\
 &= \sum_{k=-\infty}^{\infty} I_{\alpha k} h(t-kT) + \frac{1}{\sqrt{2}} \sum_{k=-\infty}^{\infty} I_{\beta k} h(t-kT) \\
 &\quad - \frac{1}{\sqrt{2}} \sum_{k=-\infty}^{\infty} Q_{\beta k} h(t-kT)
 \end{aligned}$$

Formula 5

$$\begin{aligned}
 Q(t) &= \sum_{k=-\infty}^{\infty} Q_k h(t-kT) \\
 &= \sum_{k=-\infty}^{\infty} Q_{\alpha k} h(t-kT) + \frac{1}{\sqrt{2}} \sum_{k=-\infty}^{\infty} I_{\beta k} h(t-kT) \\
 &\quad + \frac{1}{\sqrt{2}} \sum_{k=-\infty}^{\infty} Q_{\beta k} h(t-kT)
 \end{aligned}$$

Formulae 4 and 5 indicate that limiting the bands of quadrature signals I_k and Q_k may be achieved by limiting bands of each term of Formulae 2 and 3.

Here, if it is supposed that in Fig.1, symbol points A-D are odd and symbol points E-H are even in order, the following formulae are given.

Formula 6

$$I_{\alpha k}, Q_{\alpha k} = \begin{cases} \pm 1 & (k=2N+1) \\ 0 & (k=2N) \end{cases}$$

Formula 7

$$I_{\beta k}, Q_{\beta k} = \begin{cases} 0 & (k=2N+1) \\ \pm 1 & (k=2N) \end{cases}$$

Hence, $I(t)$ and $Q(t)$ are represented by the following formulae.

Formula 8

$$I(t) = \sum_{N=-\infty}^{\infty} I_{\alpha 2N+1} h\{t-(2N+1)T\} + \frac{1}{\sqrt{2}} \sum_{N=-\infty}^{\infty} I_{\beta 2N} h(t-2NT) - \frac{1}{\sqrt{2}} \sum_{N=-\infty}^{\infty} Q_{\beta 2N} h(t-2NT)$$

Formula 9

$$Q(t) = \sum_{N=-\infty}^{\infty} Q_{\alpha 2N+1} h\{t-(2N+1)T\} + \frac{1}{\sqrt{2}} \sum_{N=-\infty}^{\infty} I_{\beta 2N} h(t-2NT) + \frac{1}{\sqrt{2}} \sum_{N=-\infty}^{\infty} Q_{\beta 2N} h(t-2NT)$$

As apparent from the above formulae, of symbols $I_{\alpha k}$, $Q_{\alpha k}$, I , and Q being four vectors of signals $I(t)$ and $Q(t)$, I and $Q_{\alpha k}$ may be represented by using only odd symbol signals, and $I_{\beta k}$ and $Q_{\beta k}$ by using only even symbol signals.

Fig.2 is a block diagram showing the construction of the conventional $\pi/4$ -shift QPSK modulating apparatus 600.

$\pi/4$ -shift QPSK modulating apparatus 600 includes input terminal 601, symbol generating circuit 602, mapping circuit 603, timing generating circuit 605, coordinate accumulators 606, 607, 608, and 609, first storage unit 610, second storage unit 611, 5 third storage unit 612, fourth storage unit 613, subtractor 614,

adders 615, 616, and 617, D/A converters 618 and 619, and output terminals 620 and 621. Mapping circuit 603 includes differential encoding circuit 604.

The baseband signal that is to be modulated is serially
5 input to symbol generating circuit 602 through input terminal 601.

Symbol generating circuit 602 is achieved by a π / 4 -shift register. Symbol generating circuit 602 receives a baseband signal with the timing of clock CL1 provided by timing
10 generating circuit 605, and converts the received baseband signal through series-to-parallel conversion into a symbol (X_k, Y_k) , which is a two-bit parallel signal.

Mapping circuit 603 receives the symbol (X_k, Y_k) generated by symbol generating circuit 602 with the timing of clock
15 CL2 provided by timing generating circuit 605. Mapping circuit 603 performs, to generate a piece of two-bit address data, a certain mapping based on the received symbol (X_k, Y_k) or a result of differential encoding. Mapping circuit 603 provides one bit of the piece of two-bit address data for each of coordinate accumulators
20 606 and 607 with odd symbol timing, and the other bit of the two-bit address data for each of coordinate accumulators 608 and 609 with even symbol timing.

Differential encoding circuit 604, if necessary, performs differential encoding using the received symbol (X_k, Y_k) and

the preceding symbol (X_{k-1}, Y) with the timing of clock CL2 provided by timing generating circuit 605.

Timing generating circuit 605 generates timing signals for entire $\pi/4$ -shift QPSK modulating apparatus 600 based on a
5 clock signal having a higher frequency than that of the baseband signal. CL1 is a clock signal having the same frequency as that of the baseband signal. CL2 is a clock signal having the same frequency as that of symbol data. CL3 is a clock signal having the same frequency as that of symbol data and generates even and odd
10 symbol timing. Timing generating circuit 605 generates elapsed-time information of even and odd symbol periods and provides the information as a lower address for first storage unit 610, second storage unit 611, third storage unit 612, and fourth storage unit 613.

15 Coordinate accumulators 606, 607, 608, and 609 are shift registers and converts in series and parallel each of the addresses provided by mapping circuit 603. Outputs from coordinate accumulators 606, 607, 608, and 609 are respectively provided for first storage unit 610, second storage unit 611, third storage unit
20 612, and fourth storage unit 613.

First storage unit 610 receives an output from coordinate accumulator 606 as a higher address and elapsed-time information from timing generating circuit 605 as a lower address. First storage unit 610 prestores waveform data corresponding to I-

coordinates (I-components). The waveform data indicates response waveforms from the lowpass filter at the time when ± 1 is input to the lowpass filter with odd symbol timing, and a response waveform from the lowpass filter when 0 is input with even symbol timing.

5 Accordingly, first storage unit 610 prestores a digital value corresponding to " $\sum I_{a2N+1} h\{t-(2N+1)T\}$ " in Formula 8.

Second storage unit 611 receives an output from coordinate accumulator 607 as a higher address and elapsed-time information from timing generating circuit 605 as a lower address.

10 Second storage unit 611 prestores waveform data corresponding to Q-coordinates (Q-components). The waveform data indicates response waveforms from the lowpass filter at the time when ± 1 is input to the lowpass filter with odd symbol timing, and a response waveform when 0 is input with even symbol timing. Accordingly, second

15 storage unit 611 stores a digital value corresponding to " $\sum Q_{a2N+1} h\{t-(2N+1)T\}$ " in Formula 9.

Third storage unit 612 receives an output from coordinate accumulator 608 as a higher address and elapsed-time information from timing generating circuit 605 as a lower address.

20 Third storage unit 612 prestores waveform data corresponding to I-coordinates (I-components). The waveform data indicates $1/\sqrt{2}$ response waveforms from the lowpass filter (in the present specification, square root of 2 is represented by $\sqrt{2}$) at the time when ± 1 is input to the lowpass filter with even symbol timing, and

a $1/\sqrt{2}$ response waveform when 0 is input with odd symbol timing. Accordingly, third storage unit 612 stores a digital value corresponding to " $\sum (1/\sqrt{2}) I_{\beta 2N} h(t-2NT)$ " in Formulae 8 and 9.

Fourth storage unit 613 stores an output from coordinate
5 accumulator 609 as a higher address and elapsed-time information
from timing generating circuit 605 as a lower address and stores
waveform data corresponding to Q-coordinates (Q-components). The
waveform data indicates $1/\sqrt{2}$ response waveforms from the lowpass
filter at the time when ± 1 is input to the lowpass filter with even
10 symbol timing, and a $1/\sqrt{2}$ response waveform when 0 is input with
odd symbol timing. Accordingly, fourth storage unit 613 stores a
digital value corresponding to " $\sum (1/\sqrt{2}) Q_{\beta} h(t-2NT)$ " in Formulae
8 and 9.

Subtractor 614 subtracts the output of fourth storage
15 unit 613 from the output of third storage unit 612 to execute a
subtraction of the third term from the second term in Formula 8.

Adder 615 adds the outputs of third and fourth storage
units 613 and 614 to execute an addition of the second and third
terms in Formula 9.

20 Adder 616 adds the output of subtracter 614 and the
output of first storage unit 610, namely, the first term of Formula
8, and outputs instantaneous value $I(t)$ of I-phase signal in
Formula 8.

Adder 617 adds the output of adder 615 and the output

of second storage unit 611, namely, the first term of Formula 9, and outputs instantaneous value $Q(t)$ of Q-phase signal in Formula 9.

D/A converter 618 converts the output of adder 616 into the analog signal and outputs the analog signal via output terminal 620 to a mixer that is not shown in the drawing. The mixer multiplies the output of D/A converter 618 by the carrier wave.

D/A converter 619 converts the output of adder 617 into the analog signal and outputs the analog signal via output terminal 621 to another mixer that is not shown in the drawing. This mixer multiplies the output of D/A converter 619 by the carrier wave which is input via a phase shifter. These two quadrature components of the carrier wave generated in this way are added and output to a transmitting circuit not shown in the drawing.

As is apparent from the above description, a response waveform corresponding to " $\sum I_{a_{2N+1}} h\{t-(2N+1)T\}$," namely, the first term in Formula 8, and a response waveform corresponding to " $\sum Q_{a_{2N+1}} h\{t-(2N+1)T\}$," namely, the first term in Formula 9, may be generated from the same waveform data. Also, a response waveform corresponding to " $\sum (1/\sqrt{2}) I_{\beta} h(t-2NT)$," namely, the second term in Formulae 8 and 9, and a response waveform corresponding to " $\sum (1/\sqrt{2}) Q_{\beta} h(t-2NT)$," namely, the third term in Formulae 8 and 9, may be generated from the same waveform data. That means first storage unit 610 and second storage unit 611 of the conventional

$\pi/4$ -shift QPSK modulating apparatus 600 store the same filter data. It is the same with third storage unit 612 and fourth storage unit 613. Generally, such storage units are achieved by ROMs. However, increases in the number and the capacity of ROMs
5 lead to an increase in the circuit scale, which generates a problem in cost and a disadvantage in achieving the circuits in LSI.

Furthermore, transmitting the signal modulated with the above construction with burst transmission causes another problem in that the frequency band of the transmission signal expands due
10 to an enormous spurious emission generated by a steep rise of the transmission signal.

A method for preventing the problem is known in which a certain ramp period is set before and after the transmission of the modulated signal so that the transmission signal rises and
15 falls smoothly according to the envelopes in the ramp periods. This processing is known as ramp processing. In the conventional ramp processing, the amplification factor of the transmission amplifier is smoothly increased or reduced so that the level of the transmission signal smoothly rises and falls. However, it is
20 difficult to change the amplification factor of the transmission amplifier, that is, to correctly change the level of the transmission signal according to the function selected as an optimal ramp waveform. Therefore, it has been difficult to perform the ramp processing accurately.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a phase modulating apparatus which has a simple circuit construction by effectively using waveform storage units and which
5 generates a modulated signal with which an accurate burst transmission is possible.

The above object is achieved by a phase modulating apparatus including: storage means for storing waveform data
10 including a plurality of waveforms used for rise ramp processing, a plurality of phase waveforms used for both I-component and Q-component of a plurality of transmission symbols, and a plurality of waveforms used for fall ramp processing; converting means for converting each of a dummy symbol for the rise ramp processing, the
15 plurality of transmission symbols, and a dummy symbol for the fall ramp processing into the I-component and the Q-component, wherein the dummy symbol for the rise ramp processing, the plurality of transmission symbols, and the dummy symbol for the fall ramp processing are provided in time series; address providing means for
20 outputting alternately during one symbol period the I-component and the Q-component converted by the converting means as addresses of the storage means; separating means for fetching an I-component waveform and a Q-component waveform which are read alternately from the storage means and outputting simultaneously the I-component

waveform and the Q-component waveform; and combining means for combining the I-component waveform and the Q-component waveform output from the separating means into a symbol waveform.

With such a construction, the storage means may be used
5 effectively as shown below. The ramp processing may be performed very easily since circuits for controlling the gain of a transmission amplifier are not required since ramp rise waveforms and ramp fall waveforms are read from the storage means respectively before and after the transmission data transmission
10 section and the read waveforms are combined into symbol waveforms via the separating means and the combining means. Furthermore, this construction has succeeded in reducing the storage capacity since the same waveforms are used in the transmission section for both I-component and Q-component by setting the address providing
15 means and the separating means respectively before and after the storage means.

The address providing means of the above phase modulating apparatus may include: timing generating means for generating first timing information which indicates any of a rise
20 ramp processing section, a transmission section, and a fall ramp processing section and second timing information which indicates the symbol period used in each of the rise ramp processing section, the transmission section, and the fall ramp processing section; selecting means for selecting alternately during one symbol period

the I-component and the Q-component converted by the converting means according to the second timing information; and inputting means for inputting an address into the storage means, wherein the address includes a first partial address, which is the first timing
5 information, and second partial address, which is an output from the selecting means.

The address providing means of the above phase modulating apparatus may include: I-shift register for accumulating I-components of a certain number of symbols converted by the
10 converting means and outputting the I-components in parallel; and Q-shift register for accumulating Q-components of the certain number of symbols converted by the converting means and outputting the Q-components in parallel, wherein the selecting means selects alternately an output from the I-shift register and an output from
15 the Q-shift register.

The separating means of the above phase modulating apparatus may include: first delay means for delaying the I-component waveform output from the storage means; and second delay means for delaying the Q-component waveform output from the storage
20 means so that the second delay means is synchronized with the first delay means in outputting.

Furthermore, in a $\pi/4$ -shift QPSK modulating apparatus achieving the above object, the switching means selects alternately an output from the I-coordinate accumulating means and an output

from the Q-coordinate accumulating means according to a switch signal, which is faster than the time information, and outputs a selected output. Also, a response waveform from a digital filter to an I-coordinate input (or a corresponding ramp waveform) and a
5 response waveform from a digital filter to an Q-coordinate input (or a corresponding ramp waveform) may be generated in a similar process based on the same response waveform from the digital filter. Accordingly, the rise ramp means, the filter means, and the fall ramp means may be used for both I-coordinate and Q-
10 coordinate. That means, the response waveforms from a digital filter to an I-coordinate input and Q-coordinate (or corresponding ramp waveforms) may be alternately output with the frequency of the switching signal. The separating means separates the response waveforms from a digital filter to an I-coordinate input and Q-
15 coordinate (or corresponding ramp waveforms) into two streams which respectively correspond to the I-coordinate and the Q-coordinate. Therefore, the $\pi/4$ -shift QPSK modulating apparatus of the present invention has succeeded in reducing the number of storage units half that of the conventional $\pi/4$ -shift QPSK modulating apparatus,
20 which includes the filter means for each of the I-coordinate and Q-coordinate input to filters. This indicates that the $\pi/4$ -shift QPSK modulating apparatus of the present invention has such a construction as reduces the number of circuits as a whole and makes it easier to achieve the whole apparatus in an LSI chip.

Furthermore, it is possible to perform the ramp processing between the burst rise section and the burst fall section since the reduction in the construction of the filter means enables including of the ramp period notifying means, the rise ramp means, and fall ramp means. This enables the present apparatus to perform accurate burst transmissions by having an embedded circuit for the ramp processing, while the conventional $\pi/4$ -shift QPSK modulating apparatus has this circuit externally.

Each of the rise ramp means, the filter means, and the fall ramp means of the present $\pi/4$ -shift QPSK modulating apparatus may include an odd storage unit and an even storage unit, wherein the odd storage unit stores response waveform data of a digital filter and also stores burst rise ramp waveform data and burst fall ramp waveform data which each correspond to the response waveform data of a digital filter, wherein the response waveform data of a digital filter is generated at a time when an I-coordinate and a Q-coordinate of an odd signal point are input to the digital filter by recognizing the ramp period notification signal, an output from the switching means, and the time information as an address, wherein the even storage unit stores response waveform data of a digital filter and also stores burst rise ramp waveform data and burst fall ramp waveform data which each correspond to the response waveform data of a digital filter, wherein the response waveform data of a digital filter is generated at a time when an I-

coordinate and a Q-coordinate of an even signal point are input to the digital filter by recognizing the ramp period notification signal, an output from the switching means, and the time information as an address. Compared to a case where a filter means of the conventional $\pi/4$ -shift QPSK modulating apparatus is achieved by a storage unit storing filter response waveforms for I-coordinate inputs, each storage unit of the present apparatus requires a larger storage capacity than the conventional filter means since each storage unit stores ramp waveform data. However, the present apparatus performs accurate burst transmissions by having an embedded circuit for the ramp processing, while the conventional $\pi/4$ -shift QPSK modulating apparatus has this circuit externally.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

Fig.1 shows symbols (X_k, Y_k) mapped on a two-dimensional I-Q coordinate;

Fig.2 is a block diagram showing the construction of a conventional $\pi/4$ -shift QPSK modulating apparatus;

Fig.3 is a block diagram showing a partial construction of the $\pi/4$ -shift QPSK modulating apparatus of the present embodiment;

Fig.4 shows the ramp period in a slot of a Time Division

Multiple Access/Time Division Duplex (TDMA/TDD) frame and shows a ramp waveform generated;

Fig.5 is a time chart showing the timing signals generated by a timing generating circuit;

5 Fig.6 is a time chart showing the operation timing of a switching circuit and separating circuit;

Figs.7A and 7B show the relation between data stored in storage units and waveform data which is read from the storage units according to the two-MSB addresses given as address signal
10 Tc;

Fig.8 shows a separating circuit; and

Fig.9 shows eye patterns representing the waveforms output during two symbol periods (including even and odd) in a general transmission.

15 DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig.3 is a block diagram showing the construction of $\pi/4$ -shift QPSK modulating apparatus 100 of the present embodiment.

$\pi/4$ -shift QPSK modulating apparatus 100, which is
20 achieved in an LSI chip, includes ramp period detecting circuit 101, timing generating circuit 102, input terminal 103, symbol generating circuit 104, mapping circuit 105, coordinate accumulators 106, 107, 108, and 109, switching circuits 110 and

111, storage units 112 and 113, separating circuits 114 and 115, subtractor 116, adders 117, 118, and 119, and D/A converters 120 and 121. Mapping circuit 105 includes differential encoding circuit 105a. Mixers 122 and 123, phase shifter 124, and adder 125
5 are external circuits connected to $\pi/4$ -shift QPSK modulating apparatus 100.

Fig.4 shows the ramp period in a slot of a Time Division Multiple Access/Time Division Duplex (TDMA/TDD) frame and shows a ramp waveform generated.

10 As has been described earlier, in the burst transmission of a modulated signal, the frequency band of the transmission signal expands due to an enormous spurious emission generated by a steep rise of the transmission signal. Therefore, for a communication system that performs burst transmissions with a
15 digital modulation method such as $\pi/4$ -shift QPSK, generally a certain ramp period is set for each of the burst rise and burst fall so that the ramp processing on the transmission signal is performed in the ramp periods.

For example, as shown in (a) SLOT of Fig.4, each slot
20 of TDMA/TDD frames for PHS (Personal Handyphone System) is assigned 625 μ sec in which 240 bits of data may be transmitted with 384KB/sec of physical transmission rate. The first four bits of each slot are used as ramp bits for the burst rise, and the last 16 bits as guard bits. The guard bits form a non-transmission section that

is set to prevent the transmission data from being affected by spurious emissions or noises by other electric waves. It is determined that the receiver should not regard the ramp bits and guards bits as substantial data. Also, the first four bits of the guard bits are used as ramp bits for the burst fall. The baseband signal is not input to the last 12 bits of the guard bits. Therefore, on ending the ramp processing of the ramp bits for the burst fall, $\pi/4$ -shift QPSK modulating apparatus 100 ends the modulating process.

10 The four bits in each of the burst rise and fall are input via input terminal 103 as a baseband signal representing dummy data. The ramp waveform as shown in (c) MODULATION SIGNAL of Fig.4 is output based on the baseband signal. The ramp waveform rises and falls according to a smooth envelope. This ramp waveform
15 is obtained by multiplying a gate signal as shown in (b) GATE SIGNAL of Fig.4 by a modulated signal combined according to the baseband signal.

 The baseband signal having substantial data is input during the 220-bit section (hereinafter referred to as "general
20 transmission") sandwiched by the ramp bits.

 Ramp period detecting circuit 101 receives clock CK being the same clock signal as that provided for timing generating circuit 102 and receives transmission trigger signal TXTRG, which indicates the transmission start of the modulated signal, from an

external element such as a TDMA circuit.

Ramp period detecting circuit 101 starts counting clock CK when transmission trigger signal TXTRG becomes active. This allows a baseband signal representing substantial data to be input
5 via input terminal 103 to $\pi/4$ -shift QPSK modulating apparatus 100, allowing 100 to start processing.

Ramp period detecting circuit 101 recognizes the start of rise ramp processing when the count value of clock CK becomes equal to the delay of the start of modulation processing from an
10 input, namely, to the response delay of digital filter for an input, after transmission trigger signal TXTRG becomes active.

Ramp period detecting circuit 101 outputs "01" as address signal Tc to storage units 112 and 113 while continuing to count clock CK. Address signal Tc being composed of two bits is
15 used as two MSBs (Most Significant Bits) in the addresses of storage units 112 and 113. The storage areas in storage units 112 and 113 indicated by the two-MSB address "01" store ramp waveform data for rise ramp processing corresponding to the two-dimensional coordinate data used in the rise ramp processing.

20 Ramp period detecting circuit 101 recognizes the end of rise ramp processing when the count value of clock CK becomes equal to the time period between the time when transmission trigger signal TXTRG becomes active and the time when rise ramp processing ends. At the same time, a baseband signal being substantial data

is input via input terminal 103 to $\pi/4$ -shift QPSK modulating apparatus 100. Ramp period detecting circuit 101 outputs "00" as address signal Tc to storage units 112 and 113 while continuing to count clock CK. The storage areas in storage units 112 and 113
5 indicated by two-MSB address "00" store response waveform data from a lowpass filter such as a route Nyquist filter to an input of two-dimensional coordinate data which is obtained from a general-transmission baseband signal.

Also, ramp period detecting circuit 101 recognizes the
10 start of fall ramp processing when the count value of clock CK becomes equal to the time period between the time when transmission trigger signal TXTRG becomes active and the time when fall ramp processing starts. A baseband signal being certain dummy data is input via input terminal 103 to $\pi/4$ -shift QPSK modulating
15 apparatus 100. Ramp period detecting circuit 101 outputs "10" as address signal Tc to storage units 112 and 113 while continuing to count clock CK. The storage areas in storage units 112 and 113 indicated by two-MSB address "10" store fall ramp waveform data corresponding to the two-dimensional coordinate data for the fall
20 ramp processing.

Ramp period detecting circuit 101 recognizes the end of fall ramp processing when the count value of clock CK becomes equal to the time period between the time when transmission trigger signal TXTRG becomes active and the time when fall ramp processing

ends. This allows $\pi/4$ -shift QPSK modulating apparatus 100 to end the modulating process.

Timing generating circuit 102 generates clocks T1-T6 as shown in Fig.5 based on clock CK which is provided from an external element and is a clock signal having a frequency higher than the bit rate of the input baseband signal. Clock T1 (four bits in Fig.5) represents a count value of clock signal CK between an odd symbol timing opportunity and immediately before the next odd symbol timing opportunity and is provided for storage units 112 and 113. That is, clock T1 is elapsed time information indicating a time elapsed during two odd/even symbol periods. Clock T2 is a clock signal having the same frequency as that of the input baseband signal. Clock T3 is a clock signal having the same frequency as that of one symbol. Clock T4 is a clock signal having the same frequency as that of two symbols. Clock T5 is a clock signal having a reversed phase of clock T4. Clock T6 is a switch signal having a switching speed twice the count of clock T1 that is elapsed time information.

Input terminal 103 is used to input a baseband signal, namely serial data as a signal to be modulated, to $\pi/4$ -shift QPSK modulating apparatus 100.

Symbol generating circuit 104 is achieved by a shift register. Symbol generating circuit 104 receives a baseband signal with the timing of clock T1 provided by timing generating circuit

102, and converts the received baseband signal in series and parallel to generate symbol (X_k, Y_k) , which is composed of successive two bits in the baseband signal.

Mapping circuit 105 receives the symbol data generated
5 by symbol generating circuit 104 with the timing of clock T3 having the same frequency as that of symbol data, the clock T3 being provided by timing generating circuit 102. Mapping circuit 105 performs a certain mapping based on the received symbol data or an encoding result of differential encoding circuit 105a to generate
10 a piece of two-bit two-dimensional coordinate data representing an address.

Now, an example of two-dimensional coordinate data output from mapping circuit 105 is described with reference to Fig.1.

15 As previously mentioned, a signal point represented by a quadrature signal (I_k, Q_k) becomes any of signal points A-D and any of signal points E-H alternately. Also, the coordinates of points A-D are respectively represented as $A(1,1)$, $B(-1,1)$, $C(-1,-1)$, and $D(1,-1)$ on a two-dimensional coordinate represented by vector $I\alpha$
20 and vector $Q\alpha$ as the axes. Also, the coordinates of points E-H are respectively represented as $E(1,1)$, $F(-1,1)$, $G(-1,-1)$, and $H(1,-1)$ on a two-dimensional coordinate represented by vector $I\beta$ and vector $Q\beta$ as the axes.

Here, suppose a baseband signal "1, 0, 1, 1, 0, 0, 0,

1, ..." is input to input terminal 103. Then, symbol generating circuit 104 generates a sequence of two-bit symbols $(X_1, Y_1) = (1, 0)$, $(X_2, Y_2) = (1, 1)$, $(X_3, Y_3) = (0, 0)$, $(X_4, Y_4) = (0, 1)$... in sequence.

Mapping circuit 105 obtains the coordinates of the
5 signal points indicated by the symbols by using signal point H shown in Fig.1 as a standard point. For example, it is found from Table 1 that the odd symbol (X_1, Y_1) indicates signal point D having phase difference $-\pi/4$ between itself and point H. The signal point D is represented as $D(1, -1)$ on a two-dimensional coordinate
10 represented by vector $I\alpha$ and vector $Q\alpha$ as the axes. Note that "-1" is represented as "0" since "-1" cannot be represented by one bit. Mapping circuit 105 outputs two-dimensional coordinates $D(1, 0)$ as the mapping result for symbol (X_1, Y_1) . The first bit "1" of the two-dimensional coordinates $D(1, 0)$ is output to coordinate
15 accumulator 106, and the second bit "0" to coordinate accumulator 107.

Similarly, the next even symbol (X_2, Y_2) indicates signal point F having phase difference $-3\pi/4$ between itself and point D. The coordinate values of signal point F are represented as $F(-1, 1)$
20 on a two-dimensional coordinate represented by vectors $I\beta$ and $Q\beta$ as the axes. Mapping circuit 105 outputs two-dimensional coordinates $F(0, 1)$ as the mapping result for symbol (X_2, Y_2) . The first bit "0" of the two-dimensional coordinates $F(0, 1)$ is output to coordinate accumulator 108, and the second bit "1" to coordinate

accumulator 109.

Similarly, the next odd symbol (X_3, Y_3) indicates signal point C having phase difference $\pi/4$ between itself and point F. Mapping circuit 105 outputs two-dimensional coordinates $C(0,0)$.
5 The first bit "0" is output to coordinate accumulator 106, and the second bit "0" to coordinate accumulator 107. The next even symbol (X_4, Y_4) indicates signal point H having phase difference $3\pi/4$ between itself and point C. Mapping circuit 105 outputs two-dimensional coordinates $H(1,0)$. The first bit "1" is output to
10 coordinate accumulator 108, and the second bit "0" to coordinate accumulator 109.

Differential encoding circuit 105a if necessary performs differential encoding on the symbol data received by mapping circuit 105. More specifically, differential encoding circuit 105a
15 obtains the signal point of symbol (X_k, Y_k) by storing in advance a conversion table corresponding to Table 1 and storing at least one signal point indicated by the preceding symbol (X_{k-1}, Y_{k-1}) .

Coordinate accumulator 106, achieved by a shift register, accumulates $I\alpha$ -coordinates one bit by one bit for each
20 odd symbol timing opportunity, and outputs a certain number of accumulated bits, for example, five bits of $I\alpha$ -coordinates as five higher bits succeeding to the two MSBs in storage unit 112 to switching circuit 110. According to these five higher bits, filter response waveform (or ramp waveform) data corresponding to the $I\alpha$ -

coordinates input with odd symbol timing is read from storage unit 112.

Coordinate accumulator 107, achieved by a shift register, accumulates $Q\alpha$ -coordinates one bit by one bit for each odd symbol timing opportunity, and outputs a certain number of accumulated bits, for example, five bits of $Q\alpha$ -coordinates as five higher bits succeeding to the two MSBs in storage unit 112 to switching circuit 110. According to these five higher bits, filter response waveform (or ramp waveform) data corresponding to the $Q\alpha$ -coordinates input with odd symbol timing is read from storage unit 112.

Coordinate accumulator 108, achieved by a shift register, accumulates $I\beta$ -coordinates one bit by one bit for each odd symbol timing opportunity, and outputs a certain number of accumulated bits, for example, five bits of $I\beta$ -coordinates as five higher bits succeeding to the two MSBs in storage unit 113 to switching circuit 111. According to these five higher bits, $1/\beta$ filter response waveform (or ramp waveform) data corresponding to the $I\beta$ -coordinates input with odd symbol timing is read from storage unit 113.

Coordinate accumulator 109, achieved by a shift register, accumulates $Q\beta$ -coordinates one bit by one bit for each odd symbol timing opportunity, and outputs a certain number of accumulated bits, for example, five bits of $Q\beta$ -coordinates as five

higher bits succeeding to the two MSBs in storage unit 113 to switching circuit 111. According to these five higher bits, $1/\beta$ filter response waveform (or ramp waveform) data corresponding to the $Q\beta$ -coordinates input with odd symbol timing is read from
5 storage unit 113.

Switching circuit 110 is achieved by a selector and the like. Switching circuit 110 outputs addresses input from coordinate accumulators 106 and 107 alternately to storage unit 112 with the timing of clock T6 before a current piece of elapsed time
10 information is switched to another one with the timing of clock T1. Fig.6 shows the output from switching circuit 110 and clock T6 at the output.

Switching circuit 111 is, as switching circuit 110 is, achieved by a selector and the like. Switching circuit 111 outputs
15 addresses input from coordinate accumulators 108 and 109 alternately to storage unit 113 with the timing of clock T6 before a current piece of elapsed time information is switched to another one with the timing of clock T1.

Storage unit 112 stores address signal Tc sent from ramp
20 period detecting circuit 101 as a two-MSB address, stores the outputs of coordinate accumulators 106 and 107 as addresses of bits succeeding to the two MSBs, and stores clock T1, namely, elapsed time information sent from timing generating circuit 102 as bits succeeding to all these bits.

Figs.7A and 7B show the relation between data stored in storage units 112 and 113 and waveform data which is read from storage units 112 and 113 according to the two-MSB addresses given as address signal Tc.

5 In a storage area indicated by two-MSB address "00" in storage unit 112, waveform data of general transmission corresponding to $I\alpha$ - and $Q\alpha$ -coordinates is stored. The waveform data of general transmission is data showing the level (instantaneous value) of the response waveform from the lowpass
10 filter such as route Nyquist filter which is given for an $I\alpha$ -/ $Q\alpha$ -coordinate input. Storage unit 112 stores waveform data corresponding to odd symbol timing, that is, response waveform data from a filter to input ± 1 which are the $I\alpha$ - and $Q\alpha$ -coordinates of odd symbol timing. Also, storage unit 112 stores waveform data
15 corresponding to even symbol timing, that is, response waveform data from the lowpass filter to input 0 which is the $I\alpha$ - and $Q\alpha$ -coordinates of even symbol timing.

In a storage area indicated by two-MSB address "01" in storage unit 112, waveform data at burst rise is stored.

20 Note that each piece of the ramp waveform data stored in storage units 112 and 113 is gained by multiplying a window function representing (b) GATE SIGNAL shown in Fig.4 by a filter response waveform corresponding to each of $I\alpha$ -, $Q\alpha$ -, $I\beta$ -, and $Q\beta$ -coordinates. That is, if it is supposed that $g(t)$ represents

the window function, and $I(t)g(t)$ and $Q(t)g(t)$ respectively instantaneous values of I-phase and Q-phase of the ramp waveform, then the following Formulae are given.

Formula 10

$$\begin{aligned}
 I(t)g(t) = & \sum_{N=-\infty}^{\infty} I_{\alpha 2N+1} h\{t-(2N+1)T\} g\{t-(2N+1)T\} \\
 & + \frac{1}{\sqrt{2}} \sum_{N=-\infty}^{\infty} I_{\beta 2N} h(t-2NT) g(t-2NT) \\
 & - \frac{1}{\sqrt{2}} \sum_{N=-\infty}^{\infty} Q_{\beta 2N} h(t-2NT) g(t-2NT)
 \end{aligned}$$

Formula 11

$$\begin{aligned}
 Q(t)g(t) = & \sum_{N=-\infty}^{\infty} Q_{\alpha 2N+1} h\{t-(2N+1)T\} g\{t-(2N+1)T\} \\
 & + \frac{1}{\sqrt{2}} \sum_{N=-\infty}^{\infty} I_{\beta 2N} h(t-2NT) g(t-2NT) \\
 & + \frac{1}{\sqrt{2}} \sum_{N=-\infty}^{\infty} Q_{\beta 2N} h(t-2NT) g(t-2NT)
 \end{aligned}$$

The ramp waveform in MODULATED SIGNAL (c) of Fig.4 is obtained by combining (adding) the inphase component in the carrier wave modulated by amplifying $I(t)g(t)$ of Formula 10 and the quadrature-phase component in the carrier wave modulated by amplifying $Q(t)g(t)$ of Formula 11.

Accordingly, the storage area in storage unit 112

indicated by two-MSB address "01" stores the ramp waveform data for rise ramp processing corresponding to two-dimensional coordinates ($I\alpha, Q\alpha$), that is, the ramp waveform data for rise ramp processing corresponding to the first term of Formulae (10) and (11). For the
5 burst rise, $I\alpha$ - and $Q\alpha$ -coordinates can only be "+1" or "-1" with odd symbol timing, and "0" with even symbol timing. This is the same as for general transmission.

Also, the storage area in storage unit 112 indicated by two-MSB address "10" stores the ramp waveform data for fall ramp
10 processing corresponding to two-dimensional coordinates ($I\alpha, Q\alpha$), that is, the ramp waveform data for fall ramp processing corresponding to the first term of Formulae (10) and (11). For the fall ramp processing, $I\beta$ -and $Q\beta$ -coordinates can only be "0" with odd symbol timing, and "+1" or "-1" with even symbol timing. This
15 is the same as for general transmission.

In a general transmission, two-MSB address "00" given as address signal Tc and the succeeding higher bits from coordinate accumulators 106 and 107 divided in time division with the timing of clock T6 are input to storage unit 112. The higher bits from
20 coordinate accumulators 106 and 107 are updated with each odd symbol timing opportunity. In parallel with these pieces of data, a lower address as clock T1 of elapsed time information is input to storage unit 112. Clock T1 represents a count value of clock signal CK between an odd symbol timing opportunity and immediately

before the next odd symbol timing opportunity.

Coordinate accumulator 106 outputs $I\alpha$ -coordinates accumulated with odd symbol timing to storage unit 112 as, for example, five higher bits succeeding to the two MSBs. The LSB of
5 the five higher bits is the $I\alpha$ -coordinate of the current odd symbol timing opportunity and the other four bits are $I\alpha$ -coordinates of the previous odd timing opportunities, with "-1" represented by "0." According to these five higher bits, the filter response waveform data corresponding to the current elapsed
10 time information for the $I\alpha$ -coordinate of the current odd symbol timing opportunity is read from storage unit 112, for example, with the odd timing of clock T6.

Coordinate accumulator 107 outputs $Q\alpha$ -coordinates accumulated with odd symbol timing to storage unit 112 as, for
15 example, five higher bits succeeding to the two MSBs. Of the five higher bits, the LSB is the $Q\alpha$ -coordinate of the current odd symbol timing opportunity and the other four bits are $Q\alpha$ -coordinates of the previous odd timing opportunities, with "-1" represented by "0." According to these five higher bits, the
20 filter response waveform data corresponding to the current elapsed time information for the $Q\alpha$ -coordinate of the current odd symbol timing opportunity is read from storage unit 112, for example, with the even timing of clock T6.

No address is input to storage unit 112 from coordinate

accumulators 106 and 107 with even symbol timing. However, clock T1 of elapsed time information indicates even symbol timing. As has been described earlier, both $I\alpha$ -and $Q\alpha$ -coordinates are "0" with even symbol timing. Therefore, two kinds of the filter
5 response waveform data at each elapsed time with input "0" are read alternately in time division from storage unit 112 every time the Lower address exceeds a certain value.

The only difference between the rise ramp processing and the general transmission is that the two-MSB address "01" given by
10 address signal Tc is input to storage unit 112. The rise ramp processing is performed the same as the general transmission in terms of the rest of the processing, that is, addresses of higher bits succeeding to the two MSBs are input from coordinate accumulators 106 and 107 to storage unit 112, and, in parallel,
15 clock T1 as a lower address.

Coordinate accumulator 106 outputs $I\alpha$ -coordinates accumulated with odd symbol timing to storage unit 112 as, for example, five higher bits succeeding to the two MSBs. According to these five higher bits, the ramp waveform data at the burst rise
20 corresponding to the current elapsed time information for the $I\alpha$ -coordinate of the current odd symbol timing opportunity is read from storage unit 112, for example, with the odd timing of clock T6.

Coordinate accumulator 107 outputs $Q\alpha$ -coordinates

accumulated with odd symbol timing to storage unit 112 as, for example, five higher bits succeeding to the two MSBs. According to these five higher bits, the ramp waveform data at the burst rise corresponding to the current elapsed time information for the $Q\alpha$ -coordinate of the current odd symbol timing opportunity is read from storage unit 112, for example, with the even timing of clock T6.

Both $I\alpha$ -and $Q\alpha$ -coordinates are "0" with even symbol timing. Therefore, two kinds of the ramp waveform data at the burst rise at each elapsed time with input "0" are read alternately in time division from storage unit 112 every time the Lower address exceeds a certain value.

The only difference between the fall ramp processing and the general transmission is that two-MSB address "10" given by address signal Tc is input to storage unit 112.

With odd symbol timing, as the higher addresses, which are input from coordinate accumulators 106 and 107 alternately in time division with the timing of clock T6, and a lower address given as clock T1 of elapsed time information are input to storage unit 112, two pieces of the ramp waveform data at the burst fall respectively corresponding to the current elapsed time information for the $I\alpha$ -coordinate of the current odd symbol timing opportunity and to the current elapsed time information for the $Q\alpha$ -coordinate are read alternately in time division from storage unit 112 with

the timing of clock T6.

Both $I\alpha$ -and $Q\alpha$ -coordinates are "0" with even symbol timing. Therefore, in the same way as the general transmission and burst rise, two kinds of the ramp waveform data at the burst fall
5 at each elapsed time with input "0" are alternately read in time division from storage unit 112 every time the Lower address exceeds a certain value.

Storage unit 113 receives address signal Tc, which is input to storage units 112 and 113 simultaneously, as an address
10 of two MSBs. Storage unit 113 prestores the outputs of coordinate accumulators 108 and 109, which are divided in time division with the timing of clock T6, as addresses of bits succeeding to the two MSBs, and receives clock T1, namely, elapsed time information sent from timing generating circuit 102 as lower addresses.

15 As shown in Fig.7A, storage unit 113 has the same area assignment with addresses as storage unit 112. That is, in a storage area indicated by two-MSB address "00" in storage unit 112, waveform data of general transmission is stored; in a storage area indicated by two-MSB address "01," ramp waveform data at burst
20 rise; and in a storage area indicated by two-MSB address "10," ramp waveform data at burst fall. The bits of each of the above waveform data respectively correspond to $I\beta$ - and $Q\beta$ -coordinates that are input to the lowpass filter.

Storage unit 113 stores the following kinds of waveform

data for general transmission: a $1/\sqrt{2}$ response waveform data of the lowpass filter, such as a root Nyquist filter, at the time when ± 1 , which are the values of $I\beta$ - and $Q\beta$ -coordinates given with even symbol timing, is input to the lowpass filter; and a $1/\sqrt{2}$ response waveform data of the lowpass filter at the time when 0, which is the value of $I\beta$ - and $Q\beta$ -coordinates given with odd symbol timing, is input to the lowpass filter.

Also, storage unit 113 stores the following kinds of ramp waveform data for burst rise: a $1/\sqrt{2}$ ramp waveform data for rise ramp processing at the time when either of ± 1 , which are the values of $I\beta$ - and $Q\beta$ -coordinates given with even symbol timing, is input to the lowpass filter; and a $1/\sqrt{2}$ ramp waveform data for rise ramp processing at the time when 0, which is the value of $I\beta$ - and $Q\beta$ -coordinates given with odd symbol timing, is input to the lowpass filter. That means storage unit 113 stores the ramp waveform data that is equal to the second and third terms in Formulae 10 and 11.

Furthermore, storage unit 113 stores the following kinds of ramp waveform data for burst fall: a $1/\sqrt{2}$ ramp waveform data for fall ramp processing at the time when either of ± 1 , which are the values of $I\beta$ - and $Q\beta$ -coordinates given with even symbol timing, is input to the lowpass filter; and a $1/\sqrt{2}$ ramp waveform data for fall ramp processing at the time when 0, which is the value of $I\beta$ - and $Q\beta$ -coordinates given with odd symbol timing, is

input to the lowpass filter.

In a general transmission, address signal Tc is input as two-MSB address "00" to storage unit 113, and the succeeding higher bits divided in time division with the timing of clock T6
5 are input alternately from coordinate accumulators 108 and 109. The higher bits from coordinate accumulators 108 and 109 are updated with each even symbol timing opportunity. In parallel with these pieces of data, a lower address as clock T1 of elapsed time information is input to storage unit 113.

10 Coordinate accumulator 108 outputs $I\beta$ -coordinates accumulated with even symbol timing to storage unit 113 as, for example, five higher bits succeeding to the two MSBs. The LSB of the five higher bits is the $I\beta$ -coordinate of the current even
15 symbol timing opportunity and the other four bits are $I\beta$ -coordinates of the previous even timing opportunities, with "-1" represented by "0." According to these five higher bits, the $1/\sqrt{2}$ filter response waveform data corresponding to the current elapsed time information for the $I\beta$ -coordinate of the current even symbol timing opportunity is read from storage unit 113, for example, with
20 the odd timing of clock T6.

 Coordinate accumulator 109 outputs $Q\beta$ -coordinates accumulated with even symbol timing to storage unit 113 as, for example, five higher bits succeeding to the two MSBs. Of the five higher bits, the LSB is the $Q\beta$ -coordinate of the current even

symbol timing opportunity and the other four bits are $Q\beta$ -coordinates of the previous even timing opportunities, with "-1" represented by "0." According to these five higher bits, the $1/\sqrt{2}$ filter response waveform data corresponding to the current elapsed
5 time information for the $Q\beta$ -coordinate of the current even symbol timing opportunity is read from storage unit 113, for example, with the even timing of clock T6.

With odd symbol timing, the address in storage unit 113 is not updated as no address is input from coordinate accumulators
10 108 and 109. However, clock T1 of elapsed time information indicates odd symbol timing. As has been described earlier, both $I\beta$ - and $Q\beta$ -coordinates are "0" with odd symbol timing. Therefore, two kinds of the $1/\sqrt{2}$ filter response waveform data at each elapsed time with input "0" are read alternately in time
15 division from storage unit 113 every time the Lower address exceeds a certain value.

The only difference between the rise ramp processing and the general transmission is that two-MSB address "01" given by address signal Tc is input to storage unit 113. The rise ramp
20 processing is performed the same as the general transmission in terms of the rest of the processing, that is, addresses of higher bits succeeding to the two MSBs are input alternately from coordinate accumulators 108 and 109 to storage unit 113, and, in parallel, clock T1 as lower addresses.

Therefore, two kinds of the $1/\sqrt{2}$ ramp waveform data of the current elapsed time information with input "0" corresponding to $I\beta$ - and $Q\beta$ -coordinates are read alternately in time division with the timing of clock T6 when the lower address given by clock T1 is less than a certain value. Also, the $1/\sqrt{2}$ ramp waveform data of the current elapsed time information with $I\beta$ -coordinate input with the current even symbol timing is read, for example, with odd timing of clock T6. The $1/\sqrt{2}$ ramp waveform data of the current elapsed time information with $Q\beta$ -coordinate input with the current even symbol timing is read, for example, with even timing of clock T6.

The only difference between the fall ramp processing and the general transmission is that two-MSB address "10" given by address signal Tc is input to storage unit 113. The fall ramp processing is performed the same as the general transmission and rise ramp processing for the rest, that is, addresses of higher bits succeeding to the two MSBs are input from coordinate accumulators 108 and 109 to storage unit 113, and, in parallel, clock T1 as a lower address.

Therefore, the $1/\sqrt{2}$ ramp waveform data at the burst fall of the current elapsed time information with "0" input with the current odd symbol timing is read with the timing of clock T6 when the Lower address given by clock T1 is less than a certain value. The $1/\sqrt{2}$ ramp waveform data at the burst fall of the

current elapsed time information with the $I\beta$ -coordinate input with the current even symbol timing is read, for example, with odd timing of clock T6. The $1/\sqrt{2}$ ramp waveform data at the burst fall of the current elapsed time information with the $Q\beta$ -coordinate
5 input with the current even symbol timing is read, for example, with even timing of clock T6.

Separating circuit 114 separates the output from storage unit 112 into the filter response waveform (or ramp waveform) data corresponding to $I\alpha$ -coordinate and the filter response waveform
10 (or ramp waveform) data corresponding to $Q\alpha$ -coordinate with the timing of clock T6 and outputs the two kinds of data simultaneously, for example, with the cycle of clock T1. More specifically, separating circuit 114 receives the filter response waveform data corresponding to $I\alpha$ -coordinate, for example, with
15 odd timing of clock T6 and outputs the data to adder 118 with the following even timing of the same clock T6. Also, separating circuit 114 receives and outputs the filter response waveform data corresponding to $Q\alpha$ -coordinate to adder 119, for example, with even timing of clock T6. Fig.8 shows separating circuit 114 in
20 detail. The drawing includes registers 114a-114c and inverter 114d. Note that a clock having a shorter synchronous cycle than clock T6 may be used for registers 114a-114c to shorten the delay.

Separating circuit 115 separates the output from storage

unit 112 into the $1/\sqrt{2}$ filter response waveform (or ramp waveform) data corresponding to $I\beta$ -coordinate and the $1/\sqrt{2}$ filter response waveform (or ramp waveform) data corresponding to $Q\beta$ -coordinate with the timing of clock T6 and outputs the two kinds of data simultaneously, for example, with the cycle of clock T1. More specifically, separating circuit 115 receives the $1/\sqrt{2}$ filter response waveform data corresponding to $I\beta$ -coordinate, for example, with odd timing of clock T6 and outputs the data to subtracter 116 and adder 117 with the following even timing of the same clock T6. Also, separating circuit 115 receives and outputs the $1/\sqrt{2}$ filter response waveform data corresponding to $Q\beta$ -coordinate to subtracter 116 and adder 117, for example, with even timing of clock T6. Separating circuit 115 has the same construction as that shown Fig.8.

Subtractor 116 subtracts the $1/\sqrt{2}$ filter response waveform data corresponding to $Q\beta$ -coordinate from the $1/\sqrt{2}$ filter response waveform data corresponding to $I\beta$ -coordinate, both kinds of data being output from separating unit 115. That is, subtracter 116 executes the subtraction of the third term from the second term in Formula 8.

Adder 117 adds two kinds of data being output from separating unit 115, namely, two kinds of $1/\sqrt{2}$ filter response waveform data respectively corresponding to $I\beta$ -coordinate and $Q\beta$ -coordinate. That is, adder 117 executes the addition of the second

and third terms in Formula 9.

Adder 118 adds the output from subtracter 116 to the filter response waveform (or ramp waveform) data corresponding to $I\alpha$ -coordinate, namely, one of the outputs from separating unit 114 to output instantaneous value $I(t)$ of I-phase signal given by Formula 8.

Adder 119 adds the output from adder 117 to the filter response waveform (or ramp waveform) data corresponding to $Q\alpha$ -coordinate, namely, the other of the outputs from separating unit 114 to output instantaneous value $Q(t)$ of Q-phase signal given by Formula 9.

D/A converting unit 120 converts digital data $I(t)$ into an analog signal, $I(t)$ being the output from adder 118 and representing the instantaneous value of the I-phase signal.

D/A converting unit 121 converts digital data $Q(t)$ into an analog signal, $Q(t)$ being the output from adder 119 and representing the instantaneous value of the Q-phase signal.

The above operations performed by subtracter 116 and adders 117-119 generate instantaneous value $I(t)$ of I-phase signal and instantaneous value $Q(t)$ of Q-phase signal which are used to generate corresponding ramp waveforms at the burst rise and fall. Also, the above operations generate instantaneous value $I(t)$ of I-phase signal and instantaneous value $Q(t)$ of Q-phase signal which correspond to the response waveforms of the lowpass filter at

general transmissions.

Fig.9 shows eye patterns representing the waveforms output from D/A converters 120 and 121 during two symbol periods (including even and odd) in a general transmission. In the drawing, the horizontal axis shows the elapsed time, the vertical axis the output level of filter response waveform $h(t)$ of I- and Q-phases. It is supposed that when filter input is 1 and interference between codes is 0, instantaneous value of base point is 1.

With even symbol timing, the levels of instantaneous values $I(t)$ and $Q(t)$ of the standard point are any of $+\sqrt{2}$, $-\sqrt{2}$, and 0 since the first terms in Formulae 8 and 9 may be "0" and at the same time the second and third terms may cancel each other out. When the second and third terms cancel each other out, either of $I(t)$ and $Q(t)$, namely, respective instantaneous values of I and Q phases, is level 0. For example, instantaneous value $I(t)$ of I phase is level 0 for signal point E or G in Fig.1. At the same time, instantaneous value $Q(t)$ of Q phase is level $+\sqrt{2}$ for signal point E, level $-\sqrt{2}$ for signal point G.

With odd symbol timing, each level of instantaneous values $I(t)$ and $Q(t)$ of the standard point is either of +1 and -1 since the second and third terms are level 0 and each of $I\alpha$ and $Q\alpha$ of the first term is either of +1 and -1. For example, instantaneous values $I(t)$ and $Q(t)$ of the standard point are level

1 for signal point A.

Mixer 122 mixes the output from D/A converter 120 and a carrier wave. The output from mixer 122 is represented by $I(t)\cos 2\pi fCt$ which is a result of multiplying $I(t)$, the output
5 from D/A converter 120, by carrier wave $\cos 2\pi fCt$.

Mixer 123 mixes the output from D/A converter 121 and a carrier wave input via $\pi/2$ phase shifter 124. The output from mixer 123 is represented by $Q(t)\sin 2\pi fCt$ which is a result of multiplying $Q(t)$, the output from D/A converter 121, by carrier
10 wave $\sin 2\pi fCt$ having phase difference $\pi/2$.

$\pi/2$ phase shifter 124 delays the phase of input carrier waves by $\pi/2$.

Adder 125 multiplexes the outputs from mixers 122 and 123 and outputs the multiplexed value. Adder 125 outputs modulated
15 signal $I(t)\cos 2\pi fCt + Q(t)\sin 2\pi fCt$ which corresponds to a response waveform from the lowpass filter. Adder 125 outputs a certain ramp waveform as shown in Fig.4 (c) MODULATED SIGNAL during the ramp period.

As apparent from the above description, this embodiment
20 of the present invention has succeeded in reducing the number of storage units from four, as storage units 610-613 in conventional $\pi/4$ -shift QPSK modulating apparatus 600, to two by reading the waveform data stored in storage units 112 and 113 with time division with clock T6 corresponding to I- and Q-coordinates. This

reduces the number of circuits as a whole and makes it easier to achieve $\pi/4$ -shift QPSK modulating apparatus 100 in an LSI chip.

Also, the reduction in the number of circuits makes it possible for storage units 112 and 113 to store the ramp waveform data at burst rise and burst fall enabling the ramp processing at the burst rise and burst fall. Furthermore, it is possible to generate the ramp waveform more accurately with the same procedure as that used in general transmissions by using the ramp waveform data stored in storage units 112 and 113.

10 In the present embodiment, the ramp waveform data is generated for each of the burst rise and burst fall and is stored in storage units 112 and 113. For the burst rise, one pattern of the ramp waveform data generated based on a certain piece of dummy data may be stored in each of storage units 112 and 113 since the
15 substantial data has not been input yet and the data is not demodulated from the ramp waveform. Also, for the burst fall, one pattern of the ramp waveform data generated in advance may be stored in each of storage units 112 and 113 so that the ramp wave falls smoothly from the filter response waveform at general
20 transmission. This is because there is no need of considering interferences response components which are generated by the previous inputs at general transmission. Even for the burst fall, the interference by response components by the inputs at general transmission would not be ignored if the ramp waveform were to be

generated according to the response waveform from the actual filter. However, in reality, storage units 112 and 113 do not store such interferences but store the genuine waveform data which is read as response waveforms. Accordingly, storage space not so
5 much as that required for storing the filter response waveform data at a general transmission is required even if the ramp waveform data for both burst rise and fall is stored.

In this embodiment of the present invention, the ramp waveform data is stored for both burst rise and burst fall.
10 However, the ramp waveform data may not necessarily be stored for both burst rise and burst fall. For example, storage units 112 and 113 may store only ramp waveform data at burst rise. Alternatively, a counter for counting down the elapsed time, that is, with a reversed direction of clock T1, may be set so that at
15 burst falls, the output from this counter is used as lower bits instead of clock T1 to read the ramp waveform of the burst rise.

Also, the ramp waveform of the modulated signal may be generated from the waveform data for general transmissions with dummy data input instead of being generated from the ramp waveform
20 data. For example, amplitude adjustment circuits consisting of shift registers may be set at the outputs of adders 118 and 119 or at the outputs of storage units 112 and 113 so that at burst rises, lower bits of an input value are output in the beginning then the number of output bits is increased as the time elapses to generate

the ramp waveform at the burst rise. Similarly, for the burst falls, the number of output bits may be decreased as the time elapses to generate the ramp waveform at the burst fall.

In this embodiment of the present invention, address
5 signal Tc is used as two MSBs in the addresses of storage units 112 and 113. However, address signal Tc may not necessarily be used as a two-MSB address. Address signal Tc may be used as two bits succeeding to two MSBs in the addresses, the two
s being the outputs from switching circuits 110 and 111 since the
10 ramp waveform data does not require as much amount of data as the waveform data at general transmissions.

In this embodiment of the present invention, each of coordinate accumulators 106, 107, 108, and 109 accumulates, for example, five bits of coordinates. However, they may accumulate
15 seven, ten, or other number of bits instead of five bits. That is, the number of bits accumulated by the accumulators may be determined based on the degree in which the filter response to the earlier coordinate values affects the filter response to the later coordinate values as time elapses. Note that as the number of bits
20 accumulated by accumulators 106, 107, 108, and 109 increases, the accuracy of the filter response waveform improves but the amount of data stored in storage units 112 and 113 increases.

In this embodiment of the present invention, a case with $\pi/4$ -shift QPSK is described. However, QPSK may be used instead of

$\pi/4$ -shift QPSK. In that case, either of the two horizontal data flows shown in Fig.3 may be used to achieve such an operation.

INDUSTRIAL USE POSSIBILITY

This invention is suitable for phase modulating
5 apparatuses for allowing storage units to store the waveform data
of I- and Q-components of the symbol data in advance and generating
the symbol waveform according to the waveform data. This invention
is also suitable for simplifying circuits since the transmission
amplifier need not perform a gain control since the reduction in
10 the capacity of the storage unit enables the storage of the
waveform data used in the ramp processing around the burst
transmission in the storage unit with other waveforms.



CLAIMS

What is claimed is:

- 1 1. A phase modulating apparatus comprising:
 - 2 storage means for storing waveform data including a
 - 3 waveform used for rise ramp processing, a plurality of phase
 - 4 waveforms used for both I-component and Q-component of a plurality
 - 5 of transmission symbols, and a waveform used for fall ramp
 - 6 processing;
 - 7 converting means for converting each of a dummy symbol
 - 8 for the rise ramp processing, the plurality of transmission
 - 9 symbols, and a dummy symbol for the fall ramp processing into the
 - 10 I-component and the Q-component, wherein the dummy symbol for the
 - 11 rise ramp processing, the plurality of transmission symbols, and
 - 12 the dummy symbol for the fall ramp processing are provided in time
 - 13 series;
 - 14 address providing means for providing alternately during
 - 15 one symbol period the I-component and the Q-component converted by
 - 16 the converting means as addresses of the storage means;
 - 17 separating means for fetching an I-component waveform
 - 18 and a Q-component waveform which are read alternately from the
 - 19 storage means and outputting simultaneously the I-component
 - 20 waveform and the Q-component waveform; and
 - 21 combining means for combining the I-component waveform
 - 22 and the Q-component waveform output from the separating means into





23 a symbol waveform.

1 2. The phase modulating apparatus of CLAIM 1, wherein the address
2 providing means comprises:

3 timing generating means for generating first timing
4 information which indicates a rise ramp processing section, a
5 transmission section, and a fall ramp processing section and second
6 timing information which indicates the symbol period used in each
7 of the rise ramp processing section, the transmission section, and
8 the fall ramp processing section;

9 selecting means for selecting alternately during one
10 symbol period the I-component and the Q-component converted by the
11 converting means according to the second timing information; and

12 inputting means for inputting an address into the
13 storage means, wherein the address includes a first partial
14 address, which is the first timing information, and second partial
15 address, which is an output from the selecting means.

1 3. The phase modulating apparatus of CLAIM 2, wherein the address
2 providing means further comprises:

3 I-shift register for accumulating I-components of a
4 certain number of symbols converted by the converting means and
5 outputting the I-components in parallel; and

6 Q-shift register for accumulating Q-components of the





7 certain number of symbols converted by the converting means and
8 outputting the Q-components in parallel, wherein
9 the selecting means selects alternately an output from
10 the I-shift register and an output from the Q-shift register.

1 4. The phase modulating apparatus of CLAIM 1, wherein the
2 separating means comprises:

3 first delay means for delaying the I-component waveform
4 output from the storage means; and

5 second delay means for delaying the Q-component waveform
6 output from the storage means so that the second delay means is
7 synchronized with the first delay means in outputting.

1 5. A $\pi/4$ -shift QPSK modulating apparatus for assigning uniquely
2 a signal point on a two-dimensional coordinate, which has an I-axis
3 and a Q-axis perpendicular to one another, for each set of
4 sequential two bits in serial data input and generating a modulated
5 signal corresponding to a response waveform which is output from
6 a lowpass digital filter at a time when an I-coordinate and a Q-
7 coordinate of the signal point is input, the $\pi/4$ -shift QPSK
8 modulating apparatus comprising:

9 I-coordinate accumulating means for accumulating the I-
10 coordinate and outputting accumulated I-coordinates;

11 Q-coordinate accumulating means for accumulating the Q-





12 coordinate and outputting accumulated Q-coordinates;

13 ramp period notifying means for outputting a ramp period

14 notification signal which indicates a burst rise period for ramp

15 processing, a burst transmission period during which a modulated

16 signal representing transmission data is transmitted, and a burst

17 fall period for ramp processing;

18 clock means for outputting time information and a switch

19 signal, wherein the time information, having a frequency higher

20 than input data, indicates a certain elapsed time, and the switch

21 signal is faster than the time information;

22 switching means for selecting alternately an output from

23 the I-coordinate accumulating means and an output from the Q-

24 coordinate accumulating means according to the switch signal and

25 outputting a selected output;

26 rise ramp means for outputting alternately a burst rise

27 ramp waveform for an I-coordinate filter input and a burst rise

28 ramp waveform for a Q-coordinate filter input according to the ramp

29 period notification signal, an output from the switching means, and

30 the time information;

31 filter means for outputting alternately a filter

32 response waveform for an I-coordinate input and a filter response

33 waveform for a Q-coordinate input according to the ramp period

34 notification signal, an output from the switching means, and the

35 time information;





36 fall ramp means for outputting alternately a burst fall
37 ramp waveform for an I-coordinate filter input and a burst fall
38 ramp waveform for a Q-coordinate filter input according to the ramp
39 period notification signal, an output from the switching means, and
40 the time information; and

41 separating means for separating each output from the
42 rise ramp means, the filter means, and the fall ramp means into two
43 streams which respectively correspond to the I-coordinate and the
44 Q-coordinate.

1 6. The $\pi/4$ -shift QPSK modulating apparatus of CLAIM 5, wherein
2 the I-coordinate accumulating means comprises:
3 odd I-coordinate accumulating means for accumulating I-
4 coordinates of odd signal points in the serial data input and
5 outputting an I-coordinate sequence including a certain number of
6 accumulated I-coordinates; and
7 even I-coordinate accumulating means for accumulating
8 I-coordinates of even signal points in the serial data input and
9 outputting an I-coordinate sequence including the certain number
10 of accumulated I-coordinates, wherein

11 the Q-coordinate accumulating means comprises:
12 odd Q-coordinate accumulating means for accumulating Q-
13 coordinates of odd signal points in the serial data input and
14 outputting an Q-coordinate sequence including the certain number





15 of accumulated Q-coordinates; and

16 even Q-coordinate accumulating means for accumulating

17 Q-coordinates of even signal points in the serial data input and

18 outputting an Q-coordinate sequence including the certain number

19 of accumulated Q-coordinates, wherein

20 the switching means comprises:

21 odd switching means for selecting alternately an output

22 from the odd I-coordinate accumulating means and an output from the

23 odd Q-coordinate accumulating means according to the switch signal

24 and outputting a selected output; and

25 even switching means for selecting alternately an output

26 from the even I-coordinate accumulating means and an output from

27 the even Q-coordinate accumulating means according to the switch

28 signal and outputting a selected output, wherein

29 the rise ramp means, the filter means, and the fall ramp

30 means include an odd storage unit and an even storage unit,

31 wherein

32 the odd storage unit stores response waveform data of

33 a digital filter and also stores burst rise ramp waveform data and

34 burst fall ramp waveform data which each correspond to the response

35 waveform data of the digital filter, wherein the response waveform

36 data of the digital filter corresponds to an I-coordinate and a Q-

37 coordinate which are determined by two bits at odd input data which

38 is indicated by addresses, namely, the ramp period notification





39 signal, an output from the switching means, and the time
40 information, wherein
41 the even storage unit stores response waveform data of
42 a digital filter and also stores burst rise ramp waveform data and
43 burst fall ramp waveform data which each correspond to the response
44 waveform data of the digital filter, wherein the response waveform
45 data of the digital filter corresponds to an I-coordinate and a Q-
46 coordinate which are determined by two bits at even input data
47 which is indicated by addresses, namely, the ramp period
48 notification signal, an output from the switching means, and the
49 time information.

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ABSTRACT

Ramp period detecting circuit 101 outputs signal T_c that indicates the start and end of the ramp period. Two-dimensional quadrature coordinates $(I\alpha, Q\alpha)$ and $(I\beta, Q\beta)$ are output alternately. Coordinate accumulator 106 accumulates $I\alpha$ which is
5 +1 or -1 corresponding to each odd piece of two-bit data; coordinate accumulator 107 accumulates $Q\alpha$ which is 0 corresponding to each even piece of two-bit data. Response waveforms from a digital lowpass filter (or rise/fall ramp waveforms) corresponding to signal T_c and outputs from coordinate accumulators 106 and 107,
10 namely accumulated values of $I\alpha$ and $Q\alpha$, are alternately read from storage unit 112.

Fig. 1

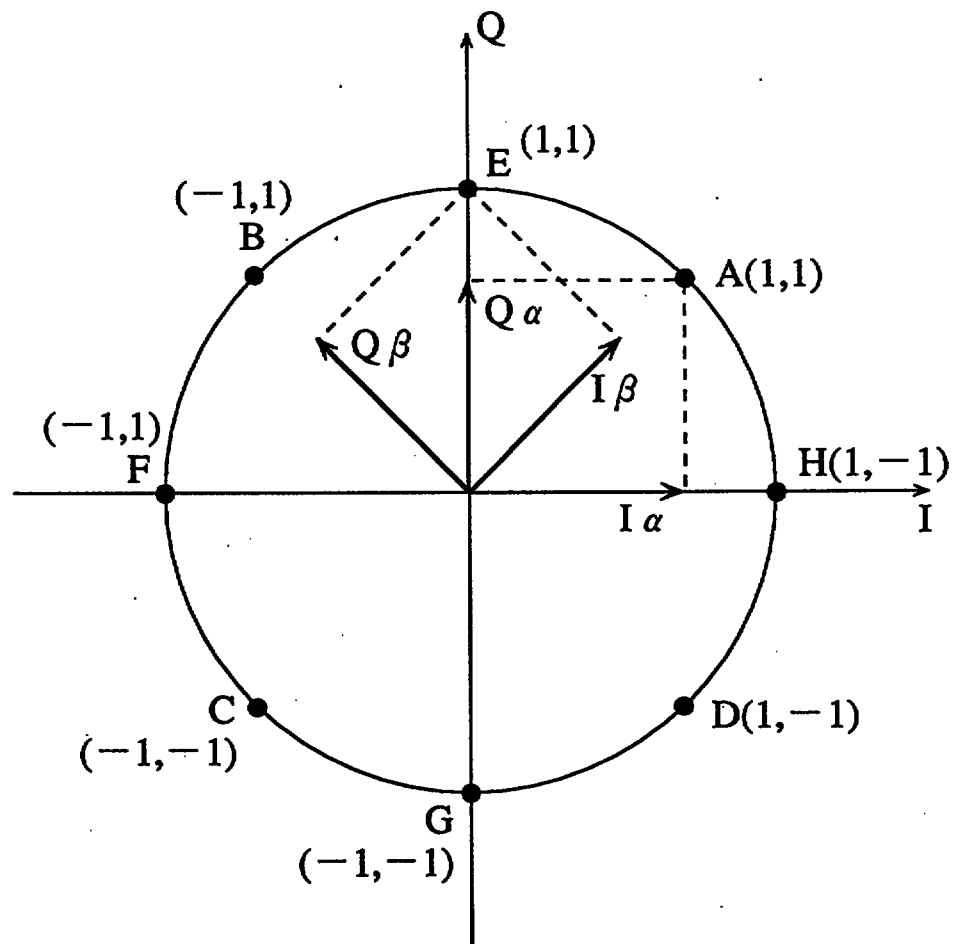


Fig. 2

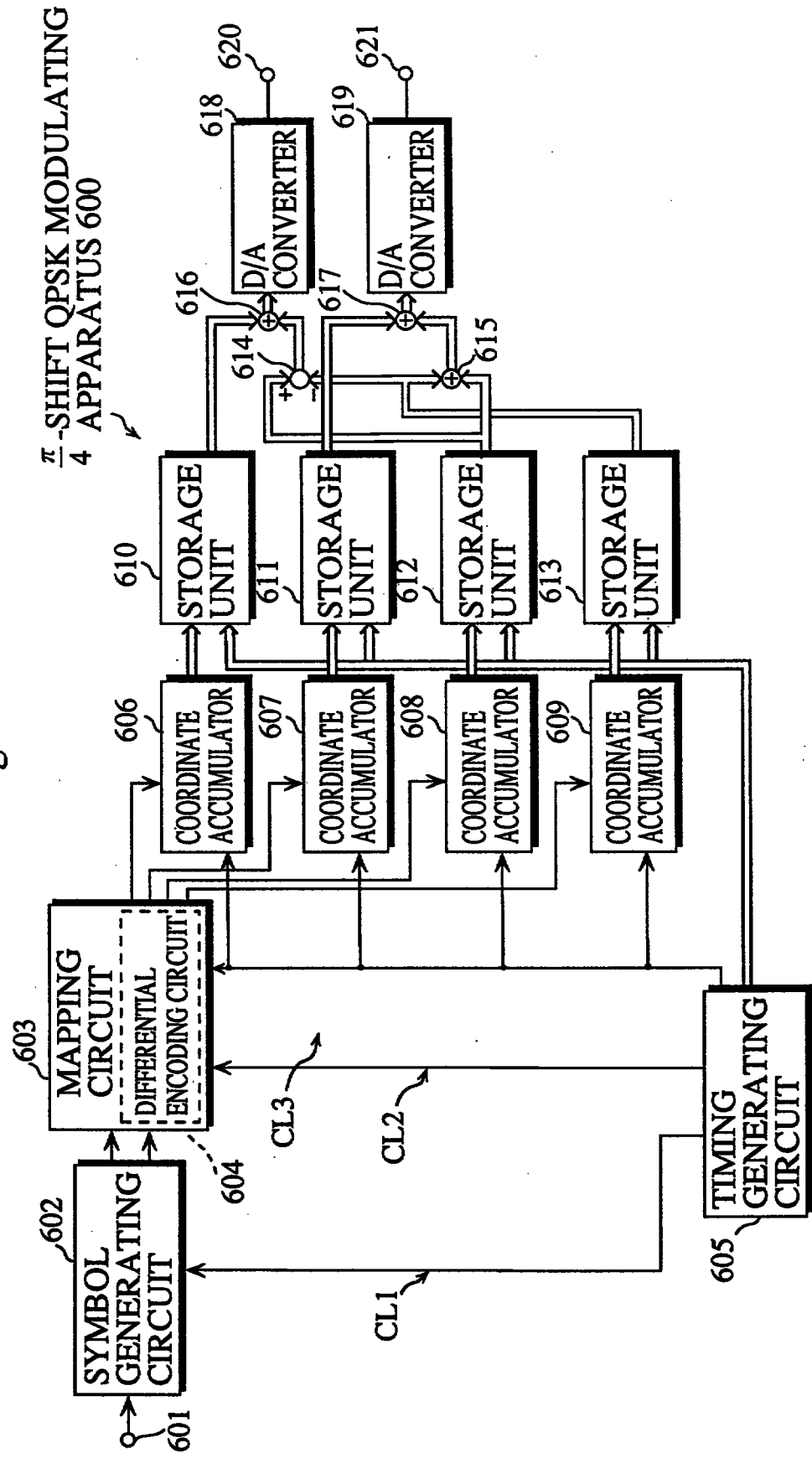


Fig. 3

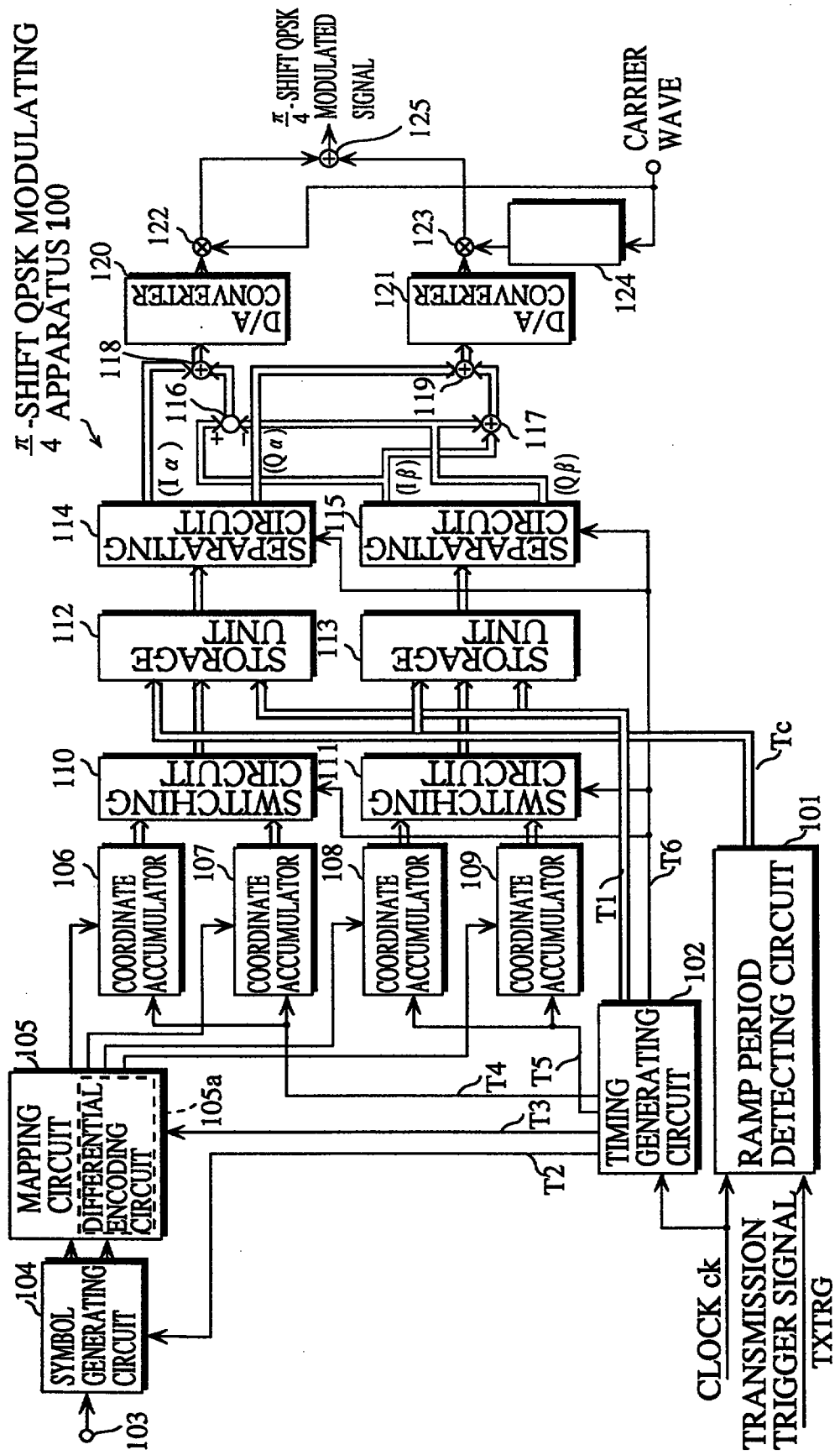


Fig. 4

The diagram illustrates the timing of a transmission burst across three parts: (a) SLOT, (b) GATE SIGNAL, and (c) MODULATED SIGNAL.

(a) SLOT: A horizontal timeline showing the structure of a transmission slot. The total duration is 625 μ s. It is divided into several sections: 4 RAMP BITS, 16 GUARD BITS, 4 RAMP BITS, 220 BITS, 240 BITS, and a final section labeled R. The 220 BITS and 240 BITS sections are further divided into sub-sections labeled G(16), R(4), and R.

(b) GATE SIGNAL (GAIN OF TRANSMISSION SIGNAL): A graph showing the gain of the transmission signal over time. The vertical axis is labeled 0 and 1. The signal starts at 0, rises to 1, and then falls back to 0. The rising and falling edges are labeled BURST RISE and BURST FALL respectively.

(c) MODULATED SIGNAL: A graph showing the modulated signal over time. The signal is a high-frequency carrier wave whose amplitude is modulated by the gate signal. The rising and falling edges of the modulated signal are labeled BURST RISE and BURST FALL respectively.

(b) GATE SIGNAL $\left(\begin{array}{c} \text{GAIN OF} \\ \text{TRANSMISSION} \\ \text{SIGNAL} \end{array} \right)$

(c) MODULATED SIGNAL

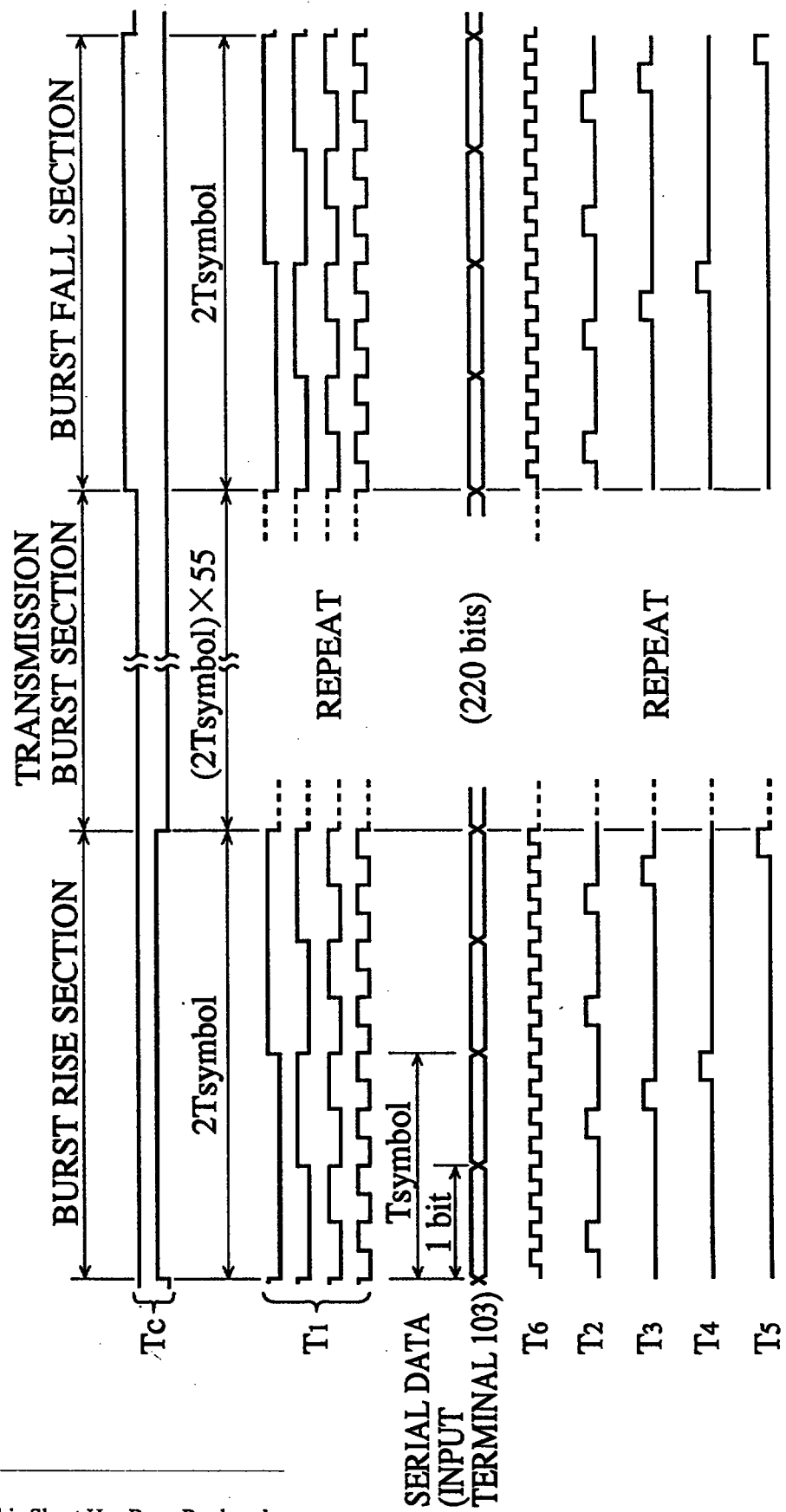


Fig. 6

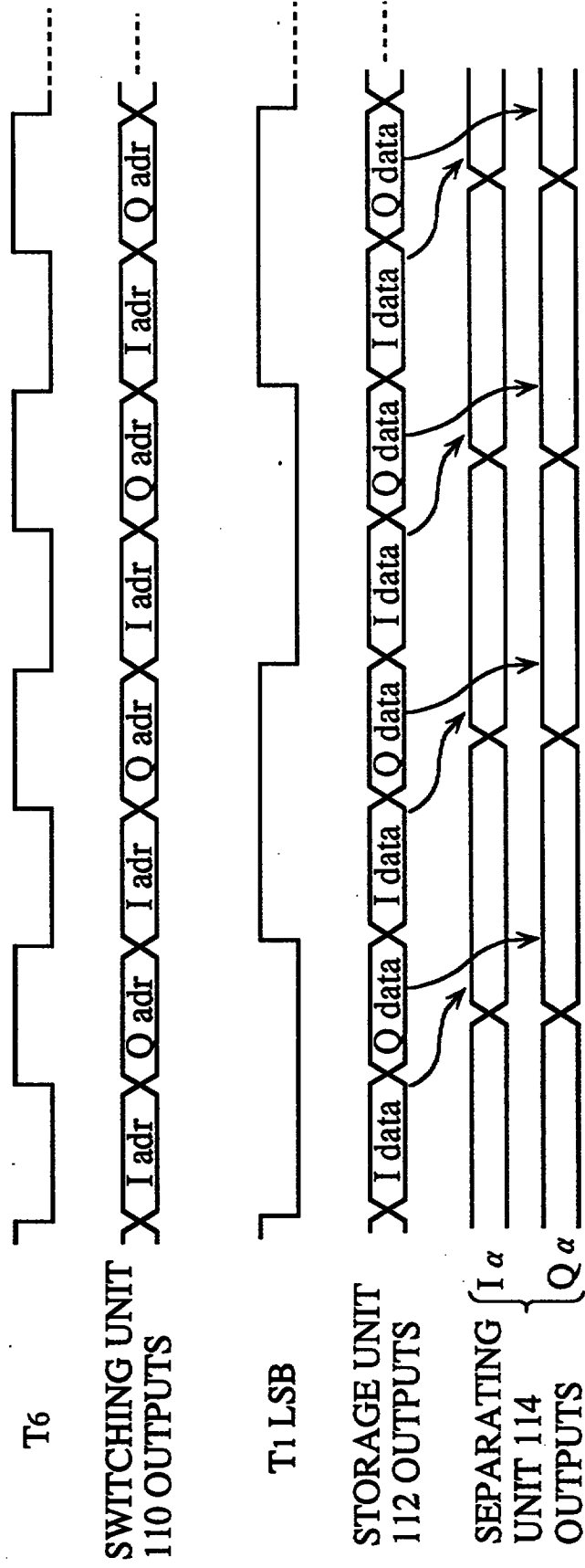


Fig. 7A

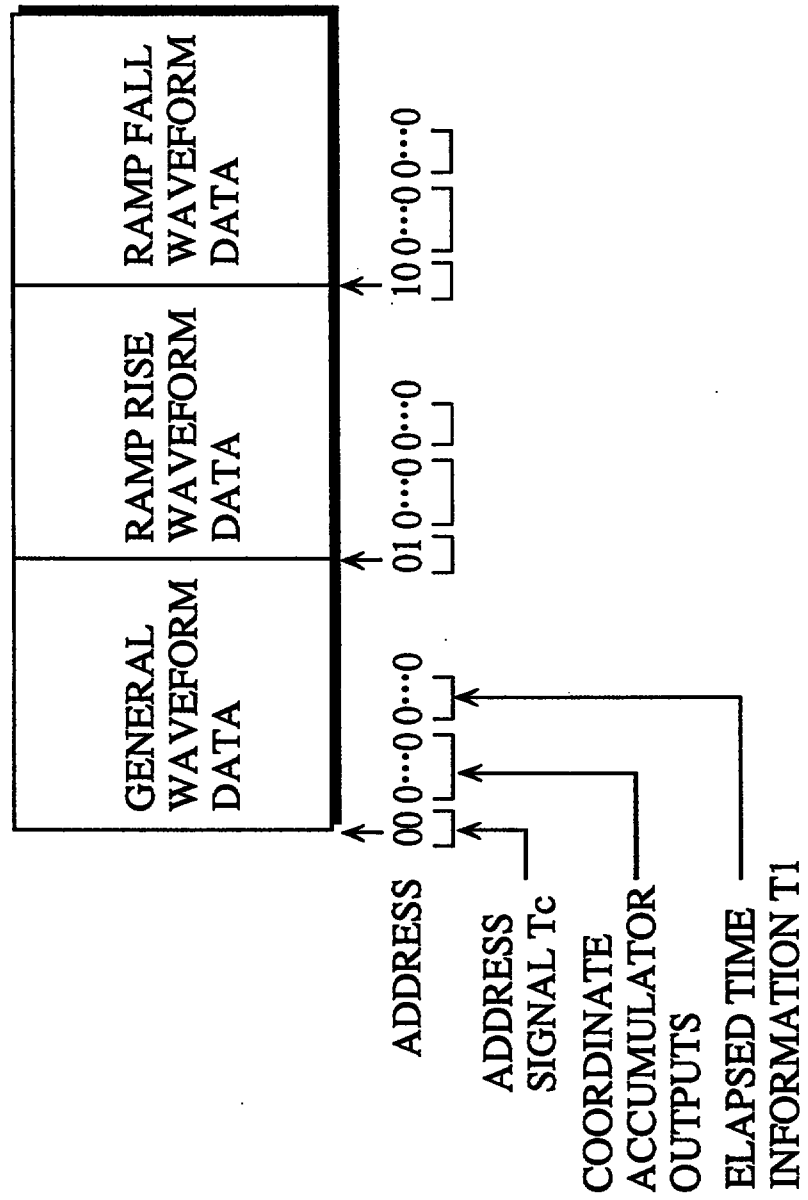


Fig. 7B

WAVEFORM DATA	ADDRESS SIGNAL T _c
GENERAL	00
RAMP RISE	01
RAMP FALL	10

Fig. 8

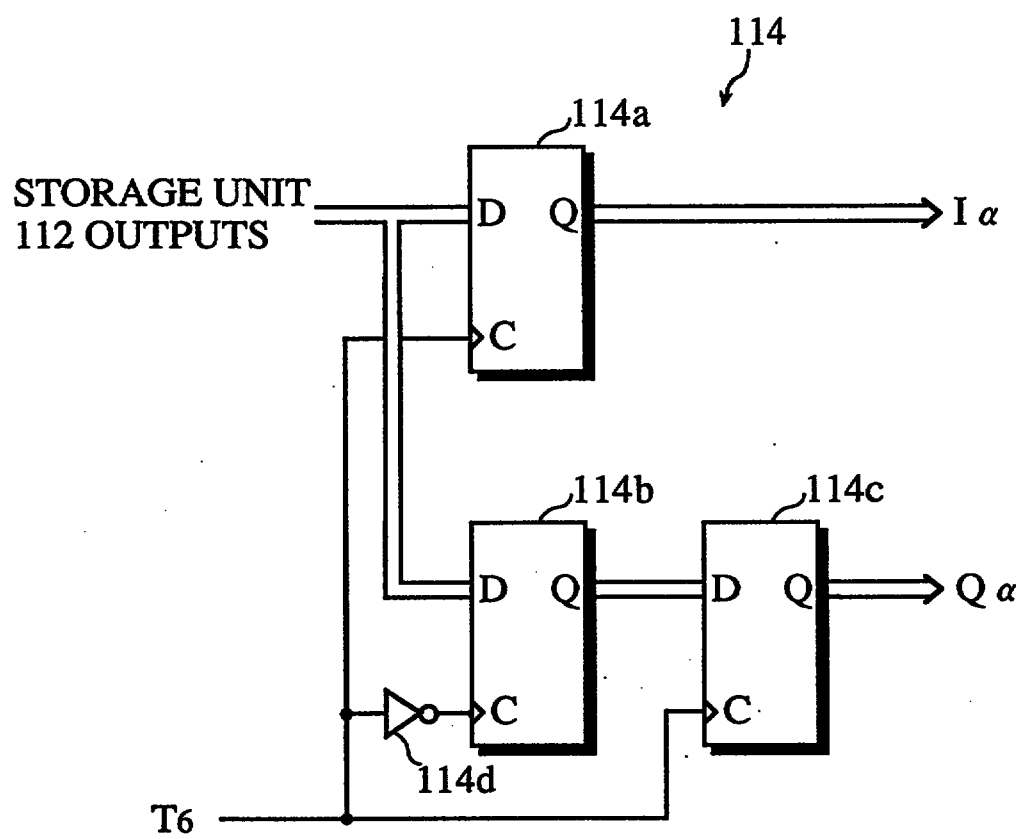
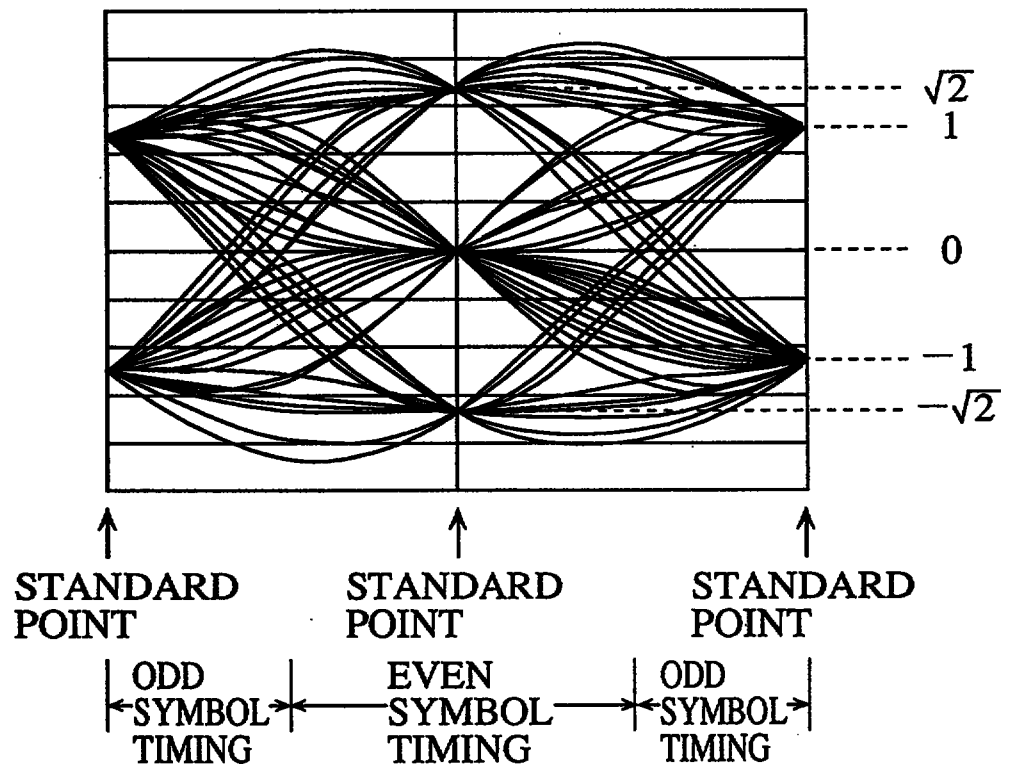


Fig. 9



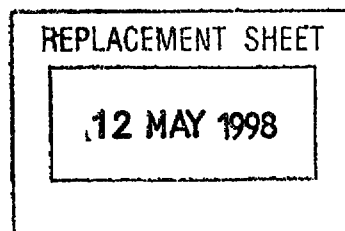


CLAIMS

(This claim amendment was received by the International Bureau April 29, 1997. Of the original claims, only CLAIM 1 has been amended.)

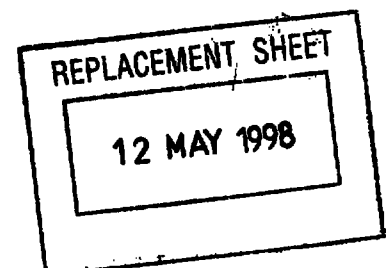
What is claimed is:

- 1 1. (Amended) A phase modulating apparatus comprising:
 - 2 storage means for storing waveform data including a
 - 3 waveform used for rise ramp processing, a plurality of phase
 - 4 waveforms used for both I-component and Q-component of a
 - 5 plurality of transmission symbols, and a waveform used for fall
 - 6 ramp processing;
 - 7 symbol generating means for generating in time series
 - 8 a dummy symbol for the rise ramp processing, the plurality of
 - 9 transmission symbols, and a dummy symbol for the fall ramp
 - 10 processing;
 - 11 converting means for converting each of the dummy symbol
 - 12 for the rise ramp processing, the plurality of transmission
 - 13 symbols, and the dummy symbol for the fall ramp processing into
 - 14 the I-component and the Q-component, wherein the dummy symbol
 - 15 for the rise ramp processing, the plurality of transmission
 - 16 symbols, and the dummy symbol for the fall ramp processing are
 - 17 provided in time series;





18 address providing means for providing alternately during
19 one symbol period the I-component and the Q-component converted
20 by the converting means as addresses of the storage means;
21 separating means for fetching an I-component waveform
22 and a Q-component waveform which are read alternately from the
23 storage means and outputting simultaneously the I-component
24 waveform and the Q-component waveform; and
25 combining means for combining the I-component waveform
26 and the Q-component waveform output from the separating means
27 into a symbol waveform, wherein
28 the storage means includes:
29 an even storage unit for storing waveform data
30 corresponding to even symbols, receiving alternately an I-
31 component and a Q-component from the address providing means as
32 an address in an even symbol period, and outputting alternately
33 an I-component waveform for an even symbol and a Q-component
34 waveform for an even symbol; and
35 an odd storage unit for storing waveform data
36 corresponding to odd symbols, the waveform data having a level
37 $1/\sqrt{2}$ times that of the waveform data stored in the even storage
38 unit, receiving alternately an I-component and a Q-component
39 from the address providing means as an address in an odd symbol
40 period, and outputting alternately an I-component waveform for





41 an odd symbol and a Q-component waveform for an odd symbol.

1 2. The phase modulating apparatus of CLAIM 1, wherein the
2 address providing means comprises:

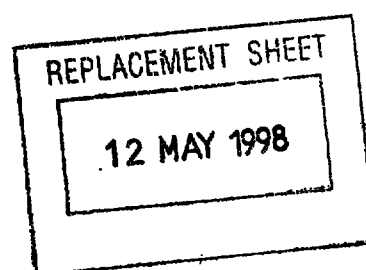
3 timing generating means for generating first timing
4 information which indicates a rise ramp processing section, a
5 transmission section, and a fall ramp processing section and
6 second timing information which indicates the symbol period used
7 in each of the rise ramp processing section, the transmission
8 section, and the fall ramp processing section;

9 selecting means for selecting alternately during one
10 symbol period the I-component and the Q-component converted by
11 the converting means according to the second timing information;
12 and

13 inputting means for inputting an address into the
14 storage means, wherein the address includes a first partial
15 address, which is the first timing information, and second
16 partial address, which is an output from the selecting means.

1 3. The phase modulating apparatus of CLAIM 2, wherein the
2 address providing means further comprises:

3 I-shift register for accumulating I-components of a
4 certain number of symbols converted by the converting means and





5 outputting the I-components in parallel; and

6 Q-shift register for accumulating Q-components of the
7 certain number of symbols converted by the converting means and
8 outputting the Q-components in parallel, wherein

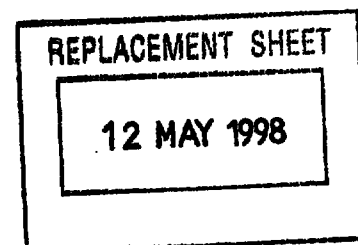
9 the selecting means selects alternately an output from
10 the I-shift register and an output from the Q-shift register.

1 4. The phase modulating apparatus of CLAIM 1, wherein the
2 separating means comprises:

3 first delay means for delaying the I-component waveform
4 output from the storage means; and

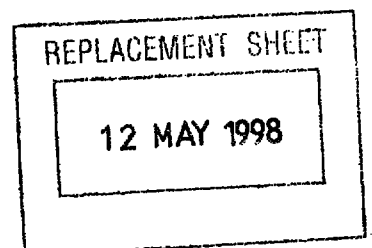
5 second delay means for delaying the Q-component waveform
6 output from the storage means so that the second delay means is
7 synchronized with the first delay means in outputting.

1 5. A $\pi/4$ -shift QPSK modulating apparatus for assigning
2 uniquely a signal point on a two-dimensional coordinate, which
3 has an I-axis and a Q-axis perpendicular to one another, for
4 each set of sequential two bits in serial data input and
5 generating a modulated signal corresponding to a response
6 waveform which is output from a lowpass digital filter at a time
7 when an I-coordinate and a Q-coordinate of the signal point is
8 input, the $\pi/4$ -shift QPSK modulating apparatus comprising:





9 I-coordinate accumulating means for accumulating the I-
10 coordinate and outputting accumulated I-coordinates;
11 Q-coordinate accumulating means for accumulating the Q-
12 coordinate and outputting accumulated Q-coordinates;
13 ramp period notifying means for outputting a ramp period
14 notification signal which indicates a burst rise period for ramp
15 processing, a burst transmission period during which a modulated
16 signal representing transmission data is transmitted, and a
17 burst fall period for ramp processing;
18 clock means for outputting time information and a switch
19 signal, wherein the time information, having a frequency higher
20 than input data, indicates a certain elapsed time, and the
21 switch signal is faster than the time information;
22 switching means for selecting alternately an output from
23 the I-coordinate accumulating means and an output from the Q-
24 coordinate accumulating means according to the switch signal and
25 outputting a selected output;
26 rise ramp means for outputting alternately a burst rise
27 ramp waveform for an I-coordinate filter input and a burst rise
28 ramp waveform for a Q-coordinate filter input according to the
29 ramp period notification signal, an output from the switching
30 means, and the time information;
31 filter means for outputting alternately a filter





32 response waveform for an I-coordinate input and a filter
33 response waveform for a Q-coordinate input according to the ramp
34 period notification signal, an output from the switching means,
35 and the time information;

36 fall ramp means for outputting alternately a burst fall
37 ramp waveform for an I-coordinate filter input and a burst fall
38 ramp waveform for a Q-coordinate filter input according to the
39 ramp period notification signal, an output from the switching
40 means, and the time information; and

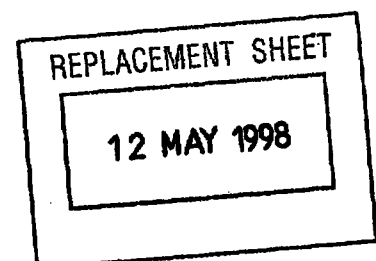
41 separating means for separating each output from the
42 rise ramp means, the filter means, and the fall ramp means into
43 two streams which respectively correspond to the I-coordinate
44 and the Q-coordinate.

1 6. The $\pi/4$ -shift QPSK modulating apparatus of CLAIM 5,
2 wherein

3 the I-coordinate accumulating means comprises:

4 odd I-coordinate accumulating means for accumulating I-
5 coordinates of odd signal points in the serial data input and
6 outputting an I-coordinate sequence including a certain number
7 of accumulated I-coordinates; and

8 even I-coordinate accumulating means for accumulating
9 I-coordinates of even signal points in the serial data input and





10 outputting an I-coordinate sequence including the certain number
11 of accumulated I-coordinates, wherein

12 the Q-coordinate accumulating means comprises:

13 odd Q-coordinate accumulating means for accumulating Q-
14 coordinates of odd signal points in the serial data input and
15 outputting an Q-coordinate sequence including the certain number
16 of accumulated Q-coordinates; and

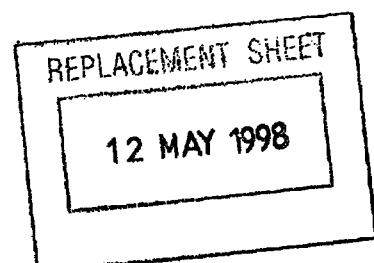
17 even Q-coordinate accumulating means for accumulating
18 Q-coordinates of even signal points in the serial data input and
19 outputting an Q-coordinate sequence including the certain number
20 of accumulated Q-coordinates, wherein

21 the switching means comprises:

22 odd switching means for selecting alternately an output
23 from the odd I-coordinate accumulating means and an output from
24 the odd Q-coordinate accumulating means according to the switch
25 signal and outputting a selected output; and

26 even switching means for selecting alternately an output
27 from the even I-coordinate accumulating means and an output from
28 the even Q-coordinate accumulating means according to the switch
29 signal and outputting a selected output, wherein

30 the rise ramp means, the filter means, and the fall ramp
31 means include an odd storage unit and an even storage unit,
32 wherein





33 the odd storage unit stores response waveform data of
34 a digital filter and also stores burst rise ramp waveform data
35 and burst fall ramp waveform data which each correspond to the
36 response waveform data of the digital filter, wherein the
37 response waveform data of the digital filter corresponds to an
38 I-coordinate and a Q-coordinate which are determined by two bits
39 at odd input data which is indicated by addresses, namely, the
40 ramp period notification signal, an output from the switching
41 means, and the time information, wherein

42 the even storage unit stores response waveform data of
43 a digital filter and also stores burst rise ramp waveform data
44 and burst fall ramp waveform data which each correspond to the
45 response waveform data of the digital filter, wherein the
46 response waveform data of the digital filter corresponds to an
47 I-coordinate and a Q-coordinate which are determined by two bits
48 at even input data which is indicated by addresses, namely, the
49 ramp period notification signal, an output from the switching
50 means, and the time information.

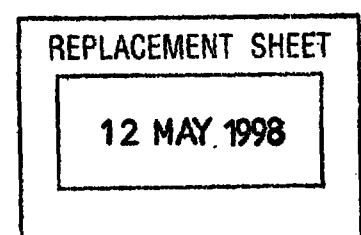
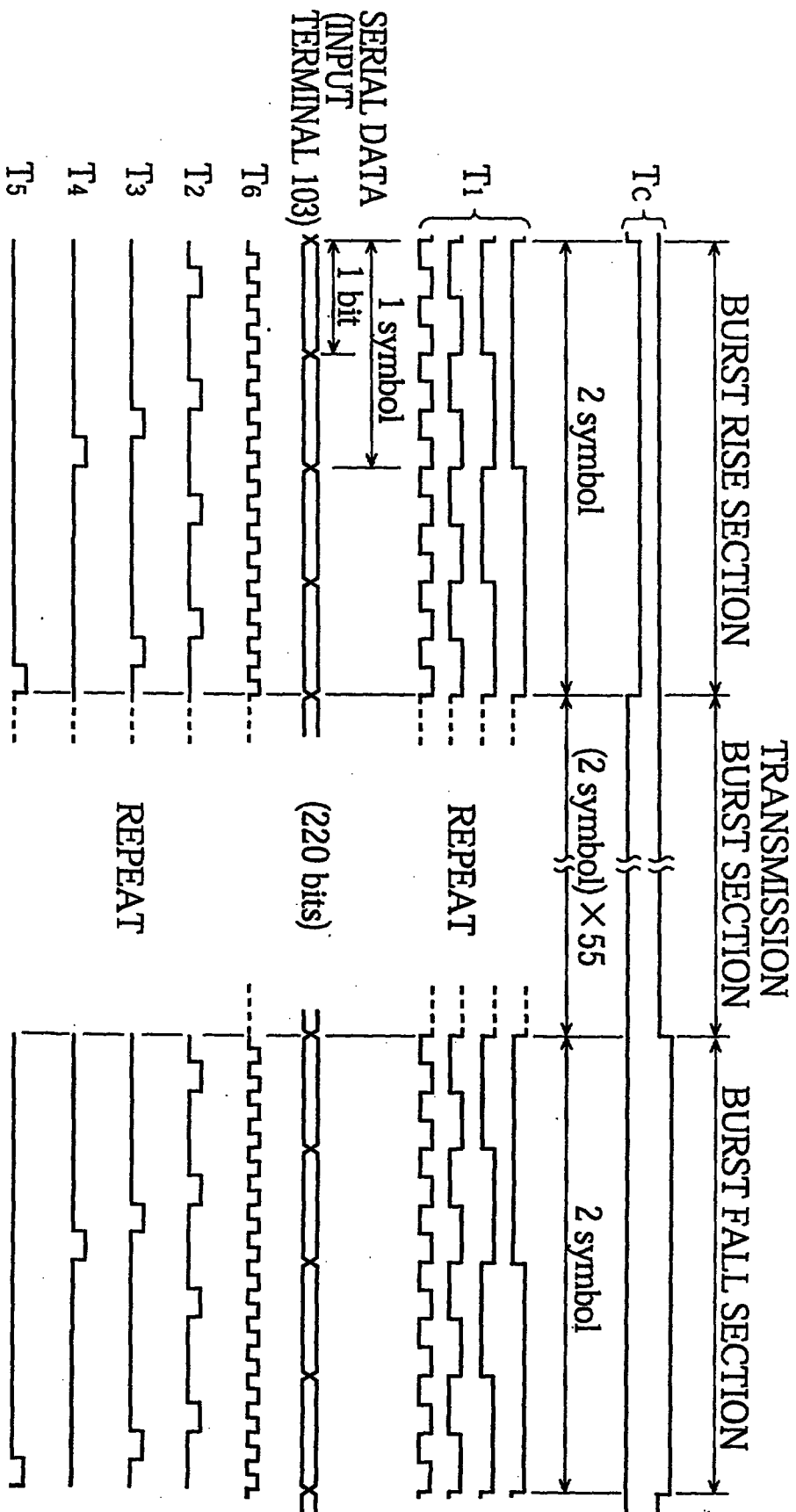


Fig. 5



REPLACEMENT SHEET

12 MAY 1998