

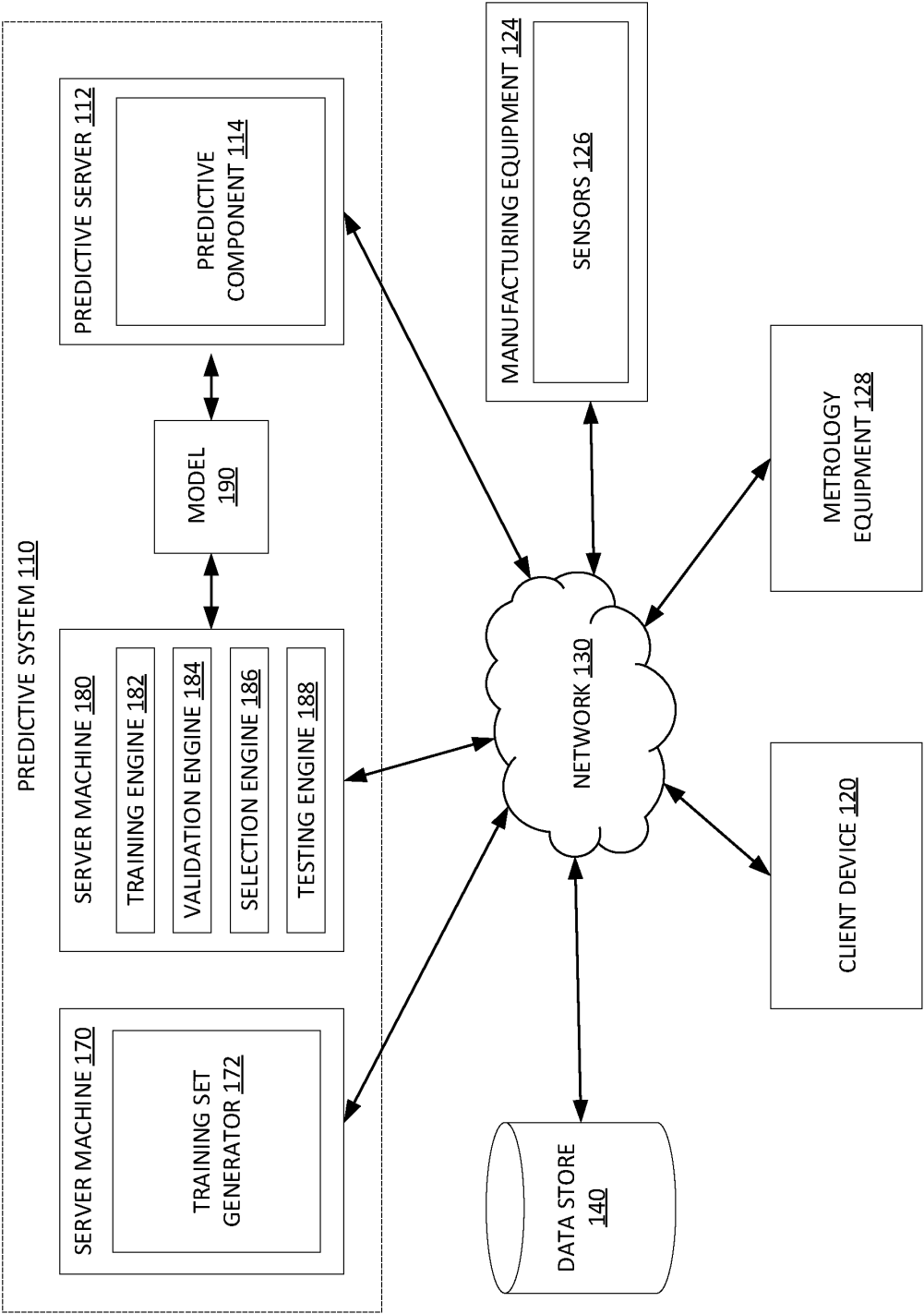
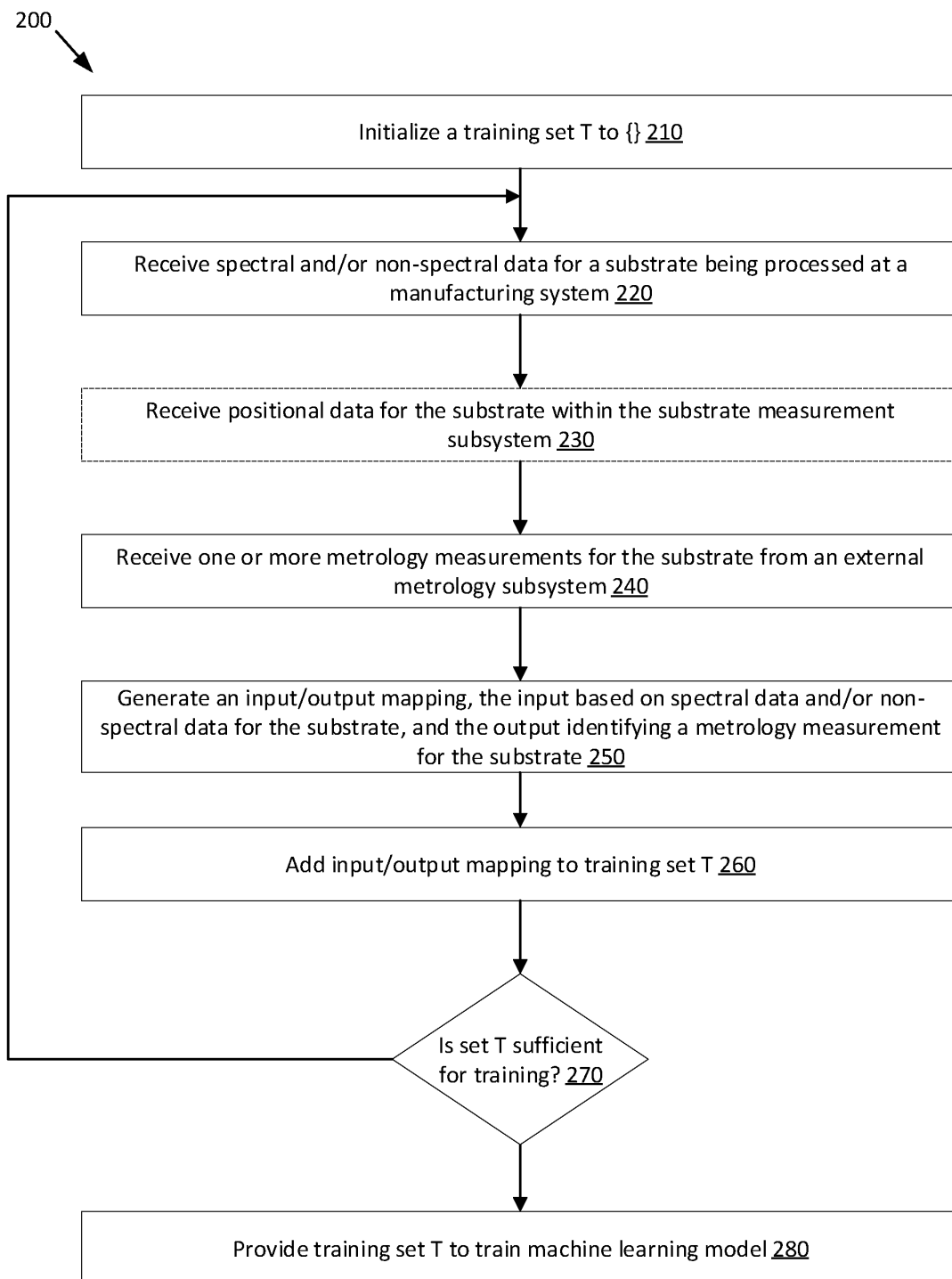


FIG. 1

**FIG. 2**

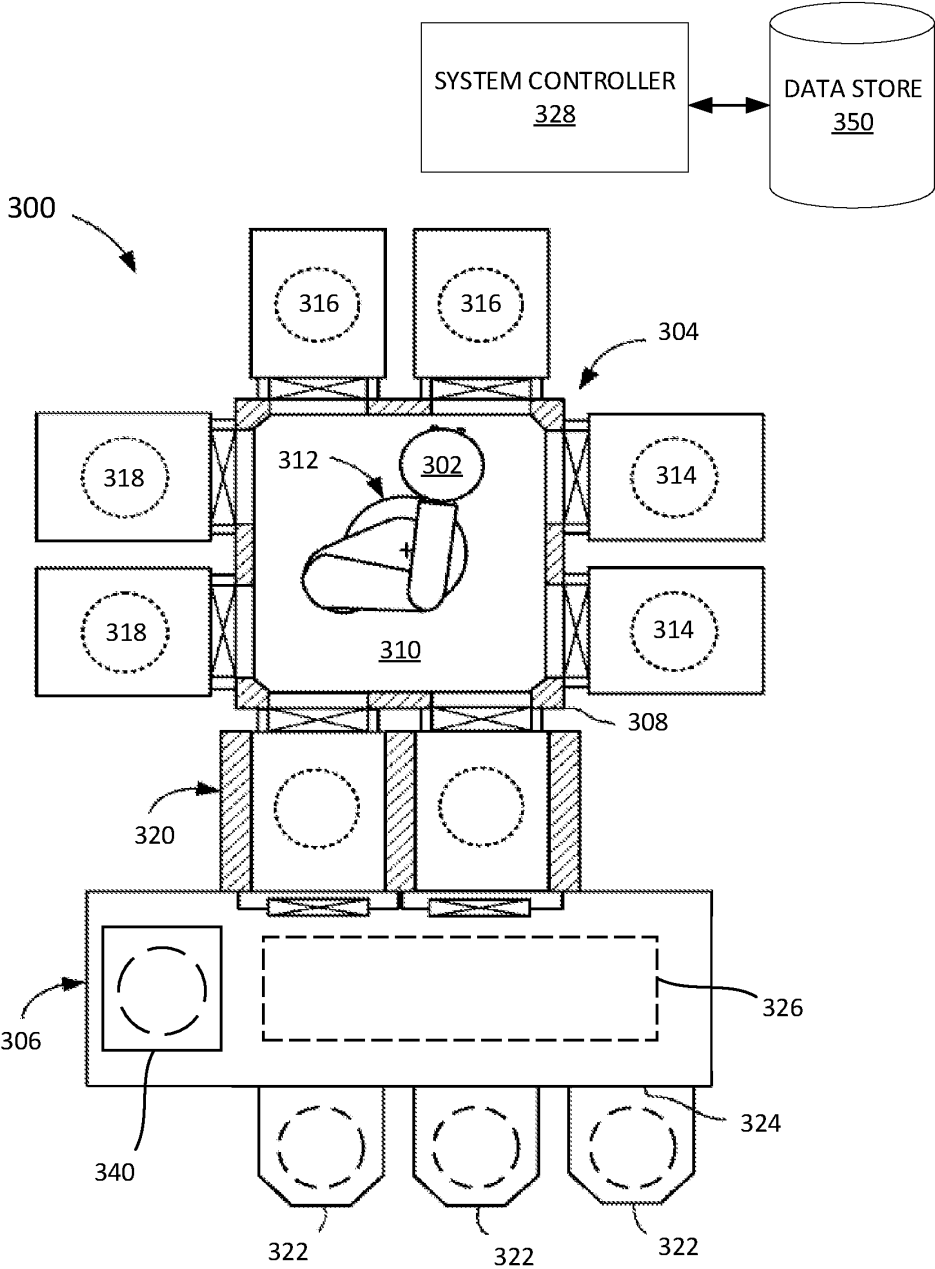


FIG. 3

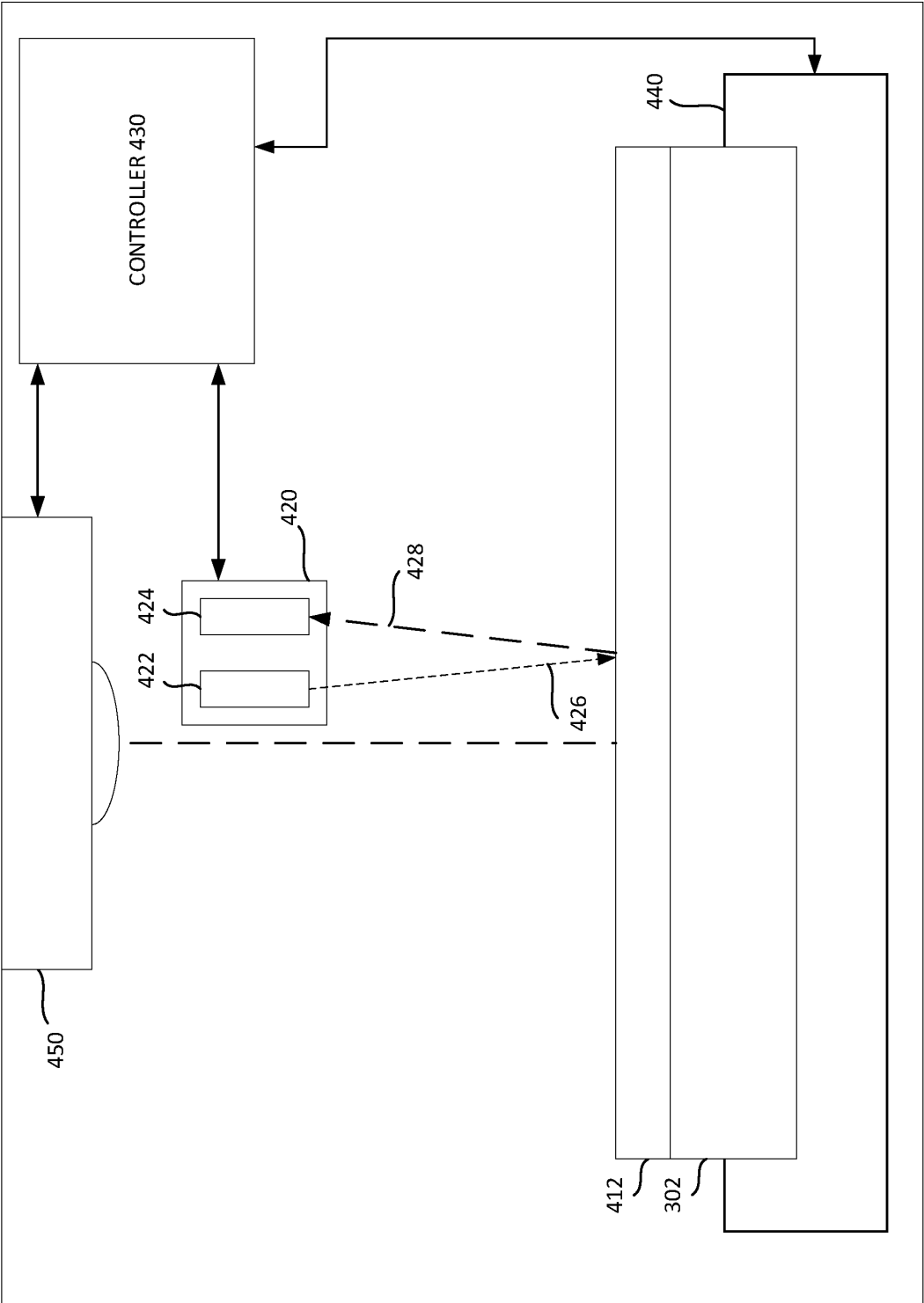


FIG. 4

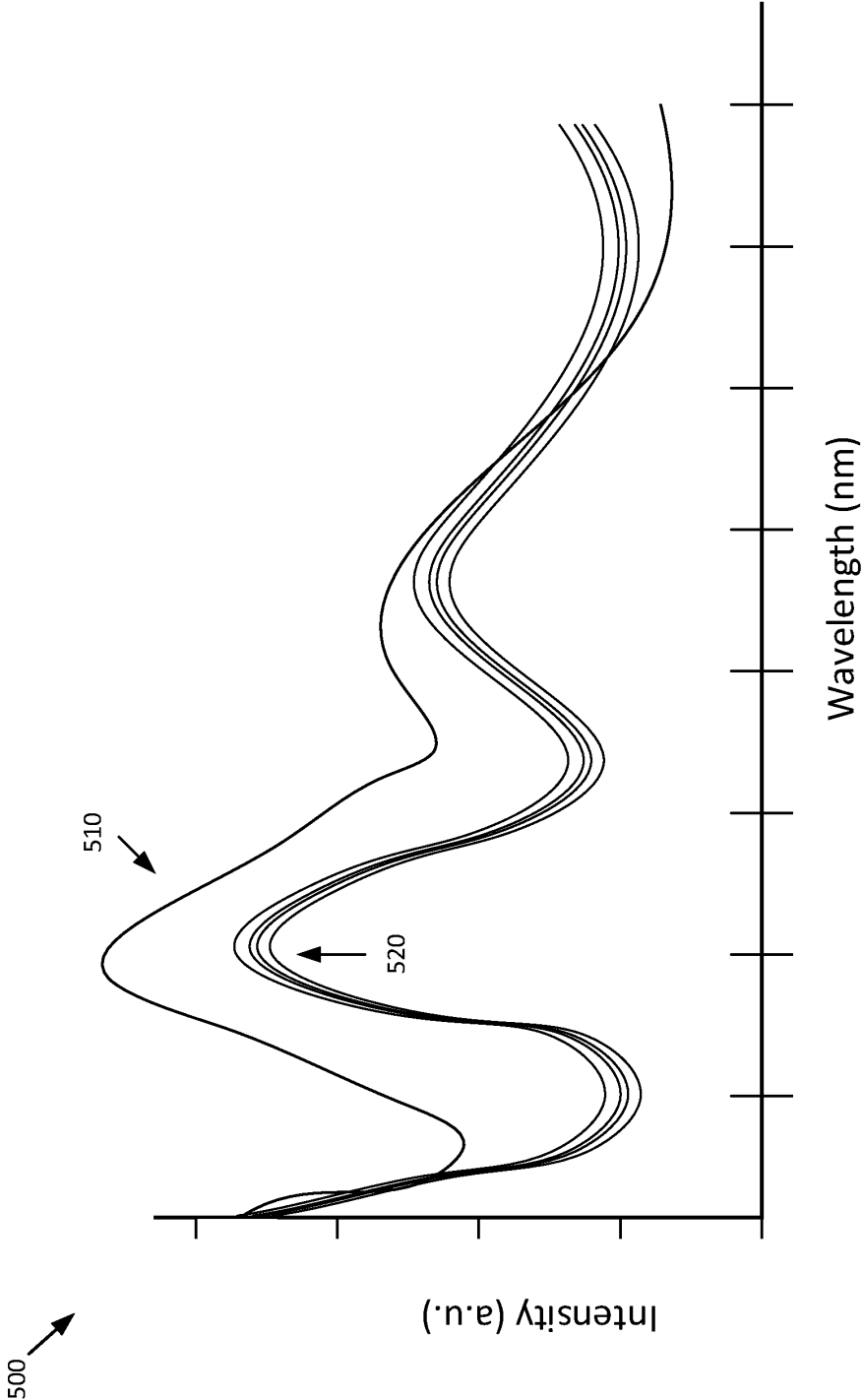
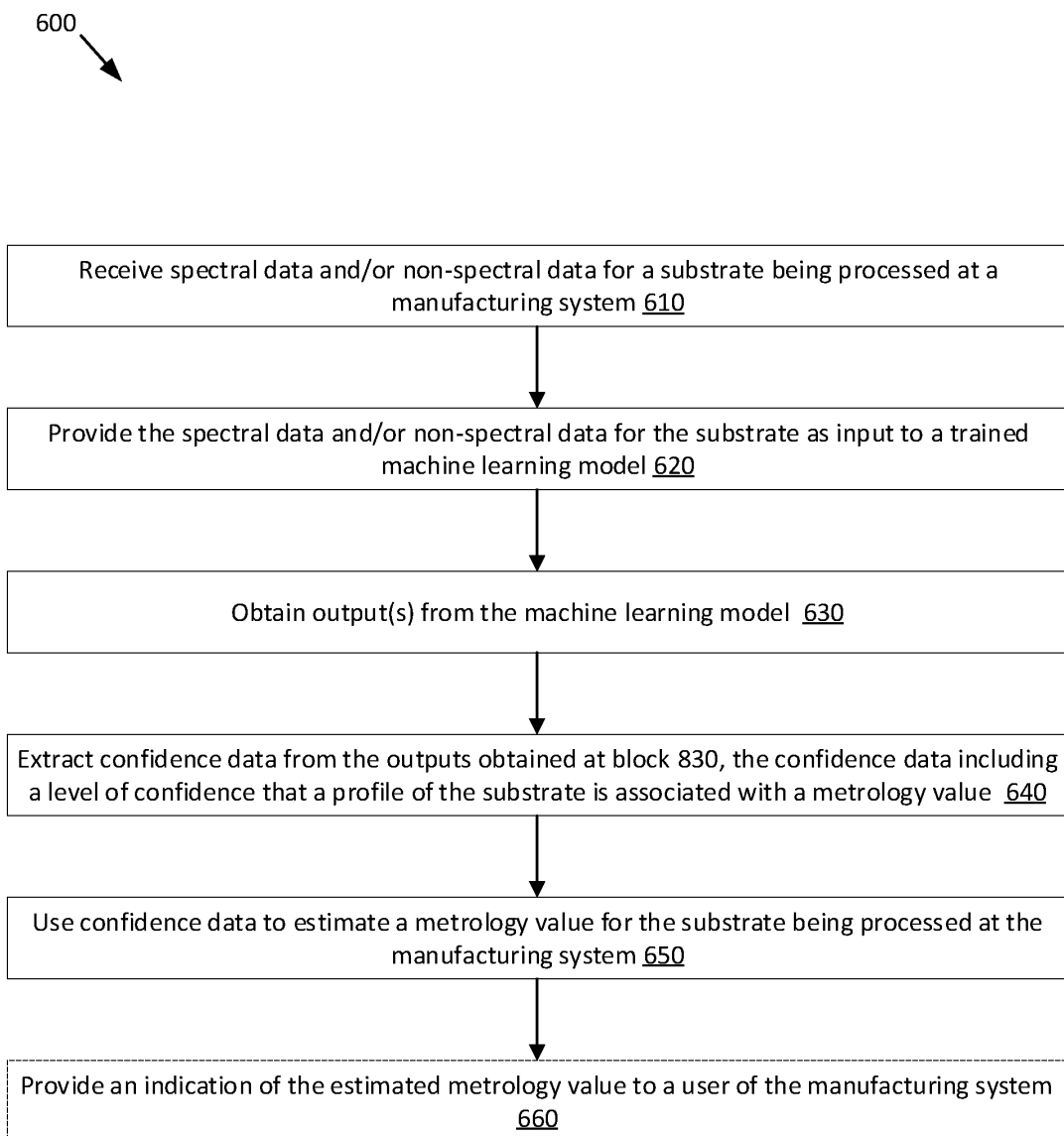


FIG. 5

**FIG. 6**

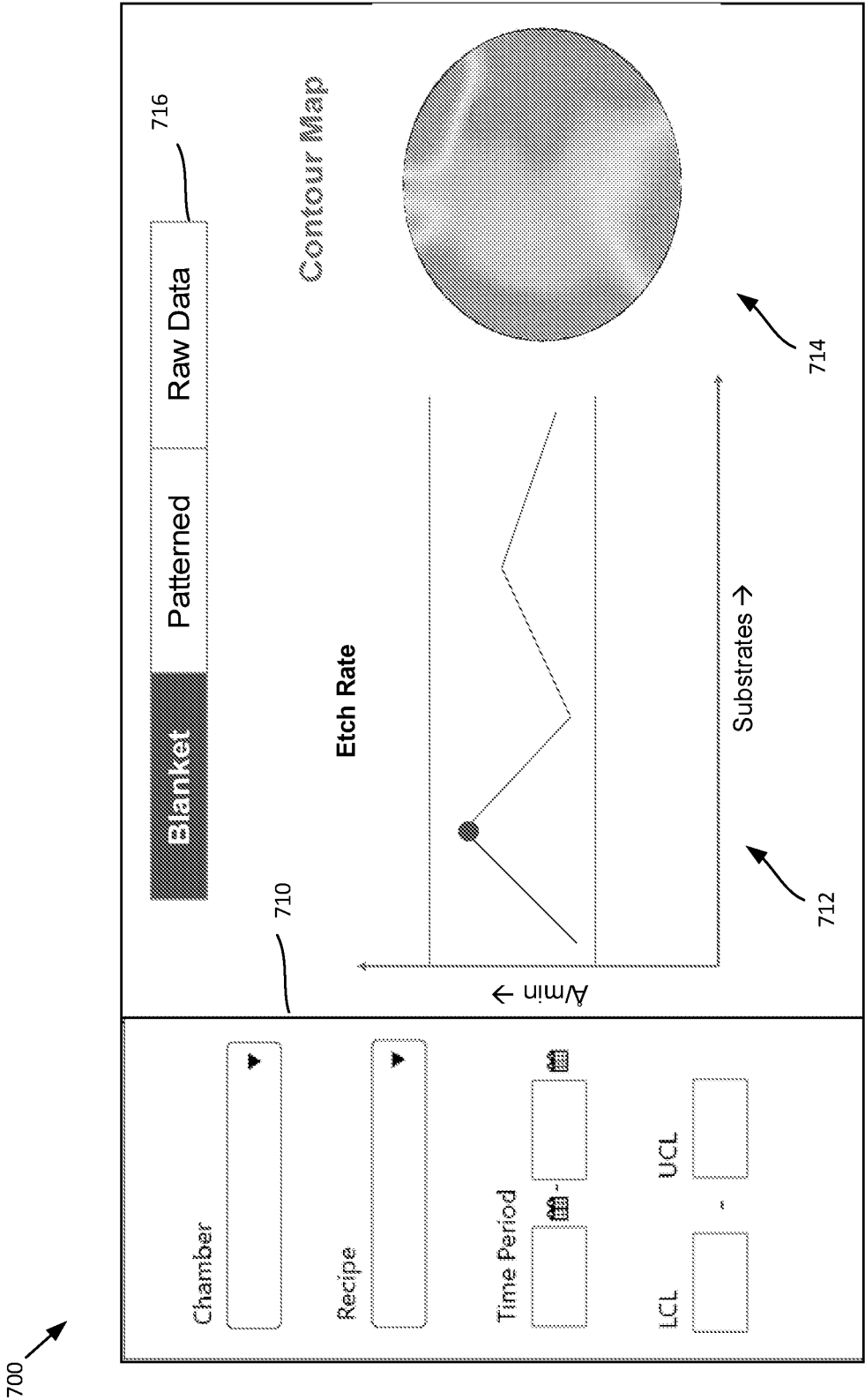


FIG. 7A

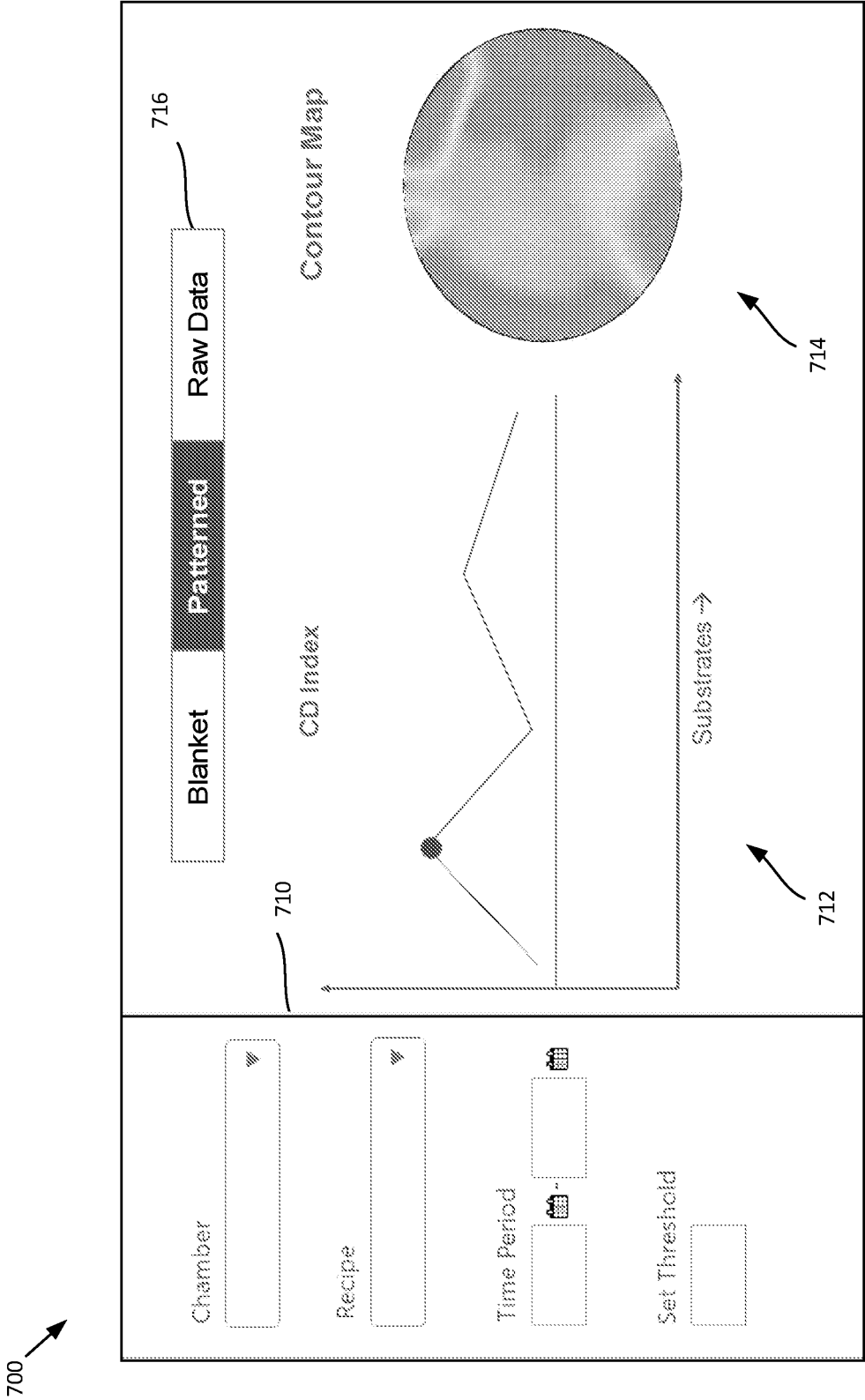


FIG. 7B

700

Chamber

Recipe

Time Period

Set Threshold

710

Blanket

Patterned

Raw Data

716

Timestamp	Lot ID	Wafer ID	Recipe	Operation	Loop	X	Y	Model Thickness
1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6	6
7	7	7	7	7	7	7	7	7
8	8	8	8	8	8	8	8	8
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720

FIG. 7C

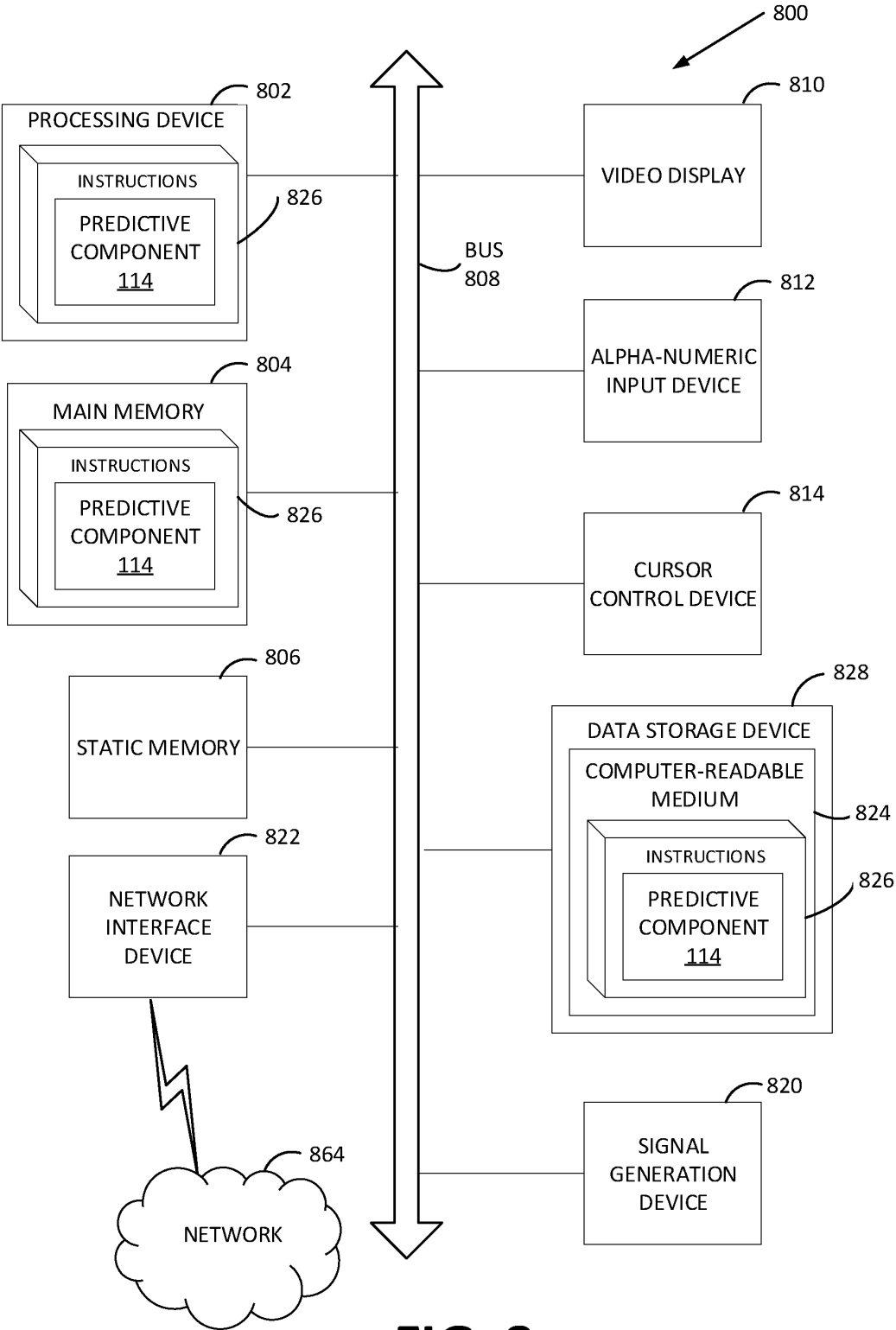


FIG. 8