What is claimed is:

1. (Original) A phase change memory cell, comprising:

a vertical transistor including a bottom electrode on a pillar;

a dielectric on a top surface of a portion of the bottom electrode;

a top electrode on the dielectric;

a phase change material on a side surface of the top electrode, on a side surface of the dielectric, and on a top surface of the bottom electrode.

2. (Original) The phase change memory cell of claim 1, wherein a width of the phase change material is less than a width of the top surface of the bottom electrode.

3. (Original) The phase change memory cell of claim 1, wherein a width of the phase change material is less than a width of the side surface of the top electrode.

4. (Original) The phase change memory cell of claim 1, wherein the phase change memory cell includes additional phase change material on an opposite side surface of the top electrode and on an opposite side surface of the dielectric.

5. (Original) The phase change memory cell of claim 1, wherein the phase change memory cell includes an additional dielectric on a side surface of the phase change material opposite the side surface of the top electrode and opposite the side surface of the dielectric.

6. (Original) The phase change memory cell of claim 1, wherein the phase change material includes an active region on the dielectric between the top electrode and the bottom electrode.

7. (Original) The phase change memory cell of claim 1, wherein the phase change material extends from a top surface of the top electrode to a top surface of the bottom electrode.

8. (Original) A phase change memory cell, comprising:

a vertical transistor including a vertical line electrode;

a dielectric on a top surface of a portion of the vertical line electrode;

a top electrode on a top surface of the dielectric; and

a phase change material on a side surface of the top electrode, on a side surface of the dielectric, and on a top surface of the vertical line electrode.

9. (Original) The phase change memory cell of claim 8, wherein the phase change material is in point contact with the vertical line electrode.

10. (Original) The phase change memory cell of claim 9, wherein the phase change material includes an active region on the dielectric and on the point contact.

11. (Original) The phase change memory cell of claim 8, wherein the phase change memory cell includes a spacer surrounding side surfaces of the vertical line electrode.

12. (Original) The phase change memory cell of claim 8, wherein the top electrode comprises a data line.

13. (Original) The phase change memory cell of claim 8, wherein the vertical transistor is a metal oxide semiconductor field effect transistor (MOSFET).

14. (Original) An array of phase change memory cells, comprising:

a dielectric on an array of vertical transistors;

an electrode on the dielectric; and

a phase change material on, and in contact with, the dielectric and the electrode by a common plane, wherein the phase change material is on, and in contact with, a number of vertical transistors of the array of vertical transistors.

15. (Original) The array of phase change memory cells of claim 14, including removed portions of the dielectric and the electrode, wherein the removed portions are separated by one feature width spans of remaining

dielectric and electrode, and wherein the remaining dielectric and electrode span from a position above a particular vertical transistor to a position between the particular vertical transistor and an adjacent vertical transistor in a first direction.

16. (Original) The array of phase change memory cells of claim 15, wherein the phase change material is at least on top of the electrode, on the side of the electrode, on the side of the dielectric, and on top of the array of vertical transistors.

17. (Original) The array of phase change memory cells of claim 16, wherein the array includes an additional dielectric on the phase change material; and

wherein removed portions of the additional dielectric and the phase change material extend to a depth equal to the thickness of the formed additional dielectric and the phase change material.

18. (Original) The array of phase change memory cells of claim 17, wherein removed portions of the additional dielectric and phase change material extend from above a distal edge of a first vertical transistor to above a proximal edge of a second vertical transistor adjacent to the first vertical transistor in a second direction.

What is claimed is:

1. A method of processing a phase change memory cell, comprising:

forming a dielectric on at least a portion of a vertical transistor;

forming an electrode on the dielectric; and

forming a vertical strip of phase change material on a portion of a side of the electrode and on a portion of a side of the dielectric extending along the electrode and the dielectric into contact with the vertical transistor.

2. The method of claim 1, wherein the method includes:

forming the dielectric on an array of vertical transistors; and

removing portions of the electrode and the dielectric, wherein removed portions are separated by two feature widths in a first direction.

3. The method of claim 2, wherein the method includes removing portions of the electrode and the dielectric such that the two feature widths in the first direction span from a position above a first vertical transistor near a center point of the first vertical transistor to a position above a second vertical transistor adjacent to the first vertical transistor near a center point of the second vertical transistor.

4. The method of claim 2, wherein forming the vertical strip of phase change material includes conformally depositing the phase change material at least on top of the electrode, on the side of the electrode, on the side of the dielectric, and on top of the vertical transistor.

5. The method of claim 4, wherein the method includes:

conformally depositing an additional dielectric on the phase change material; and

removing material from a top of the array of vertical transistors to a depth equal to a thickness of the conformal deposition of the additional dielectric plus a thickness of the conformal deposition of the phase change material.

6. The method of claim 5, wherein the method includes removing one feature width of material in the first direction between the portions separated by two feature widths to a

height of the array of vertical transistors.

7. The method of claim 6, wherein the method includes removing portions of the phase change material between adjacent vertical transistors in a second direction.

8. A method of processing phase change memory cells, comprising:

forming a dielectric on an array of vertical transistors;

forming an electrode on the dielectric; and

forming a phase change material on, and in contact with, the dielectric and the electrode by a common plane, wherein the phase change material is on, and in contact with, a number of vertical transistors of the array of vertical transistors.

9. The method of claim 8, wherein the method includes removing portions of the dielectric and the electrode, wherein the removed portions are separated by one feature width spans of remaining dielectric and electrode, and wherein the remaining dielectric and electrode span from a position above a particular vertical transistor to a position between the particular vertical transistor and an adjacent vertical transistor in a first direction.

10. The method of claim 9, wherein forming the phase change material includes conformally depositing the phase change material at least on top of the electrode, on the side of the electrode, on the side of the dielectric, and on top of the array of vertical transistors.

11. The method of claim 10, wherein the method includes:

conformally depositing an additional dielectric on the phase change material; and

removing portions of the additional dielectric and the phase change material to a depth equal to the thickness of the formed additional dielectric and the phase change material.

12. The method of claim 11, wherein the method includes removing portions of the additional dielectric and phase change material extending from above a distal edge of a

first vertical transistor to above a proximal edge of a second vertical transistor adjacent to the first vertical transistor in a second direction.

13. A method of processing phase change memory cells, comprising:

forming a spacer on an exposed pillar of a vertical transistor;

forming a vertical line electrode between the spacer on the exposed pillar of the vertical transistor;

forming a dielectric on at least a portion of the vertical line electrode;

forming a top electrode on the dielectric; and

forming a phase change material on and in contact with the vertical line electrode, the dielectric, and the top electrode.

14. The method of claim 13, wherein forming the spacer includes forming the spacer around an inner periphery of the exposed pillar of the vertical transistor.

15. The method of claim 13, wherein forming the phase change material includes:

forming the phase change material on a top surface of the vertical line electrode;

forming the phase change material on a side surface of the dielectric; and

forming the phase change material on a side surface of the top electrode.

16. The method of claim 13, wherein forming the phase change material includes forming a vertical line of phase change material in a direction orthogonal to a direction of the vertical line electrode.

17. The method of claim 13, wherein the method includes forming an additional dielectric on a side surface of the phase change material.

18. A phase change memory cell, comprising:

a vertical transistor including a bottom electrode on a pillar;

a dielectric on a top surface of a portion of the bottom electrode;

a top electrode on the dielectric;

a phase change material on a side surface of the top electrode, on a side surface of

the dielectric, and on a top surface of the bottom electrode.

19. The phase change memory cell of claim 18, wherein a width of the phase change material is less than a width of the top surface of the bottom electrode.

20. The phase change memory cell of claim 18, wherein a width of the phase change material is less than a width of the side surface of the top electrode.

21. The phase change memory cell of claim 18, wherein the phase change memory cell includes additional phase change material on an opposite side surface of the top electrode and on an opposite side surface of the dielectric.

22. The phase change memory cell of claim 18, wherein the phase change memory cell includes an additional dielectric on a side surface of the phase change material opposite the side surface of the top electrode and opposite the side surface of the dielectric.

23. The phase change memory cell of claim 18, wherein the phase change material includes an active region on the dielectric between the top electrode and the bottom electrode.

24. The phase change memory cell of claim 18, wherein the phase change material extends from a top surface of the top electrode to a top surface of the bottom electrode.

25. A phase change memory cell, comprising:

a vertical transistor including a vertical line electrode;

a dielectric on a top surface of a portion of the vertical line electrode;

a top electrode on a top surface of the dielectric; and

a phase change material on a side surface of the top electrode, on a side surface of the dielectric, and on a top surface of the vertical line electrode.

26. The phase change memory cell of claim 25, wherein the phase change material is

in point contact with the vertical line electrode.

27. The phase change memory cell of claim 26, wherein the phase change material includes an active region on the dielectric and on the point contact.

28. The phase change memory cell of claim 25, wherein the phase change memory cell includes a spacer surrounding side surfaces of the vertical line electrode.

29. The phase change memory cell of claim 25, wherein the top electrode comprises a data line.

30. The phase change memory cell of claim 25, wherein the vertical transistor is a metal oxide semiconductor field effect transistor (MOSFET).