ABSTRACT

METHOD OF GATE PATTERNING FOR SUB-0.1μm TECHNOLOGY

A method of gate patterning, including the following steps. A semiconductor structure having an upper silicon layer is provided. The semiconductor structure has a gate conductor region. A first gate oxide layer is formed over the semiconductor structure. A polysilicon layer is formed over the first gate oxide layer. A patterned oxide mask and photoresist layer are formed over the polysilicon layer within the gate conductor region leaving unmasked polysilicon layer portions and unmasked first gate oxide layer portions. An oxygen implant is conducted within the unmasked polysilicon layer portions proximate the unmasked first gate oxide layer portions. The patterned photoresist mask is removed. The structure is annealed to form second gate oxide portions within the unmasked polysilicon layer portions over the unmasked first gate oxide layer portions. The unmasked polysilicon layer portions are etched and removed to the second gate oxide portions forming a polysilicon gate conductor within the gate conductor region.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)