

METHOD FOR CORRECTING ANALOG EQUALIZER, AND CONTROL CHIP, RECEIVER AND STORAGE MEDIUM

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Chinese Patent Application No. 202011289876.4, filed on November 17, 2020, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present application relates to digital signal communication, for example, to a method for correcting an analog equalizer, a control chip, a receiver and a storage medium.

BACKGROUND

[0003] Continuous Time Linear Equalization (CTLE) is an analog filter at the signal receiving end, also known as an analog equalizer. When a high-speed digital signal is transmitted through a lossy channel, CTLE can be used to increase the high-frequency component of the signal to compensate for the loss of the high-frequency channel, and improve the performance of the receiver and the quality of the received signal. As the signal transmission rate continues to increase, the attenuation of the signal by channels such as long-distance backplanes becomes more serious, and the intersymbol interference becomes more serious, which makes the equalization processing of the signal more complicated. If the compensation degree is too large or too small, the signal will be distorted, which is not conducive to subsequent detection and processing. This requires the receiving end to be able to adjust and correct CTLE, so as to moderately compensate for high-frequency channel loss and achieve optimal performance of the receiving circuit.

[0004] The principle of correction is mainly to increase the amplitude of the high-frequency signal in the high-speed serial signal by adjusting the high-frequency gain of CTLE. Correction is done when the amplitude of the high-frequency signal is equal to that of the low-frequency signal, but this method requires the design of a rectifier circuit. There are also some methods to correct CTLE through analog circuits, but complex high-pass or low-pass filters need to be

designed, and the correction process is easily affected by channel quality and data rate. CTLE can also be corrected by counting the bit error rate. When the bit error rate reaches the minimum, the correction is considered complete, but this method needs to predict the transmission data to count the bit error rate. CTLE can also be corrected by using the variable step-size least mean square (LMS) algorithm and the zero-forcing least mean square error algorithm, but the calculation of the correction process is complicated.

SUMMARY

[0005] Embodiments of the present application provide a method for correcting an analog equalizer, including:

[0006] monitoring a positive eye height of an output signal of an analog front end (AFE) circuit, the AFE circuit including at least one stage of analog equalizer;

[0007] generating a correction instruction in response to that the monitored positive eye height is lower than an eye height threshold; and

[0008] correcting the analog equalizer in the AFE circuit according to the correction instruction until the monitored positive eye height reaches the eye height threshold.

[0009] Embodiments of the present application further provide a control chip, including: a memory, a processor, and a computer program stored on the memory and operable on the processor, when the computer program is executed by the processor, the method for correcting the analog equalizer as described above is implemented.

[0010] Embodiments of the present application further provide a receiver, including: an analog front end (AFE) circuit; a monitoring circuit; and the control chip as described above,

[0011] an output end of the AFE circuit is connected to an input end of the monitoring circuit, an output end of the monitoring circuit is connected to an input end of the control chip, and the control chip is configured to correct an analog equalizer in the AFE circuit according to a monitoring result of the monitoring circuit.

[0012] Embodiments of the present application further provide a computer-readable storage medium, a computer program is stored on the computer-readable storage medium, and when the computer program is executed by a processor, the method for correcting an analog equalizer as described above is implemented.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 is a flowchart of a method for correcting an analog equalizer according to an embodiment of the present application.

[0014] FIG. 2 is a flowchart of a method for correcting an analog equalizer according to another embodiment of the present application.

[0015] FIG. 3 is a schematic structural diagram of a device for correcting an analog equalizer according to an embodiment of the present application.

[0016] FIG. 4 is a schematic diagram of a hardware structure of a control chip according to an embodiment of the present application.

[0017] FIG. 5 is a schematic structural diagram of a receiver according to an embodiment of the present application.

[0018] FIG. 6 is a schematic diagram of a working principle of a receiver according to an embodiment of the present application.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0019] The present application will be described below in conjunction with the accompanying drawings and embodiments. It should be understood that the specific embodiments described herein are only used to explain the present application, but not to limit the present application. It should be noted that, in the case of no conflict, the embodiments in the present application and the features in the embodiments can be combined arbitrarily with each other. In addition, it should be noted that, for the convenience of description, only some structures related to the present application are shown in the drawings but not all structures.

[0020] FIG. 1 is a flowchart of a method for correcting an analog equalizer provided by an embodiment. The method can be applied to a control chip of a receiver. As shown in FIG. 1, the method provided by this embodiment includes the operations 110 to 130.

[0021] At operation 110, monitoring a positive eye height of an output signal of an analog front end (AFE) circuit, the AFE circuit including at least one stage of analog equalizer.

[0022] In this embodiment, the transmitter sends high-speed serial data signals to the receiver. After the channel attenuation, the intersymbol interference becomes very serious. The receiver compensates the channel attenuation through the AFE circuit, which can reduce the intersymbol interference. The AFE circuit may include digital circuit devices and analog circuit devices, and may include at least one stage of CTLE. CTLE can increase the high-frequency component of

the signal to compensate for high-frequency channel loss, improve the performance of the receiver and the quality of the received signal.

[0023] An eye diagram is a graph representing a series of digital signals accumulated and displayed on an oscilloscope, which is configured to analyze the characteristics of the digital signal, analyze the influence of intersymbol interference and noise, so as to estimate the quality of the received digital signal. The positive eye height is configured to describe the size of the “eye” opening in the eye diagram, reflecting the strength of the intersymbol interference. The higher the positive eye height and the more correct the eye diagram, the smaller the intersymbol interference; otherwise, the greater the intersymbol interference. In this embodiment, the compensation ability of CTLE is adjusted according to the positive eye height to reduce the intersymbol interference and improve the performance of the receiver. The control chip determines whether CTLE needs to be corrected and the strategy for correcting CTLE by monitoring the positive eye height of the output signal of the AFE circuit in real time, such as, whether to enable the compensation function of CTLE at all stages, whether to adjust the high-frequency gain or low-frequency gain, or the like.

[0024] At operation 120, generating a correction instruction in response to that the monitored positive eye height is lower than an eye height threshold.

[0025] In this embodiment, the eye height threshold is set to measure the circuit equalization effect of CTLE. If the positive eye height is lower than the eye height threshold, it means that the inter-symbol interference is large, and the current AFE circuit cannot effectively compensate for high-frequency channel loss, and CTLE needs to be corrected. If the positive eye height reaches the eye height threshold, it means that the intersymbol interference is small and can meet the requirements, and there is no need to correct the CTLE. The correction instruction can be used to control and adjust the compensation capability of CTLE. When the positive eye height is lower than the eye height threshold, the positive eye height can be increased to meet the demand by changing the number of CTLE stages that enable the compensation function and adjusting the high-frequency gain or low-frequency gain of the CTLE.

[0026] In an embodiment, the eye height threshold can be a fixed value or an adjustable dynamic value, which can be set or adjusted according to the channel type of signal transmission, the length of the backplane, the degree of channel attenuation, and the number of CTLE stages. For example, if the degree of channel attenuation is large, the quality of the received signal is poor, and the eye height threshold can be appropriately reduced to obtain an equalized signal that can meet actual needs. If the degree of channel attenuation is small, the eye height threshold can be appropriately increased to obtain a higher-quality equalized signal. For another example, the

more stages of CTLE, the stronger the compensation capability of the AFE circuit, and the eye height threshold can be appropriately increased to obtain a higher-quality equalized signal.

[0027] At operation 130, correcting the analog equalizer in the AFE circuit according to the correction instruction until the monitored positive eye height reaches the eye height threshold.

[0028] In this embodiment, correcting the CTLE includes controlling on-off of the compensation functions of the CTLEs at all stages, and/or adjusting the gains of the CTLEs at all stages, and the correction process can be performed in layers. For example, firstly, when the compensation function of each stage of CTLE is turned off, it is determined whether the currently monitored positive eye height is lower than the eye height threshold, and if so, the compensation function of the first-stage CTLE can be turned on. In the case of enabling the compensation function of the first-stage CTLE, the high-frequency gain of the CTLE is gradually increased. If the monitored positive eye height is still lower than the eye height threshold after increasing to the upper limit, the compensation function of the two-stage CTLE can be turned on, and then the high-frequency gain of the CTLE is gradually increased until the positive eye height reaches the eye height threshold. By analogy, at most all CTLE compensation functions in the AFE circuit can be turned on. Besides, if the positive eye height cannot reach the eye height threshold simply by increasing the high-frequency gain, the low-frequency gain can also be reduced to further increase the overall compensation capability of the CTLE, so that the receiver can achieve optimal performance.

[0029] In this embodiment, there is no need to preset data code patterns, count the bit error rate, and there is no need for the complex mathematical algorithm. The method is used in any channel attenuation scenario, the circuit structure is simple and easy to implement. The positive eye height is taken as the basis for correction, the analog equalizer is corrected to make the positive eye height of the signal high enough to improve the quality of the eye diagram and the output signal of the AFE circuit, thereby realizing the adaptive correction of the analog equalizer.

[0030] In an embodiment, the correction instruction includes a compensation function enabling instruction, and the compensation function enabling instruction is configured to instruct to enable a compensation function of the analog equalizer in the AFE circuit.

[0031] In this embodiment, the compensation function enabling instruction is configured to instruct to enable the compensation function of CTLE at any stage in the AFE circuit. The more stages of CTLEs that enable the compensation function, the stronger the ability of the AFE circuit to compensate for high-frequency attenuation. For example, if the AFE circuit includes three stages of CTLE, which are CTLE 1, CTLE 2, and CTLE 3, respectively, then in the initial stage of the calibration process, only the compensation function of CTLE 1 can be turned on. If

the required positive eye height cannot be obtained by adjusting the gain in this case, the compensation function enabling instruction is updated to instruct to enable the compensation function of CTLE 1 and CTLE 2. Similarly, if the required positive eye height cannot be obtained by adjusting the gain in this case, the compensation function enabling instruction is updated to instruct to enable the compensation functions of CTLE 1, CTLE 2 and CTLE 3. The compensation function enabling instruction can be expressed as: CTLE_BOOST_EN<x:0>, x represents the number of bits of the control code, for example, the two-bit control code can indicate the number of stages of CTLE that enables the compensation function, and the maximum number of stages is 4. By enabling the CTLE compensation function stage by stage, it is possible to avoid a single adjustment that is too large, so that the minimum CTLE is used to achieve high-frequency attenuation compensation that meets actual needs.

[0032] In an embodiment, the correction instruction includes a gain adjustment instruction. The gain adjustment instruction is configured to instruct at least one of the following: to increase a high-frequency gain of the analog equalizer in the AFE circuit according to a first step size; to reduce a low-frequency gain of the analog equalizer in the AFE circuit according to a second step size.

[0033] In this embodiment, the gain adjustment instruction is configured to instruct adjusting the compensation function of CTLE step by step. For example, in the initial stage of the calibration process, it is possible to give priority to increasing the high-frequency gain according to the first step size. If the required positive eye height cannot be obtained only by increasing the high-frequency gain, the gain adjustment instruction is updated to further instruct to reduce the low-frequency gain according to the second step size. For example, the gain adjustment instruction is LFG<y1:0>, which means reducing the low-frequency gain of CTLE, and y1 means the number of bits of the control code. The gain adjustment instruction is HFG<y1:0>, which means increasing the high-frequency gain of CTLE, and y2 means the number of bits of the control code. With the increase of LFG and HFG control codes, the low-frequency gain and high-frequency gain increase respectively.

[0034] It should be noted that the correction instruction may include both the compensation function enabling instruction and the gain adjustment instruction.

[0035] In an embodiment, during the calibration process, the high-frequency gain can be increased preferentially to obtain a higher overall gain, improve the signal-to-noise ratio of the received signal, and facilitate subsequent processing of the received signal. In some embodiments, during the calibration process, the high-frequency gain can also be increased and the low-frequency gain can be decreased at the same time, or the low-frequency gain can be

decreased preferentially. If the high-frequency gain cannot be met, CTLE correction can also be achieved, but the overall gain of the signal will be reduced to a certain extent.

[0036] In an embodiment, the first step size and the second step size can be fixed values or dynamic values, which can be set or adjusted according to the channel type of signal transmission, the length of the backplane, the degree of channel attenuation, the number of CTLE stages, the difference between the positive eye height and the eye height threshold, etc. Taking the first step size as an example, the first step size can be a preset value, or can be determined according to the upper limit of the high-frequency gain. For example, the range of high-frequency gain is $[0, A]$, then the first step size can be $[0, A]/B$, B is a positive integer. In addition, in the initial stage of the correction process, the difference between the monitored positive eye height and the eye height threshold is large, and the first step size can be set to a larger value. As the correction process proceeds, the difference between the monitored positive eye height and the eye height threshold gradually decreases, and the first step size can be gradually reduced in a linear or non-linear manner, so as to avoid excessive adjustment range.

[0037] In an embodiment, the operation 110 includes:

[0038] Operation 1110, sampling the output signal through a first decision circuit and a clock data recovery (CDR) circuit to obtain a first data signal, an edge signal and a two-phase clock corresponding to the first data signal and the edge signal.

[0039] Operation 1120, sampling the output signal according to a sampling clock through a second decision circuit to obtain a second data signal.

[0040] Operation 1130, comparing the second data signal with the first data signal to determine a relationship between the monitored positive eye height and the eye height threshold.

[0041] In this embodiment, the first decision circuit is configured to sample the output signal of the AFE circuit to obtain the first data signal and the edge signal. There may be two first decision circuits in the receiver, and the two first decision circuits are respectively configured to output the first data signal and the edge signal. The first data signal and the edge signal are input to the CDR circuit to recover the two-phase clock and serve as the sampling clock of the first decision circuit. In the scenario of high-speed serial communication, only serial data is transmitted on the channel, and no clock signal is transmitted. The received serial data can be clock recovered through the CDR circuit, so as to obtain accurate and reliable received data. The clock corresponding to the first data signal and the clock corresponding to the edge signal are inverted clocks.

[0042] Besides, the second decision circuit is configured to sample the output signal according to the sampling clock to obtain a second data signal. Each bit of the second data signal

is 0 or 1, respectively indicating whether the positive eye height corresponding to the bit is lower than the decision threshold. The decision threshold herein is the eye height threshold, which can be set by using the threshold voltage circuit. By comparing the first data signal with the second data signal, the degree of intersymbol interference can be analyzed, so as to determine whether the monitored positive eye height reaches the eye height threshold, and then determine a correction strategy for CTLE.

[0043] In an embodiment, a sampling clock corresponding to the second data signal is synchronized and edge-aligned with a clock corresponding to the first data signal.

[0044] In this embodiment, the sampling clock of the second decision circuit is synchronized and edge-aligned with the sampling clock of the first decision circuit to obtain the first data signal, to ensure that the second data signal output by the second decision circuit is the same data as the first data signal output by the first decision circuit.

[0045] In an embodiment, the operation 1103 includes:

[0046] in response to detecting a clock lock signal, reading the second data signal and the first data signal of the same length; XORing a bit with a value of 1 in the first data signal and a value of a corresponding bit in the second data signal, and accumulating XOR results of each bit; in response to that the accumulation result is 0, determining that the monitored positive eye height reaches the eye height threshold; or in response to that the accumulation result is not 0, determining that the monitored positive eye height is lower than the eye height threshold or a positive eye diagram of the output signal is closed.

[0047] In this embodiment, the decision threshold of the second decision circuit, that is, the eye height threshold is denoted as V_{TH1} . When the clock lock signal (that is, $CDR_LOCK=1$) is detected, the first data signal and the second data signal of the same length are read. XORing a bit with a value of 1 in the first data signal with a corresponding bit in the second data signal. Then, the XOR result is accumulated, and the accumulation result shows that the first data signal is consistent with the second data signal. If the accumulation result is 0, it indicates that the first data signal is completely consistent with the second data signal, an indication signal $Eyeopen=1$ can be output, indicating that the eye diagram of the output signal is open and the positive eye height is greater than or equal to V_{TH1} , and CTLE does not need to be corrected. If the accumulation result is not 0, it indicates that the first data signal is not completely consistent with the second data signal, and then an indication signal $Eyeopen=0$ can be output, indicating that the positive eye height is lower than V_{TH1} or the eye diagram is closed, and CTLE needs to be corrected.

[0048] In an embodiment, the operation 120 includes:

[0049] Operation 1210, in response to that the monitored positive eye height is lower than the eye height threshold, determining an on-off state of the compensation function of each analog equalizer in the AFE circuit, and a gain adjustment strategy for the analog equalizer based on the first data signal, the second data signal and the clock lock signal.

[0050] Operation 1220, generating the correction instruction based on the on-off state and the gain adjustment strategy.

[0051] In this embodiment, when the clock lock signal (i.e., CDR_LOCK=1) is detected, according to the first data signal and the second data signal, different on-off states and/or gain adjustment strategies of CTLE can be determined, and different correction instructions can be generated. For example, when the clock lock signal (i.e., CDR_LOCK=1) is detected, ESDATA and DATA of the same length are read. If the accumulation result is 0, CTLE does not need to be corrected. If the accumulation result is not 0, CTLE needs to be corrected. The larger the accumulation result is, the more inconsistent bits the first data signal and the second data signal have. In this case, the more CTLEs that need to enable the compensation function, or the larger the range of gain adjustment (i.e., the step size).

[0052] In an embodiment, the method further includes:

[0053] Operation 140, determining a relationship between an amplitude of the output signal and an amplitude threshold based on the second data signal; and

[0054] Operation 150, determining whether the low-frequency gain of the analog equalizer in the AFE circuit is reduced to a lower limit based on the relationship between the amplitude of the output signal and the amplitude threshold.

[0055] In this embodiment, the amplitude of the output signal is also monitored to ensure that the low-frequency gain of the analog equalizer will not be too low, so as to prevent the subsequent processing from being affected by the too small amplitude of the received signal.

[0056] In an embodiment, when the amplitude of the output signal needs to be monitored, there may be one or more second decision circuits. The first decision circuit may perform sampling based on the eye height threshold (VTH1) during the entire correction process to obtain the first data signal. Each bit of the first data signal being 0 or 1 respectively indicates whether the positive eye height corresponding to the bit is lower than the eye height threshold, the control chip can determine the relationship between the monitored positive eye height and the eye height threshold, so as to determine whether the CTLE needs to be corrected. The second decision circuit is mainly configured to obtain the second data signal by sampling based on the amplitude threshold (VTH2) during the correction process of reducing the low-frequency gain, each bit of the second data signal being 0 or 1 respectively indicates whether the amplitude of the bit is

greater than or equal to the amplitude threshold, the control chip can determine the relationship between the amplitude of the output signal and the amplitude threshold, and then determine whether the low-frequency gain has been reduced to the lower limit. If yes, the correction is done, if not, the low-frequency gain can be continued to increase the positive eye height. When there is only one second decision circuit, the second decision circuit can be alternately used to obtain the first data signal and the second data signal. When there are two second decision circuits, one of them can be used to obtain the first data signal based on the eye height threshold, and the other can be used to obtain the second data signal based on the amplitude threshold.

[0057] In an embodiment, the operation 140 includes:

[0058] in response to detecting the clock lock signal, reading the second data signal of a set length; counting number of bits with a value of 1 in the second data signal, or accumulating the values of each bit in the second data signal; in response to that the number of bits with a value of 1 is greater than or equal to a set value, or the accumulation result is greater than or equal to the set value, determining that the amplitude of the output signal reaches the amplitude threshold; in response to that the number of bits with a value of 1 is less than the set value, or the accumulation result is less than the set value, determining that the amplitude of the output signal is lower than the amplitude threshold.

[0059] In this embodiment, the decision threshold of the second decision circuit, that is, the amplitude threshold is recorded as VTH2. When the clock lock signal (i.e. CDR_LOCK=1) is detected, the second data signal of the set length is read, and the number of digits with a value of 1 in the second data signal is counted, or the values of each bit in the second data signal are accumulated, and the obtained number of digits or accumulation result reflects the amplitude of the output signal. If the obtained number of digits or the accumulation result is greater than or equal to the set value (for example, 1), the indicator signal Vamp_valid=1 is output, indicating that the output signal amplitude is greater than or equal to VTH2, and the low-frequency gain can continue to decrease. If the obtained number of digits or the accumulated result is less than the set value, the indicator signal Vamp_valid=0 is output, indicating that the output signal amplitude is less than VTH2, and the low-frequency gain has been reduced to the lower limit.

[0060] In an embodiment, the operation 130 includes:

[0061] Operation 1310, enabling the compensation function of the analog equalizer in the AFE circuit according to the correction instruction;

[0062] Operation 1320, based on an initial state, increasing the high-frequency gain of the analog equalizer in the AFE circuit according to the first step size until the monitored positive eye height reaches the eye height threshold; and

[0063] Operation 1330, in response to that the high-frequency gain of the analog equalizer is increased to an upper limit and the monitored positive eye height has not yet reached the eye height threshold, enabling the compensation function of at least one stage of the analog equalizer that is not enabled and repeating the operation of increasing the high-frequency gain, or reducing the low-frequency gain of the analog equalizer in the AFE circuit according to the second step size until the monitored positive eye height reaches the eye height threshold.

[0064] In this embodiment, the correction of CTLE is carried out in layers, including enabling the compensation function of CTLE at all stages step by step; prioritize gradually increasing the high-frequency gain of CTLE. If the high-frequency gain increases to the upper limit and the monitored positive eye height still has not yet reached the eye height threshold, more CTLE compensation functions can be enabled, and the low-frequency gain of CTLE can also be gradually reduced. The three-stage CTLE included in the AFE circuit is taken as an example for illustration. The positive eye height of the output signal of the AFE circuit is monitored in real time. First, when the monitored positive eye height is lower than the eye height threshold, a correction instruction CTLE_BOOST_EN<2:0>=000 is generated, that is, the compensation functions of the three stages of CTLE are all turned off, and CTLE is equivalent to a buffer at this time.

[0065] Then, whether the current positive eye height is open and whether the current positive eye height reaches the eye height threshold (whether Eyeopen=1) are monitored, if so, the CTLE configuration is kept, and the adaptive correction process is completed, otherwise, the compensation function of CTLE 1 is enabled, the low-frequency gain of the three-stage CTLE is set to the maximum value, and the high-frequency gain is set to the minimum value of 0.

[0066] Next, whether the current positive eye height is open and whether the current positive eye height reaches the eye height threshold (whether Eyeopen=1) are monitored, if so, the CTLE configuration is kept, and the adaptive correction process is completed, otherwise, when the high-frequency gain does not reach the upper limit, the high-frequency gain is increased by 1 each time until Eyeopen=1. If the high-frequency gain reaches the upper limit and Eyeopen=0, the compensation functions of CTLE 1 and CTLE 2 are enabled, the low-frequency gain of the three-stage CTLE is set to the maximum value, and the high-frequency gain is set to the minimum value of 0.

[0067] Again, whether the current positive eye height is open and whether the current positive eye height reaches the eye height threshold (whether Eyeopen=1) are monitored, if so, the CTLE configuration is kept, and the adaptive correction process is completed, otherwise, when the high-frequency gain does not reach the upper limit, the high-frequency gain is

increased by 1 each time until Eyeopen=1. If the high-frequency gain reaches the upper limit and Eyeopen=0, the compensation functions of CTLE 1, CTLE 2 and CTLE 3 are enabled, the low-frequency gain of the three-stage CTLE is set to the maximum value, and the high-frequency gain is set to the minimum value of 0.

[0068] Finally, when the compensation functions of CTLE at all stages are all enabled, whether the current positive eye height is open and whether the current positive eye height reaches the eye height threshold (whether Eyeopen=1) are monitored, if so, the CTLE configuration is kept, and the adaptive correction process is completed. Otherwise, when the high-frequency gain has not reached the upper limit, the high-frequency gain is increased by 1 each time until Eyeopen=1. If the high-frequency gain reaches the upper limit, Eyeopen=0, and the low-frequency gain can also be reduced.

[0069] In an embodiment, the operation 130 includes:

[0070] Operation 1340, in response to that the amplitude of the output signal is not lower than the amplitude threshold and the low-frequency gain of the analog equalizer is not lower than the lower limit, decreasing the low-frequency gain of the analog equalizer in the AFE circuit according to the second step size until the monitored positive eye height reaches the eye height threshold.

[0071] In this embodiment, the positive eye height can also be increased by reducing the low-frequency gain. For example, when the compensation functions of CTLE 1, CTLE 2 and CTLE 3 are all enabled and the high-frequency gain has reached the upper limit, in a case where the positive eye height has not yet reached the eye height threshold, it may be determined whether the low-frequency gain is higher than the lower limit and the low-frequency gain is not 0. If yes, the low-frequency gain is reduced by 1 each time until Eyeopen=1; otherwise, stop the correction process, and finally the positive eye height does not reach the eye height threshold, and Eyeopen=0.

[0072] In an embodiment, the initial state includes: the low-frequency gain of the analog equalizer is set to a maximum value, and the high-frequency gain of the analog equalizer is set to a minimum value.

[0073] In this embodiment, based on the initial state, the high-frequency gain can be gradually increased from the minimum value of the high-frequency gain, or the low-frequency gain can be gradually reduced from the maximum value of the low-frequency gain, so as to avoid excessive adjustment and optimize the performance of the receiver.

[0074] FIG. 2 is a flowchart of a method for correcting an analog equalizer according to another embodiment of the present application. In this embodiment, the layered correction

process is described by taking the CTLE compensation function step by step and giving priority to increasing the high-frequency gain as an example. For technical details not exhaustively described in this embodiment, reference may be made to any of the foregoing embodiments.

[0075] As shown in FIG. 2, the method includes:

[0076] a. Sampling the output signal by the first decision circuit (denoted as SLICER) and the CDR circuit, to obtain the first data signal (denoted as DATA), the edge signal (denoted as EDGE), and the two-phase clocks corresponding to the first data signal and the edge signal (denoted as CLK0 and CLK180 respectively). CLK0 and CLK180 are inverted clocks.

[0077] b. Sampling the output signal according to the sampling clock (denoted as ECLK0) by the second judgment circuit (denoted as ESSLICER) to obtain the second data signal (denoted as ESDATA). ECLK0 is synchronized and edge-aligned with CLK0.

[0078] c. Comparing the first data signal with the second data signal to determine the relationship between the monitored positive eye height and the eye height threshold. It should be noted that, the XOR and accumulation operations of the first data signal and the second data in the above embodiments may be used to determine the relationship between the monitored positive eye height and the eye height threshold.

[0079] d. The monitored positive eye height is lower than the eye height threshold? If yes, execute e; if not, complete the analog equalizer correction.

[0080] e. Generating the correction instruction, and enabling the compensation function of the analog equalizer in the AFE circuit according to the correction instruction, and entering the initial state. It can instruct to enable the compensation function of one or more stages of CTLE, and can also instruct to disable the compensation function of all stages of CTLE.

[0081] f. The monitored positive eye height reaches the eye height threshold? If yes, complete the analog equalizer correction; if not, execute g.

[0082] g. Increasing the high-frequency gain of the analog equalizer in the AFE circuit according to the first step size.

[0083] h. The monitored positive eye height reaches the eye height threshold? If yes, complete the analog equalizer correction; if not, execute i.

[0084] i. The high-frequency gain of the analog equalizer is increased to the upper limit? If yes, execute j, if not, return to execute g.

[0085] j. Are the compensation functions of the analog equalizer in the AFE circuit all enabled? If yes, execute l; if not, execute k.

[0086] k. Enabling the compensation function of at least one stage of the analog equalizer that is not enabled and entering the initial state.

[0087] l. Reducing the low-frequency gain of the analog equalizer in the AFE circuit according to a second step size.

[0088] m. The monitored positive eye height reaches the eye height threshold? If yes, complete the analog equalizer correction; if not, execute n.

[0089] n. The amplitude of the output signal is higher than the amplitude threshold and the low-frequency gain of the analog equalizer is greater than 0? If yes, return to execute l; if not, complete the analog equalizer correction.

[0090] It should be noted that before reducing the low-frequency gain, it can be determined whether the amplitude of the output signal is higher than the amplitude threshold, and whether the low-frequency gain is greater than 0 (that is, the LFG in the gain adjustment instruction is greater than 0). Therefore, it is determined whether the low-frequency gain can be continuously reduced, so as to prevent the overall gain of the received signal from being too low and avoid reducing the quality of the received signal. The statistical or cumulative operation of the second data signal in the above embodiments may be used to determine the relationship between the amplitude of the output signal and the amplitude threshold.

[0091] In this embodiment, the first decision circuit is configured to obtain the first data signal and the edge signal based on the eye height threshold, and then perform clock recovery to obtain accurate and reliable received data. The second decision circuit is configured to obtain the second data signal. On this basis, according to the numerical similarities and differences between the data path (i.e., the first data signal) of the first decision circuit locked by the CDR clock and the normal data path (i.e., the second data signal), it can be determined whether the positive eye height of the output signal reaches the eye height threshold, and whether the amplitude of the output signal reaches the amplitude threshold can be determined according to the second data signal, so as to make effective correction decisions. By enabling the compensation function of CTLE stage by stage, the high-frequency gain is gradually increased or the low-frequency gain is gradually reduced to achieve fine adaptive correction, which has high efficiency and wide applicability, does not require complex algorithms, and the control logic is simple.

[0092] Embodiments of the present application further provide a device for correcting an analog equalizer. FIG. 3 is a schematic structural diagram of the device for correcting an analog equalizer according to an embodiment of the present application. As shown in FIG. 3, the device for correcting an analog equalizer includes a monitoring module 210, a control module 220 and a correction module 230.

[0093] The monitoring module 210 is configured to monitor a positive eye height of an output signal of an analog front end (AFE) circuit, and the AFE circuit includes at least one stage

of analog equalizer.

[0094] The control module 220 is configured to generate a correction instruction in response to that the monitored positive eye height is lower than an eye height threshold.

[0095] The correction module 230 is configured to correct the analog equalizer in the AFE circuit according to the correction instruction until the monitored positive eye height reaches the eye height threshold.

[0096] This embodiment of the present application provides the device for correcting an analog equalizer. The positive eye height is taken as the basis for correction, the positive eye height of the signal is high enough to improve the quality of the eye diagram and the quality of the output signal of the AFE circuit by correcting the analog equalizer. Therefore, the adaptive correction of the analog equalizer is realized, which can be used in any channel attenuation scene, and the circuit structure is simple and easy to implement.

[0097] In an embodiment, the correction instruction includes a compensation function enabling instruction.

[0098] The compensation function enabling instruction is configured to instruct to enable a compensation function of the analog equalizer in the AFE circuit.

[0099] In an embodiment, the correction instruction includes a gain adjustment instruction; the gain adjustment instruction is configured to instruct at least one of the following: to increase a high-frequency gain of the analog equalizer in the AFE circuit according to a first step size; to reduce a low-frequency gain of the analog equalizer in the AFE circuit according to a second step size.

[0100] In an embodiment, the monitoring module includes:

[0101] a first decision unit, configured to sample the output signal through a first decision circuit and a clock data recovery circuit to obtain a first data signal, an edge signal and a two-phase clock corresponding to the first data signal and the edge signal;

[0102] a second decision unit, configured to sample the output signal according to a sampling clock through a second decision circuit to obtain a second data signal; and

[0103] a first monitoring unit, configured to compare the second data signal with the first data signal to determine a relationship between the monitored positive eye height and the eye height threshold.

[0104] In an embodiment, the first monitoring unit is further configured to:

[0105] in response to detecting a clock lock signal, read the second data signal and the first data signal of the same length;

[0106] XOR a bit with a value of 1 in the first data signal and a value of a corresponding bit

in the second data signal, and accumulating XOR results of each bit;

[0107] in response to that the accumulation result is 0, determine that the monitored positive eye height reaches the eye height threshold; or

[0108] in response to that the accumulation result is not 0, determine that the monitored positive eye height is lower than the eye height threshold or a positive eye diagram of the output signal is closed.

[0109] In an embodiment, a sampling clock corresponding to the second data signal is synchronized and edge-aligned with a clock corresponding to the first data signal.

[0110] In an embodiment, the control module 220 is configured to:

[0111] in response to that the monitored positive eye height is lower than the eye height threshold, determine an on-off state of the compensation function of each analog equalizer in the AFE circuit, and a gain adjustment strategy for the analog equalizer according to the first data signal, the second data signal and the clock lock signal; and

[0112] generate the correction instruction according to the on-off state and the gain adjustment strategy.

[0113] In an embodiment, the monitoring module 210 further includes:

[0114] a second monitoring unit, configured to determine a relationship between an amplitude of the output signal and an amplitude threshold according to the second data signal; and determine whether the low-frequency gain of the analog equalizer in the AFE circuit is reduced to a lower limit according to the relationship between the amplitude of the output signal and the amplitude threshold.

[0115] In an embodiment, the second monitoring unit is further configured to:

[0116] in response to detecting the clock lock signal, read the second data signal of a set length;

[0117] count number of bits with a value of 1 in the second data signal, or accumulate the values of each bit in the second data signal;

[0118] in response to that the number of bits with a value of 1 is greater than or equal to a set value, or the accumulation result is greater than or equal to the set value, determine that the amplitude of the output signal reaches the amplitude threshold;

[0119] in response to that the number of bits with a value of 1 is less than the set value, or the accumulation result is less than the set value, determine that the amplitude of the output signal is lower than the amplitude threshold.

[0120] In an embodiment, the correction module 230 is configured to:

[0121] enable the compensation function of the analog equalizer in the AFE circuit according

to the correction instruction;

[0122] based on an initial state, increase the high-frequency gain of the analog equalizer in the AFE circuit according to the first step size until the monitored positive eye height reaches the eye height threshold; and

[0123] in response to that the high-frequency gain of the analog equalizer is increased to an upper limit, the monitored positive eye height has not yet reached the eye height threshold, enable the compensation function of at least one stage of the analog equalizer that is not enabled and repeat the operation of increasing the high-frequency gain, or reduce the low-frequency gain of the analog equalizer in the AFE circuit according to the second step size until the monitored positive eye height reaches the eye height threshold.

[0124] In an embodiment, the correction module 230 is configured to:

[0125] in response to that the amplitude of the output signal is not lower than the amplitude threshold and the low-frequency gain of the analog equalizer is not lower than the lower limit, decrease the low-frequency gain of the analog equalizer in the AFE circuit according to the second step size until the monitored positive eye height reaches the eye height threshold.

[0126] In an embodiment, the initial state includes: the low-frequency gain of the analog equalizer is set to a maximum value, and the high-frequency gain of the analog equalizer is set to a minimum value.

[0127] The device for correcting the analog equalizer in this embodiment and the method for correcting the analog equalizer in the above embodiments belong to the same inventive concept. For technical details that are not exhaustively described in this embodiment, reference may be made to any of the above-mentioned embodiments, and this embodiment has the same beneficial effects as performing the method for correcting the analog equalizer.

[0128] Embodiments of the present application further provide a control chip. FIG. 4 is a schematic diagram of a hardware structure of a control chip according to an embodiment of the present application. As shown in FIG. 4, the control chip in this embodiment includes a memory 32, a processor 31, and a computer program stored in the memory and operable on the processor. When the processor 31 executes the program, the above correction method is realized.

[0129] The control chip can further include a memory 32. The processor 31 in this control chip can be one or more, one processor 31 is taken as example in FIG. 4. The memory 32 is configured to store one or more programs. The one or more programs are executed by the one or more processors 31, so that the one or more processors 31 implement the method for correcting the analog equalizer as described in the embodiments of the present application.

[0130] The control chip further includes a communication device 33, an input device 34 and

an output device 35.

[0131] The processor 31, the memory 32, the communication device 33, the input device 34 and the output device 35 in the control chip can be connected through a bus or in other ways. In FIG. 4, connection through a bus is taken as an example.

[0132] The input device 34 can be configured to receive inputted number or character information, and generate key signal input related to user setting and function control of the control chip. The output device 35 may include a display device such as a display screen.

[0133] The communication device 33 may include a receiver and a transmitter. The communication device 33 is configured to perform information sending and receiving communication according to the control of the processor 31.

[0134] The memory 32, as a computer-readable storage medium, can be configured to store software programs, computer-executable programs and modules, such as program instructions/modules corresponding to the method for correcting the analog equalizer described in the embodiment of the present application (for example, the monitoring module 210, the control module 220, and the correction module 230 in the device for correcting the analog equalizer). The memory 32 may include a program storage area and a data storage area. The program storage area can store an operating system, an application program required by at least one function; the data storage area can store data created according to the use of the control chip, and the like. In addition, the memory 32 may include a high-speed random access memory, and may also include a non-volatile memory, such as at least one magnetic disk storage device, flash memory device, or other non-volatile solid-state storage devices. In some examples, the memory 32 may further include a memory that is remotely located relative to the processor 31, and these remote memories may be connected to the control chip through a network. Examples of the aforementioned networks include, but are not limited to, the Internet, intranets, local area networks, mobile communication networks, and combinations thereof.

[0135] Embodiments of the present application further provide a receiver. FIG. 5 is a schematic structural diagram of a receiver according to an embodiment of the present application. As shown in FIG. 5, the system includes an analog front end (AFE) circuit, a monitoring circuit, and the control chip as described in the above-mentioned embodiment. The output end of the AFE circuit is connected to the input end of the monitoring circuit. The output end of the monitoring circuit is connected to the input end of the control chip. The control chip is configured to correct the analog equalizer in the AFE circuit according to the monitoring result of the monitoring circuit.

[0136] This embodiment of the present application provides a receiver. The positive eye

height is taken as the basis for correction, the positive eye height of the signal is high enough to improve the quality of the eye diagram and the quality of the output signal of the AFE circuit by correcting the analog equalizer. Therefore, the adaptive correction of the analog equalizer is realized, which can be used in any channel attenuation scene, and the circuit structure is simple and easy to implement.

[0137] In an embodiment, the monitoring circuit includes a first decision circuit, a clock data recovery circuit and a second decision circuit.

[0138] In this embodiment, the output signal is sampled through a first decision circuit and a clock data recovery circuit to obtain a first data signal, an edge signal, and a two-phase clock corresponding to the first data signal and the edge signal; the output signal is sampled according to the sampling clock by the second decision circuit to obtain a second data signal; the second data signal is compared with the first data signal to determine the relationship between the monitored positive eye height and the eye height threshold.

[0139] FIG. 6 is a schematic diagram of a working principle of a receiver according to an embodiment of the present application. As shown in FIG. 6, the signal received by the receiver passes through the on die termination (ODT) used to weaken signal reflection, three-stage CTLE, two SLICER circuits, CDR circuit, ESSLICER circuit, VTH circuit, data demultiplexer (DMUX) circuit and control chip in sequence. The AFE circuit includes slice ODT and CTLE. The high-speed serial data signal sent by the transmitter (TX) reaches the input terminal of the receiver (RX) after channel attenuation and interference. The eye diagram may be closed or not open to a preset degree. By adjusting the on-off state and/or gain of the compensation function of the three-stage CTLE, the eye diagram of the output signal of the AFE circuit can be opened to a preset stage to realize correct data transmission.

[0140] The correction instruction generated by the control chip includes the compensation function enabling instruction, for example, CTLE_BOOST_EN<2:0> is configured to control the on-off state of the compensation function of the three-stage CTLE. The correction instruction can further include a gain adjustment instruction, for example, LFG<4:0> is configured to control the overall low-frequency gain of the three-stage CTLE, and HFG<4:0> is configured to control the overall high-frequency gain of the three-stage CTLE. The larger the control code of the LFG or HFG instruction, the greater the adjustment range of the low-frequency gain or high-frequency gain.

[0141] As shown in FIG. 6, the output signal of the AFE circuit is input to two SLICER circuits, which are respectively sampled to obtain the first data signal and the edge signal. The two-phase clocks CLK0 and CLK180 output by the CDR are respectively configured for the

sampling decision of the two SLICER circuits. The first data signal and the edge signal are input to the CDR circuit for clock recovery. The VTH circuit can be configured to set the decision threshold (VTH1 and/or VTH2) of the ESSLICER circuit, and the sampling clock ECLK0 of the ESSLICER is synchronized and edge-aligned with the sampling clock CLK0 of the SLICER for sampling the first data signal. The control chip corrects the CTLE according to the first data signal, the second data signal and the clock lock signal, and the recovered correct data can be output to the physical coding sublayer (PCS) through the DMUX after the correction is completed.

[0142] It should be noted that in this embodiment, the number of stages of CTLE, the number of bits of the control code in the calibration instruction, and the number of ESSLICER and VTH are not limited. The decision thresholds corresponding to the first decision circuit and the second decision circuit can be fixed values or dynamic values.

[0143] The receiver in this embodiment and the correction method in the above embodiments belong to the same inventive concept. For technical details that are not exhaustively described in this embodiment, reference may be made to any of the above-mentioned embodiments, and this embodiment has the same beneficial effects as performing a correction method for an analog equalizer.

[0144] Embodiments of the present application further provide a storage medium. The storage medium stores a computer program, and when the computer program is executed by a processor, any method for correcting the analog equalizer in the embodiments of the present application is implemented. The method includes: monitoring a positive eye height of an output signal of an analog front end (AFE) circuit, the AFE circuit including at least one stage of analog equalizer; generating a correction instruction in response to that the monitored positive eye height is lower than an eye height threshold; and correcting the analog equalizer in the AFE circuit according to the correction instruction until the monitored positive eye height reaches the eye height threshold.

[0145] The computer storage medium in the embodiments of the present application may use any combination of one or more computer-readable media. The computer-readable medium may be a computer-readable signal medium or a computer-readable storage medium. The computer-readable storage medium may be, for example, but not limited to: electrical, magnetic, optical, electromagnetic, infrared, or semiconductor system, or device, or any combination thereof. More specific examples (non-exhaustive list) of computer-readable storage media include: electrical connection with one or more wires, laptop computer disk, hard disk, random access memory (RAM), read only memory (ROM), erasable programmable read-only memory

(EPROM), flash memory, optical fiber, portable CD-ROM, optical storage device, magnetic storage device, or any suitable combination of the above. The computer-readable storage medium may be any tangible medium that contains or stores a program for use by or in connection with an instruction execution system, apparatus, or device.

[0146] The program code embodied on the computer-readable medium may be transmitted using any appropriate medium, including but not limited to wireless, wire, optical cable, Radio Frequency (RF), etc., or any suitable combination of the foregoing.

[0147] The computer program code for carrying out the operations of the present application may be written in one or more programming languages or a combination thereof, such programming languages include object-oriented programming languages, such as Java, Smalltalk, C++, and further include conventional procedural programming languages, such as the “C” language or similar programming languages. The program code may execute entirely on the user’s computer, partly on the user’s computer, as a stand-alone software package, partly on the user’s computer and partly on a remote computer or entirely on the remote computer or server. Where a remote computer is involved, the remote computer may be connected to the user computer through any kind of network, including a local area network (LAN) or a wide area network (WAN), or, may be connected to an external computer (e.g., via an Internet connection using an Internet service provider).

[0148] The above descriptions are merely exemplary embodiments of the present application, and are not intended to limit the scope of the present application.

[0149] Those skilled in the art will understand that the term user terminal covers any suitable type of wireless user equipment, such as a mobile phone, a portable data processing device, a portable web browser or a vehicle-mounted mobile station.

[0150] In general, the various embodiments of the present application can be implemented in hardware or special purpose circuits, software, logic or any combination thereof. For example, some aspects may be implemented in hardware, while other aspects may be implemented in firmware or software, which may be executed by a controller, microprocessor or other computing device, although the present application is not limited thereto.

[0151] Embodiments of the present application may be implemented by a data processor of a mobile device executing computer program instructions, for example in a processor entity, or by hardware, or by a combination of software and hardware. The computer program instructions may be assembly instructions, instruction set architecture (ISA) instructions, machine instructions, machine-related instructions, microcode, firmware instructions, state setting data, or source or object code written in any combination of one or more programming languages.

[0152] The foregoing has provided a detailed description of exemplary embodiments of the present application by way of exemplary and non-limiting examples. However, considering the accompanying drawings and the claims, various modifications and adjustments to the above embodiments are obvious to those skilled in the art, but do not depart from the scope of the present application. Therefore, the proper scope of the present application will be determined from the claims.

CLAIMS

What is claimed is:

1. A method for correcting an analog equalizer, comprising:
monitoring a positive eye height of an output signal of an analog front end (AFE) circuit, the AFE circuit comprising at least one stage of analog equalizer;
generating a correction instruction in response to that the monitored positive eye height is lower than an eye height threshold; and
correcting the analog equalizer in the AFE circuit according to the correction instruction until the monitored positive eye height reaches the eye height threshold.
2. The method according to claim 1, wherein the correction instruction comprises a compensation function enabling instruction, and the compensation function enabling instruction is configured to instruct to enable a compensation function of the analog equalizer in the AFE circuit.
3. The method according to claim 1, wherein the correction instruction comprises a gain adjustment instruction;
the gain adjustment instruction is configured to instruct at least one of the following:
to increase a high-frequency gain of the analog equalizer in the AFE circuit according to a first step size;
to reduce a low-frequency gain of the analog equalizer in the AFE circuit according to a second step size.
4. The method according to any one of claims 1 to 3, wherein the monitoring the positive eye height of the output signal of the AFE circuit comprises:
sampling the output signal through a first decision circuit and a clock data recovery circuit to obtain a first data signal, an edge signal and a two-phase clock corresponding to the first data

signal and the edge signal;

sampling the output signal according to a sampling clock through a second decision circuit to obtain a second data signal; and

comparing the second data signal with the first data signal to determine a relationship between the monitored positive eye height and the eye height threshold.

5. The method according to claim 4, wherein the comparing the second data signal with the first data signal to determine the relationship between the monitored positive eye height and the eye height threshold comprises:

in response to detecting a clock lock signal, reading the second data signal and the first data signal of the same length;

XORing a bit with a value of 1 in the first data signal and a value of a corresponding bit in the second data signal, and accumulating XOR results of each bit;

in response to that the accumulation result is 0, determining that the monitored positive eye height reaches the eye height threshold; or

in response to that the accumulation result is not 0, determining that the monitored positive eye height is lower than the eye height threshold or a positive eye diagram of the output signal is closed.

6. The method according to claim 4 or 5, wherein a sampling clock corresponding to the second data signal is synchronized and edge-aligned with a clock corresponding to the first data signal.

7. The method according to any one of claims 4 to 6, wherein the generating the correction instruction in response to that the monitored positive eye height is lower than the eye height threshold comprises:

in response to that the monitored positive eye height is lower than the eye height threshold, determining an on-off state of the compensation function of each analog equalizer in the AFE circuit, and a gain adjustment strategy for the analog equalizer based on the first data signal, the second data signal and the clock lock signal; and

generating the correction instruction based on the on-off state and the gain adjustment strategy.

8. The method according to any one of claims 4 to 7, further comprising:

determining a relationship between an amplitude of the output signal and an amplitude threshold based on the second data signal; and

determining whether the low-frequency gain of the analog equalizer in the AFE circuit is reduced to a lower limit based on the relationship between the amplitude of the output signal and the amplitude threshold.

9. The method according to claim 8, wherein the determining the relationship between the amplitude of the output signal and the amplitude threshold based on the second data signal comprises:

in response to detecting the clock lock signal, reading the second data signal of a set length; counting number of bits with a value of 1 in the second data signal, or accumulating the values of each bit in the second data signal;

in response to that the number of bits with a value of 1 is greater than or equal to a set value, or the accumulation result is greater than or equal to the set value, determining that the amplitude of the output signal reaches the amplitude threshold;

in response to that the number of bits with a value of 1 is less than the set value, or the accumulation result is less than the set value, determining that the amplitude of the output signal is lower than the amplitude threshold.

10. The method according to any one of claims 1 to 9, wherein the correcting the analog equalizer in the AFE circuit according to the correction instruction until the monitored positive eye height reaches the eye height threshold comprises:

enabling the compensation function of the analog equalizer in the AFE circuit according to the correction instruction;

based on an initial state, increasing the high-frequency gain of the analog equalizer in the AFE circuit according to the first step size until the monitored positive eye height reaches the

eye height threshold; and

in response to that the high-frequency gain of the analog equalizer is increased to an upper limit and the monitored positive eye height has not yet reached the eye height threshold, enabling the compensation function of at least one stage of the analog equalizer that is not enabled and repeating the operation of increasing the high-frequency gain, or reducing the low-frequency gain of the analog equalizer in the AFE circuit according to the second step size until the monitored positive eye height reaches the eye height threshold.

11. The method according to any one of claims 1 to 9, wherein the correcting the analog equalizer in the AFE circuit according to the correction instruction until the monitored positive eye height reaches the eye height threshold comprises:

in response to that the amplitude of the output signal is not lower than the amplitude threshold and the low-frequency gain of the analog equalizer is not lower than the lower limit, decreasing the low-frequency gain of the analog equalizer in the AFE circuit according to the second step size until the monitored positive eye height reaches the eye height threshold.

12. The method according to claim 10, wherein the initial state comprises: the low-frequency gain of the analog equalizer is set to a maximum value, and the high-frequency gain of the analog equalizer is set to a minimum value.

13. A control chip, comprising: a memory, a processor, and a computer program stored on the memory and operable on the processor, when the computer program is executed by the processor, the method for correcting an analog equalizer according to any one of claims 1 to 12 is implemented.

14. A receiver, comprising:

an analog front end (AFE) circuit;

a monitoring circuit; and

the control chip according to claim 13,

wherein an output end of the AFE circuit is connected to an input end of the monitoring

circuit, an output end of the monitoring circuit is connected to an input end of the control chip, and the control chip is configured to correct an analog equalizer in the AFE circuit according to a monitoring result of the monitoring circuit.

15. The receiver according to claim 14, wherein:

the monitoring circuit comprises a first decision circuit, a clock data recovery circuit and a second decision circuit;

the first decision circuit is configured to sample an output signal of the AFE circuit according to a two-phase clock provided by the clock data recovery circuit to obtain a first data signal and an edge signal; and

the second decision circuit is configured to sample the output signal according to a sampling clock to obtain a second data signal.

16. A computer-readable storage medium, wherein a computer program is stored on the computer-readable storage medium, and when the computer program is executed by a processor, the method for correcting an analog equalizer according to any one of claims 1 to 12 is implemented.